High-Speed Amplifiers Data Book

Literature Number: SLOD005

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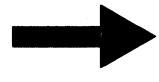
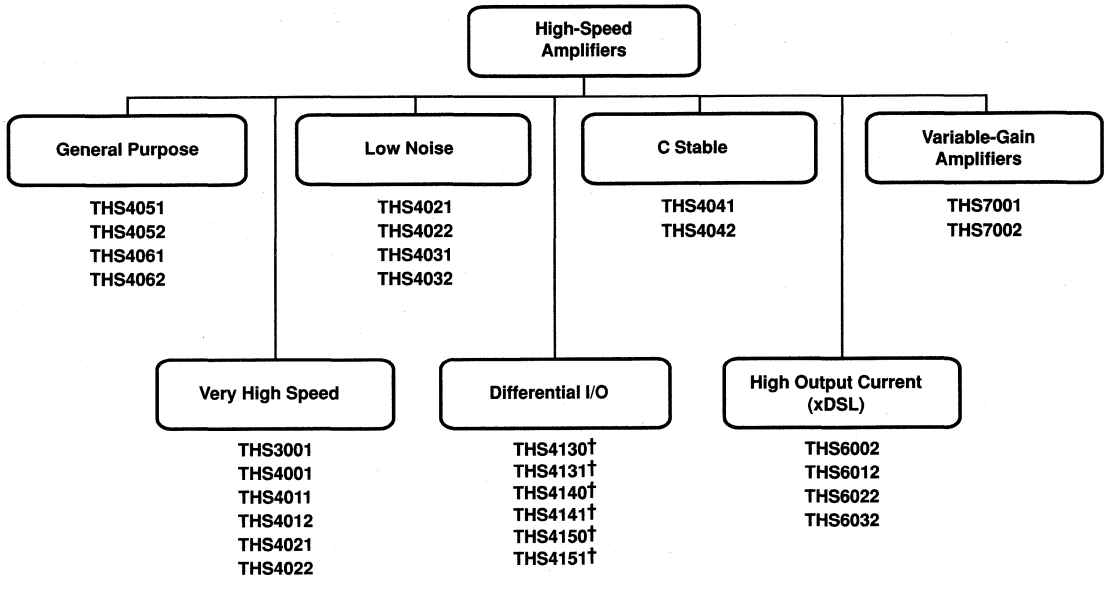
INTRODUCTION

What you will find inside...	Texas Instruments' High-Speed Amplifier Data Book presents technical information on a variety of **new High-Speed Amplifiers** from TI. This includes Data Sheets, an **Evaluation Module** selection guide, as well as a section dedicated to **Applications.** The **Evaluation Module development tools** are developed with one goal in mind: **Minimize Design Time** – the boards are specifically laid out for high-speed signals, with a user's manual, layout diagram, and response graphs. The final section contains packaging specifications, including tape and reel dimensions for the ultra-small MSOP PowerPAD™ package.
How the data book is organized...	1) Introduction and general information 2) High-Speed Amplifier Datasheets 3) Evaluation Modules 4) Application Notes (sorted alphabetically by title) 5) Mechanical Data
New products and applications...	• THS6002 • THS6012 • THS6022 • THS6032 • THS6062 • THS6072 • THS7002  • ADSL Central Office switches; DSLAMs; Remote Terminal modems • THS3001 • THS4001 • THS4011/2 • THS4021/2 • THS4031/2 • THS4041/2 • THS4051/2 • THS4061/2 • THS4081/2  • Communication • Imaging • Video/Multimedia • Instrumentation & Test Equipment • ADC/DAC buffers
Where to go for more information...	Download TI's latest datasheets and applications notes via the internet at: **http://www.ti.com/sc/docs/schome.htm** To provide full technical support, Texas Instruments has a large fully-staffed technical information center available to help you. Please turn to the last page of this data book for a complete listing of contacts ready to answer your questions.

Contents

† This device is in the **Product Preview** stage of development. Contact your local TI sales office for more information.

High-Speed Amplifier Selection Tree



† This device is in the **Product Preview** stage of development. Contact your local TI sales office for more information.

Evaluation Modules

To obtain a universal EVM board and amplifier samples for evaluation, select the appropriate EVM board from the following table and contact your local TI sales office, distributor, or the TI Product Information Center (listed on the last page of this book). Evaluation modules will be introduced in the future. Please check the web (**www.ti.com**) for the latest updates and manuals.

Device	EVM Part Number	EVM Literature Number	EVM User's Guide Literature Number
THS3001	THS3001EVM	SLOP130	SLOU021A
THS4001	THS4001EVM	SLOP119	SLOU017
THS4011	THS4011EVM	SLOP128	SLOU028
THS4012	THS4012EVM	SLOP230	SLOU041
THS4021	THS4021EVM	SLOP129	SLOU063
THS4022	THS4022EVM	SLOP231	SLOU064
THS4031	THS4031EVM	SLOP203	SLOU038
THS4032	THS4032EVM	SLOP135	SLOU039
THS4041	THS4041EVM	SLOP219	SLOU069
THS4042	THS4042EVM	SLOP233	SLOU070
THS4051	THS4051EVM	SLOP220	SLOU049
THS4052	THS4052EVM	SLOP234	SLOU050
THS4061	THS4061EVM	SLOP226	SLOU038
THS4062	THS4062EVM	SLOP235	SLOU040
THS6002	THS6002EVM	SLOP117	SLOU018
THS6012	THS6012EVM	SLOP132	SLOU034
THS6022	THS6022EVM	SLOP133	SLOU035
THS6062	THS6062EVM	SLOP221	SLOU036
THS7001	THS7001EVM	SLOP250	SLOU057
THS7002	THS7002EVM	SLOP136	SLOU037

Specification	Unit	Definition
A_D	%	**Differential Gain Error** The change in ac gain with the change in the dc level. This has applicability for television and is therefore usually measured at ac frequencies of 3.58 MHz (NTSC) or 4.43 MHz (PAL). The typical dc level change is 0 to ±0.7 V.
A_{phi}	Deg	**Differential Phase Error** The change in ac phase with the change in dc level. This has applicability for television and is therefore usually measured at ac frequencies of 3.58 MHz (NTSC) or 4.43 MHz (PAL). The typical dc level change is 0 to ±0.7 V.
A_{OL}	V/mV	**Open Loop Gain** In a voltage feedback amplifier (VFB), it is the output voltage divided by the input voltage at the input. This is typically measured by changing the output voltage in a closed loop system and measuring the change in input offset voltage.
BW	MHz	**Bandwidth** The frequency at which the output is reduced to 0.707 (–3 dB) of the low frequency value when passing a small signal sine wave.
	MHz	**Full Power Bandwidth** The maximum frequency of an amplifier in which the output amplitude is at the extents of its linear range.
C_I	pF	**Differential Input Capacitance** The equivalent capacitance from one input terminal to the other input terminal of an amplifier.
CMRR	dB	**Common-Mode Rejection Ratio** The ratio of differential voltage amplification to common-mode voltage amplification. Insufficient CMRR degrades circuit precision by effectively introducing a voltage offset as a function of dc level at the input. NOTE: This is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage.
I_{CC}	mA	**Supply Current** The current into the V_{CC+} or V_{CC-} terminal of an integrated circuit.
I_{IB}	µA	**Input Bias Current** The average of the currents into the two input terminals with the output at a specified level.
I_{OS}	nA	**Input Offset Current** The difference of the two input bias currents with the output at a specified level.
	nA/°C	**Input Offset Current Drift** The ratio of the change in input offset current to the change in temperature. This is an average value for the specified temperature range. $$\alpha_{IIO} = \frac{\left(I_{IO} \text{ at } T_{A(1)}\right) - \left(I_{IO} \text{ at } T_{A(2)}\right)}{T_{A(1)} - T_{A(2)}}$$
I_n	pA/√Hz	**Equivalent Input Noise Current** The current of an ideal current source (having an internal impedance equal to infinity) in parallel with the input terminals of the device that represents the part of the internally generated noise that can be properly represented by a current source.

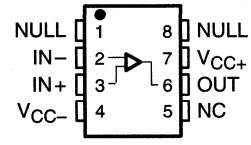
Specification	Unit	Definition
I_O	mA	**Output Current** The maximum output current that can be sinked or sourced by the amplifier for a specified load.
I_{SC}	mA	**Short-Circuit Output Current** The maximum output current available from the amplifier for a specified load, typically 20 Ω or less.
PSRR	dB	**Power Supply Rejection Ratio** The absolute value of the ratio of the change in input offset voltage to the change in supply voltages. NOTE: Unless otherwise noted, both supply voltages are varied symmetrically.
R_I	MΩ	**Input Resistance** The resistance between the input terminal and either input grounded. Typically done while in a closed-loop configuration.
R_O	Ω	**Output Resistance** The ratio of the change in output voltage to the change in output current for a specific load. This measurement is done while in an open-loop condition.
SR	V/μs	**Slew Rate** The average time rate of change of the closed-loop amplifier output voltage for a step-signal input. This is typically done at the 25% to 75% output signal levels.
THD	dBc	**Total Harmonic Distortion** The total amount of distortion in the output signal. This includes all harmonics of the fundamental signal summed up in an RMS method.
T_s	ns	**Settling Time** The amount of time to settle within a fixed percentage of the final output value when a step input is used.
V_{CC}	V	**Supply Voltage** The voltage applied to the V_{CC+} or V_{CC-} terminals of an integrated circuit.
V_{ICR}	V	**Common-Mode Input Voltage Range** The range of common-mode input voltage that if exceeded may cause the operational amplifier to cease functioning properly. Effectively, it is the maximum linear input voltage range of the amplifier.
V_{IO} / V_{OS}	mV	**Input Offset Voltage** The dc voltage that must be applied between the input terminals to force the quiescent dc output voltage to zero or other level, if specified.
	μV/°C	**Input Offset Voltage Drift** The ratio of the change in input offset voltage to the change in temperature. This is an average value for the specified temperature range. $\alpha_{VIO} = \frac{\left(V_{IO} \text{ at } T_{A(1)}\right) - \left(V_{IO} \text{ at } T_{A(2)}\right)}{T_{A(1)} - T_{A(2)}}$
V_O	V	**Output Voltage Swing** The maximum output voltage of the amplifier with a specified load resistance.

Specification	Unit	Definition
V_n/e_n	nV/√Hz	**Equivalent Input Noise Voltage** The voltage of an ideal voltage source (having an internal impedance equal to zero) in series with the input terminals of the device that represents the part of the internally generated noise that can be properly represented by a voltage source. The noise source of an amplifier is commonly modeled as a noise generator in series with the non-inverting input. This is known as input referred noise.
	dBc	**Crosstalk** A ratio (usually in dB) of the output voltage of an undriven amplifier to the output of a driven amplifier when there is two or more amplifiers in one package.
R_t	MΩ	**Open Loop Transresistance** In a current feedback amplifier (CFB), it is the ratio of change in output voltage to the change of the inverting input terminal error current. The equivalent of open loop gain for a voltage feedback amplifier (VFB).
$V_{IH-SHDN}$	V	**Turnon Voltage (Shutdown)** The voltage required on the shutdown pin to turn the device on.
$V_{IL-SHDN}$	V	**Turnoff Voltage (Shutdown)** The voltage required on the shutdown pin to turn the device off.
$I_{CC-SHDN}$	mA	**Supply Current (Shutdown)** The current into the V_{CC+} or V_{CC-} terminal of the amplifier while it is turned off.
t_{EN}	µs	**Turnon Time (Shutdown)** The time from when the turnon voltage is applied to the shutdown pin to when the supply current has reached half of its final value.
t_{DIS}	µs	**Turnoff Time (Shutdown)** The time from when the turnoff voltage is applied to the shutdown pin to when the supply current has reached half of its final value.

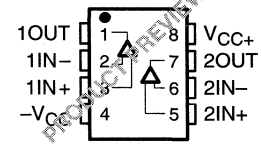
Contents

- **High Speed**
  - **420 MHz Bandwidth (G = 1, –3 dB)**
  - **6500 V/μs Slew Rate**
  - **40-ns Settling Time (0.1%)**
- **High Output Drive, I_O = 100 mA**
- **Excellent Video Performance**
  - **115 MHz Bandwidth (0.1 dB, G = 2)**
  - **0.01% Differential Gain**
  - **0.02° Differential Phase**
- **Low 3-mV (max) Input Offset Voltage**
- **Very Low Distortion**
  - **THD = –96 dBc at f = 1 MHz**
  - **THD = –80 dBc at f = 10 MHz**
- **Wide Range of Power Supplies**
  - **V_{CC} = ±4.5 V to ±16 V**
- **Evaluation Module Available**

THS3001
D AND DGN† PACKAGE
(TOP VIEW)



THS3002
D AND DGN PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

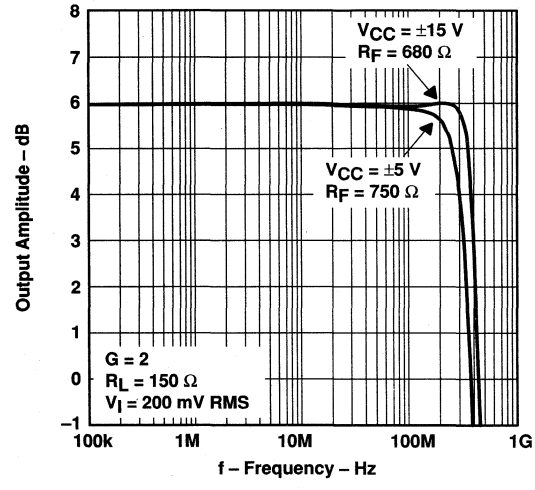
NC – No internal connection

† The THS3001 implemented in the DGN package is in the product preview stage of development. Contact your local TI sales office for availability.

description

The THS300x is a high-speed current-feedback operational amplifier, ideal for communication, imaging, and high-quality video applications. This device offers a very fast 6500-V/μs slew rate, a 420-MHz bandwidth, and 40-ns settling time for large-signal applications requiring excellent transient response. In addition, the THS300x operates with a very low distortion of –96 dBc, making it well suited for applications such as wireless communication basestations or ultrafast ADC or DAC buffers.

OUTPUT AMPLITUDE
vs
FREQUENCY



HIGH-SPEED AMPLIFIER FAMILY

DEVICE	ARCHITECTURE		SUPPLY VOLTAGE			BW (MHz)	SR (V/μs)	THD f = 1 MHz (dB)	t_s 0.1% (ns)	DIFF. GAIN	DIFF. PHASE	V_n (nV/√Hz)
	VFB	CFB	5 V	±5 V	±15 V							
THS3001/02		•		•	•	420	6500	–96	40	0.01%	0.02°	1.6
THS4001	•		•	•	•	270	400	–72	40	0.04%	0.15°	12.5
THS4011/12	•			•	•	290	310	–80	37	0.006%	0.01°	7.5
THS4031/32	•			•	•	100	100	–72	60	0.02%	0.03°	1.6
THS4061/62	•			•	•	180	400	–72	40	0.02%	0.02°	14.5

CAUTION: The THS300x provides ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE			EVALUATION MODULE
	SOIC† (D)	MSOP (DGN)		
		DEVICE	SYMBOL	
0°C to 70°C	THS3001CD THS3002CD‡	THS3001CDGN‡ THS3002CDGN‡	TIADP TIADI	THS3001EVM THS3002EVM‡
–40°C to 85°C	THS3001ID THS3002ID‡	THS3001IDGN‡ THS3002IDGN‡	TIADQ TIADJ	—

† The D package is available taped and reeled. Add an R suffix to the device type (i.e., THS3001CDR)
‡ Product Preview

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} to V_{CC-} . . . . . 33 V
Input voltage, V_I . . . . . $\pm V_{CC}$
Output Current, I_O . . . . . 175 mA
Differential input voltage, V_{ID} . . . . . ±6 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A, THS300xC . . . . . 0°C to 70°C
THS300xI . . . . . –40°C to 85°C
Storage temperature, T_{stg} . . . . . –65°C to 125°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	740 mW	6 mW/°C	470 mW	380 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} and V_{CC-}	Split supply	±4.5		±16	V
	Single supply	9		32	
Operating free-air temperature, T_A	THS300xC	0		70	°C
	THS300xI	–40		85	

electrical characteristics, T_A = 25°C, R_L = 150 Ω, R_F = 1 kΩ (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{CC}	Power supply operating range		Split supply		±4.5		±16.5	V
			Single supply		9		33	
I_{CC}	Quiescent current		V_{CC} = ±5 V	T_A = 25°C		5.5	7.5	mA
				T_A = full range			8.5	
			V_{CC} = ±15 V	T_A = 25°C		6.6	9	
				T_A = full range			10	
V_O	Output voltage swing		V_{CC} = ±5 V	R_L = 150 Ω	±2.9	±3.2		V
				R_L = 1 kΩ	±3	±3.3		
			V_{CC} = ±15 V	R_L = 150 Ω	±12.1	±12.8		
				R_L = 1 kΩ	±12.8	±13.1		
I_O	Output current (see Note 1)		V_{CC} = ±5 V,	R_L = 20 Ω		100		mA
			V_{CC} = ±15 V,	R_L = 75 Ω	85	120		
V_{IO}	Input offset voltage		V_{CC} = ±5 V or ±15 V	T_A = 25°C		1	3	mV
				T_A = full range			4	
	Input offset voltage drift		V_{CC} = ±5 V or ±15 V			5		µV/°C
I_{IB}	Input bias current	–Input	V_{CC} = ±5 V or ±15 V	T_A = 25°C		2	10	µA
				T_A = full range			15	
		+Input		T_A = 25°C		1	10	
				T_A = full range			15	
V_{ICR}	Common-mode input voltage range		V_{CC} = ±5 V		±3	±3.2		V
			V_{CC} = ±15 V		±12.9	±13.2		
	Open loop transresistance		V_{CC} = ±5 V, R_L = 1 kΩ	V_O = ±2.5 V,		1.3		MΩ
			V_{CC} = ±15 V, R_L = 1 kΩ	V_O = ±7.5 V,		2.4		
CMRR	Common-mode rejection ratio		V_{CC} = ±5 V,	V_{CM} = ±2.5 V	62	70		dB
			V_{CC} = ±15 V,	V_{CM} = ±10 V	65	73		
PSRR	Power supply rejection ratio		V_{CC} = ±5 V	T_A = 25°C	65	76		dB
				T_A = full range	63			
			V_{CC} = ±15 V	T_A = 25°C	69	76		dB
				T_A = full range	67			
R_I	Input resistance	+Input				1.5		MΩ
		–Input				15		Ω
C_I	Differential input capacitance					7.5		pF
R_O	Output resistance		Open loop at 5 MHz			10		Ω
V_n	Input voltage noise		V_{CC} = ±5 V or ±15 V, G = 2	f = 10 kHz,		1.6		nV/√Hz
I_n	Input current noise	Positive (IN+)	V_{CC} = ±5 V or ±15 V, G = 2	f = 10 kHz,		13		pA/√Hz
		Negative (IN–)				16		

† Full range = 0°C to 70°C for the THS300xC and –40°C to 85°C for the THS300xI.

NOTE 1: Observe power dissipation ratings to keep the junction temperature below absolute maximum when the output is heavily loaded or shorted. See absolute maximum ratings section.

operating characteristics, T_A = 25°C, R_L = 150 Ω, R_F = 1 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate (see Note 2)	V_{CC} = ±5 V, $V_{O(PP)}$ = 4 V	G = –5		1700		V/μs
			G = 5		1300		
		V_{CC} = ±15 V, $V_{O(PP)}$ = 20 V	G = –5		6500		
			G = 5		6300		
t_s	Settling time to 0.1%	V_{CC} = ±15 V, 0 V to 10 V Step	Gain = –1,		40		ns
	Settling time to 0.1%	V_{CC} = ±5 V, 0 V to 2 V Step,	Gain = –1,		25		
THD	Total harmonic distortion	V_{CC} = ±15 V, f_C = 10 MHz,	$V_{O(PP)}$ = 2 V, G = 2		–80		dBc
A_D	Differential gain error	G = 2, 40 IRE modulation, ±100 IRE Ramp, NTSC and PAL	V_{CC} = ±5 V		0.015%		
			V_{CC} = ±15 V		0.01%		
θ_D	Differential phase error	G = 2, 40 IRE modulation, ±100 IRE Ramp, NTSC and PAL	V_{CC} = ±5 V		0.01°		
			V_{CC} = ±15 V		0.02°		
BW	Small signal bandwidth (–3 dB)	G = 1, R_F = 1 kΩ,	V_{CC} = ±5 V,		330		MHz
			V_{CC} = ±15 V,		420		MHz
		G = 2, R_F = 750 Ω,	V_{CC} = ±5 V		300		MHz
		G = 2, R_F = 680 Ω,	V_{CC} = ±15 V		385		
		G = 5, R_F = 560 Ω,	V_{CC} = ±15 V		350		
	Bandwidth for 0.1 dB flatness	G = 2, R_F = 750 Ω,	V_{CC} = ±5 V		85		MHz
		G = 2, R_F = 680 Ω,	V_{CC} = ±15 V		115		
	Full power bandwidth (see Note 3)	V_{CC} = ±5 V, $V_{O(PP)}$ = 4 V, R_L = 500 Ω	G = –5		65		MHz
			G = 5		62		MHz
		V_{CC} = ±15 V, $V_{O(PP)}$ = 20 V R_L = 500 Ω	G = –5		32		MHz
			G = 5		31		MHz
	Crosstalk (THS3002 only)				TBD		dB

NOTES: 2. Slew rate is measured from an output level range of 25% to 75%.
3. Full power bandwidth is defined as the frequency at which the output has 3% THD.

PARAMETER MEASUREMENT INFORMATION

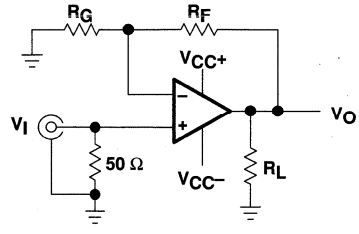


Figure 1. Test Circuit, Gain = 1 + (R_F/R_G)

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$\|V_O\|$	Output voltage swing	vs Free-air temperature	2
I_{CC}	Current supply	vs Free-air temperature	3
I_{IB}	Input bias current	vs Free-air temperature	4
V_{IO}	Input offset voltage	vs Free-air temperature	5
CMRR	Common-mode rejection ratio	vs Common-mode input voltage	6
		vs Common-mode input voltage	7
		vs Frequency	8
	Transresistance	vs Free-air temperature	9
	Closed-loop output impedance	vs Frequency	10
V_n	Voltage noise	vs Frequency	11
I_n	Current noise	vs Frequency	11
PSRR	Power supply rejection ratio	vs Frequency	12
		vs Free-air temperature	13
SR	Slew rate	vs Supply voltage	14
		vs Output step peak-to-peak	15, 16
	Normalized slew rate	vs Gain	17
	Harmonic distortion	vs Peak-to-peak output voltage swing	18, 19
		vs Frequency	20, 21
	Differential gain	vs Loading	22, 23
	Differential phase	vs Loading	24, 25
	Output amplitude	vs Frequency	26–30
	Normalized output response	vs Frequency	31–34
	Small and large signal frequency response		35, 36
	Small signal pulse response		37, 38
	Large signal pulse response		39 – 46

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE SWING
vs
FREE-AIR TEMPERATURE

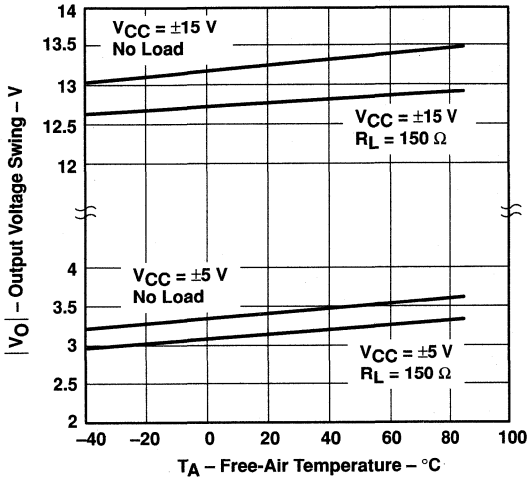


Figure 2

CURRENT SUPPLY
vs
FREE-AIR TEMPERATURE

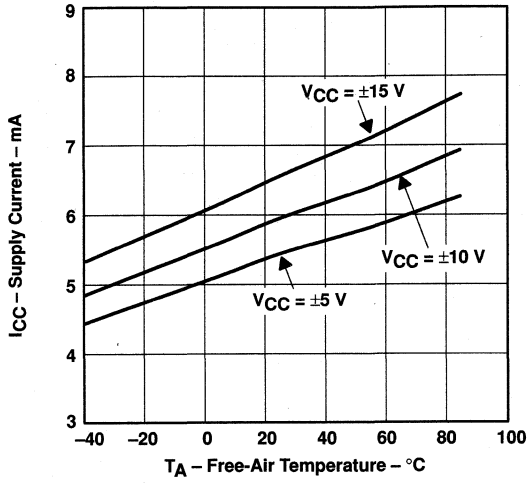


Figure 3

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

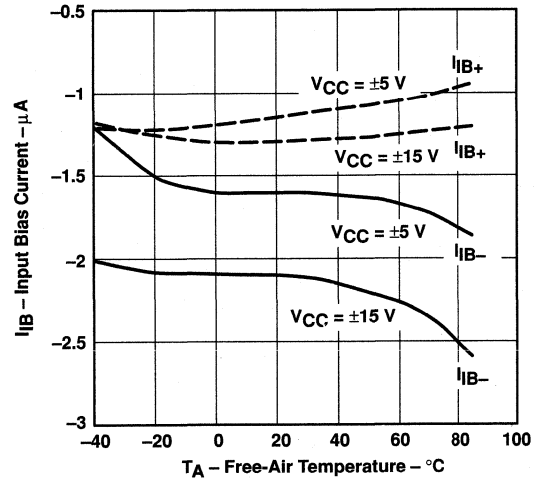


Figure 4

INPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

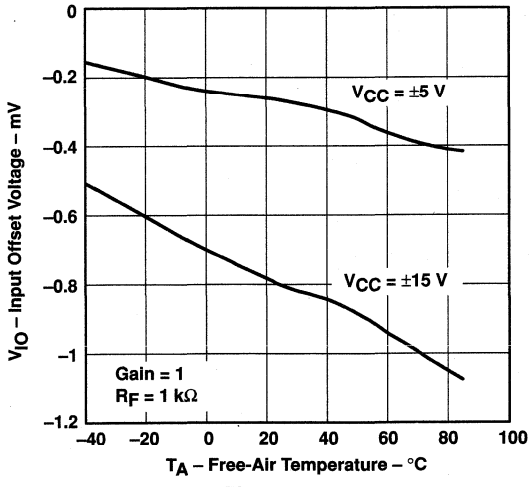


Figure 5

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
COMMON-MODE INPUT VOLTAGE

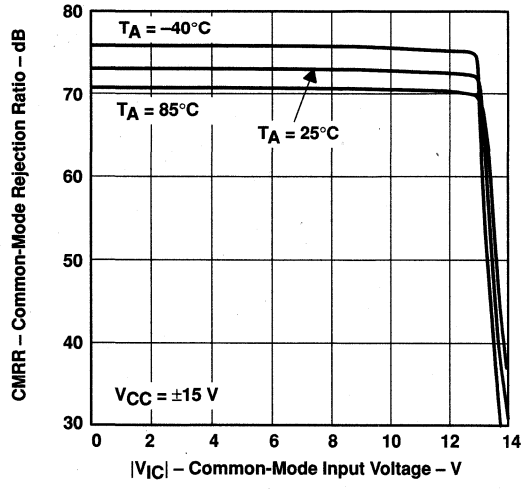


Figure 6

COMMON-MODE REJECTION RATIO
vs
COMMON-MODE INPUT VOLTAGE

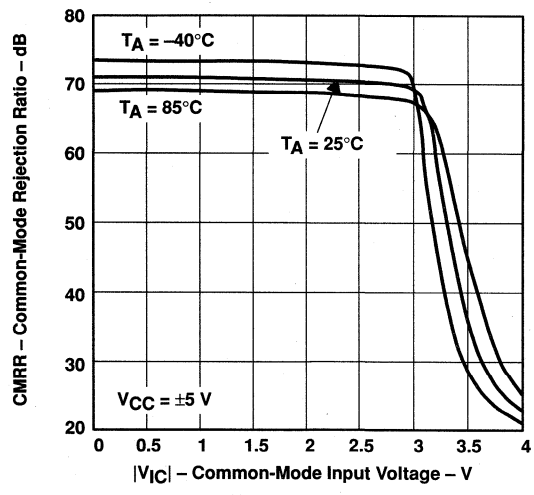


Figure 7

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

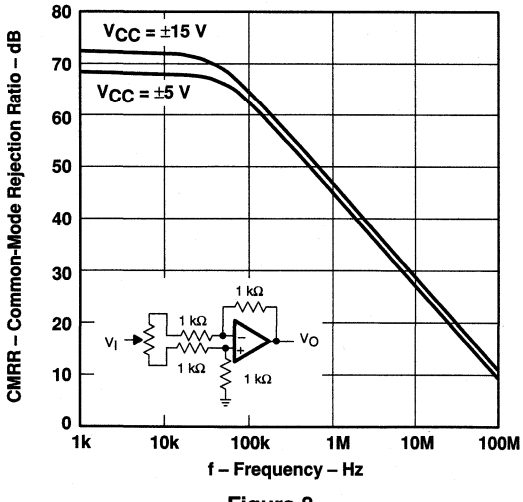


Figure 8

TRANSRESISTANCE
vs
FREE-AIR TEMPERATURE

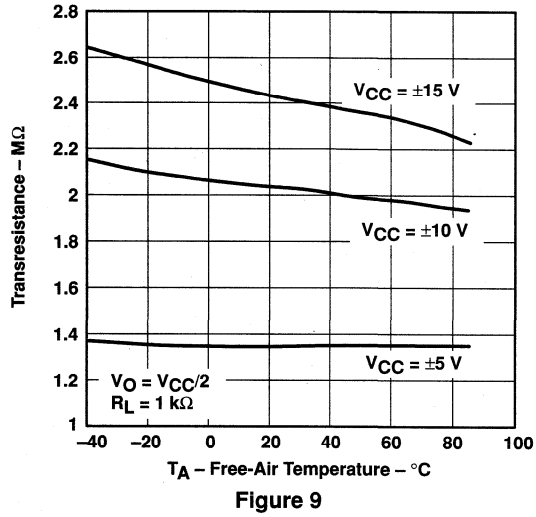


Figure 9

TYPICAL CHARACTERISTICS

CLOSED-LOOP OUTPUT IMPEDANCE
vs
FREQUENCY

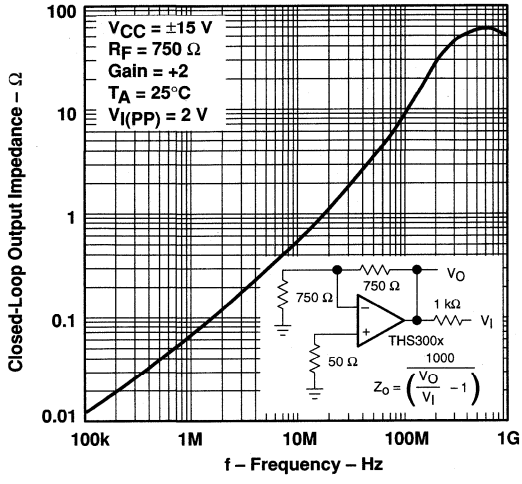


Figure 10

VOLTAGE NOISE AND CURRENT NOISE
vs
FREQUENCY

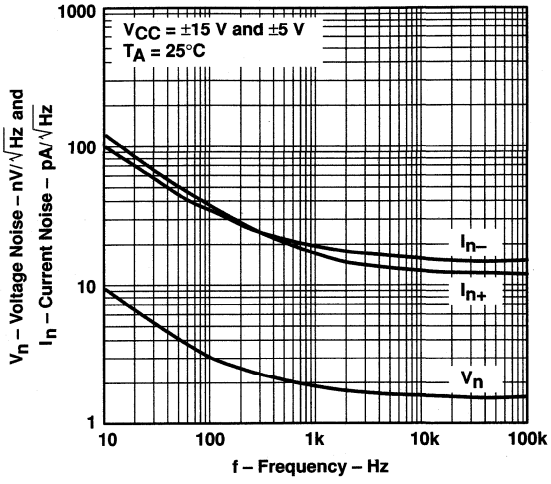


Figure 11

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

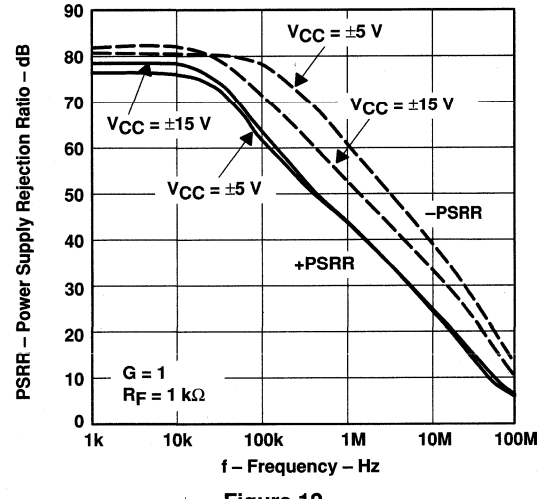


Figure 12

POWER SUPPLY REJECTION RATIO
vs
FREE-AIR TEMPERATURE

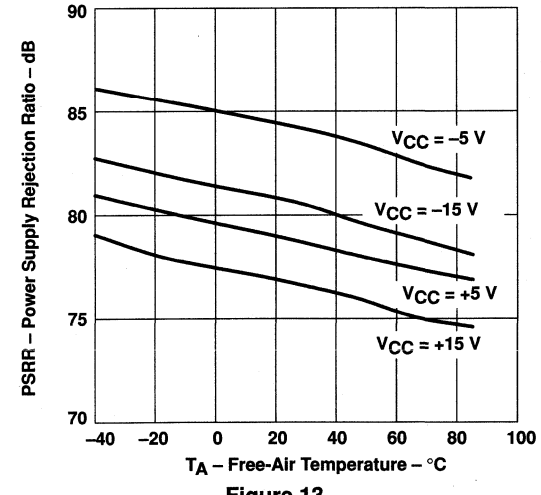


Figure 13

TYPICAL CHARACTERISTICS

SLEW RATE vs SUPPLY VOLTAGE

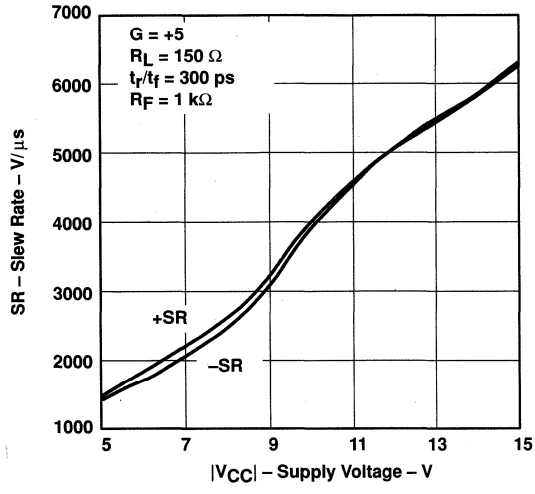


Figure 14

SLEW RATE vs OUTPUT STEP

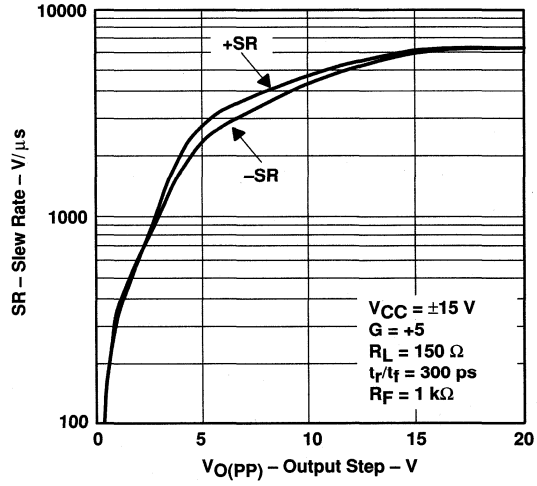


Figure 15

SLEW RATE vs OUTPUT STEP

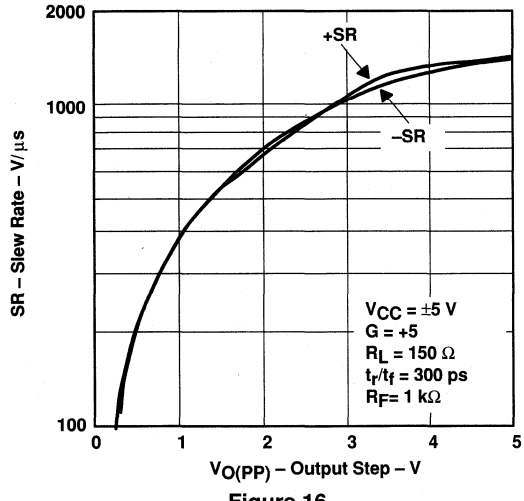


Figure 16

NORMALIZED SLEW RATE vs GAIN

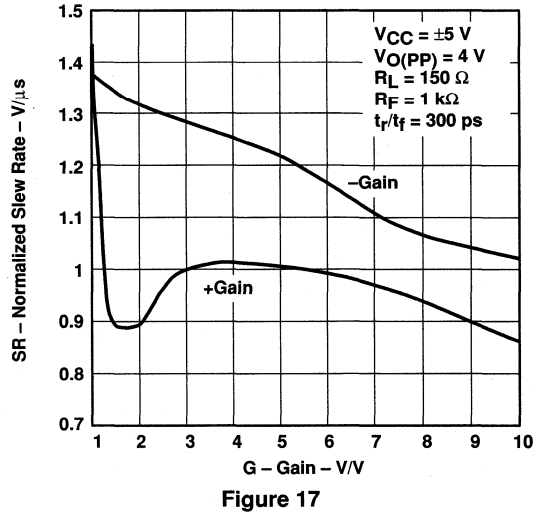


Figure 17

TYPICAL CHARACTERISTICS

HARMONIC DISTORTION
vs
PEAK-TO-PEAK OUTPUT VOLTAGE SWING

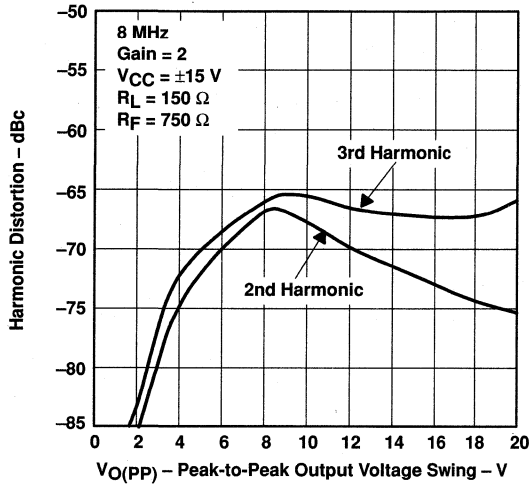


Figure 18

HARMONIC DISTORTION
vs
PEAK-TO-PEAK OUTPUT VOLTAGE SWING

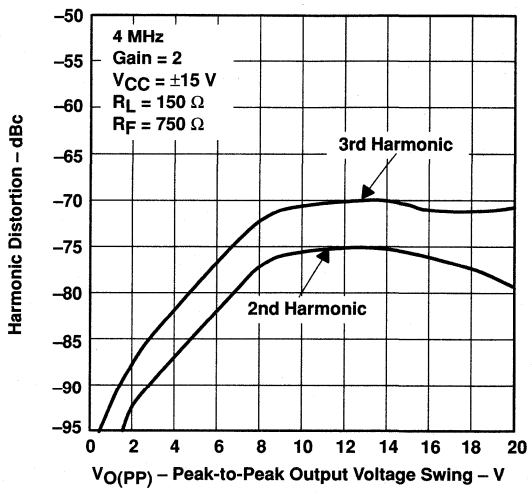


Figure 19

HARMONIC DISTORTION
vs
FREQUENCY

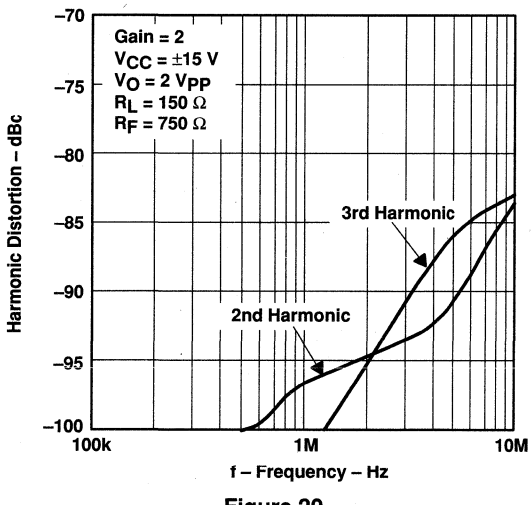


Figure 20

HARMONIC DISTORTION
vs
FREQUENCY

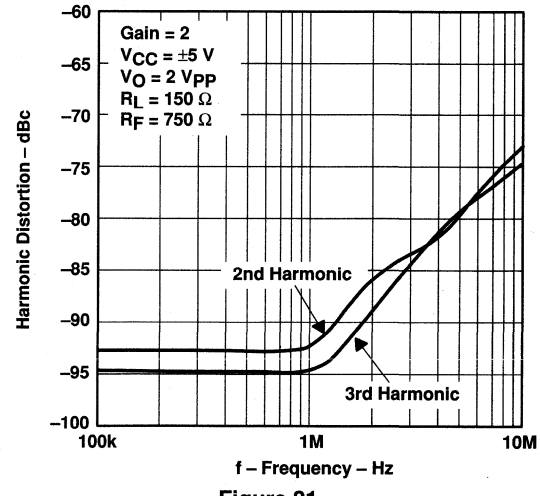


Figure 21

TYPICAL CHARACTERISTICS

DIFFERENTIAL GAIN
vs
LOADING

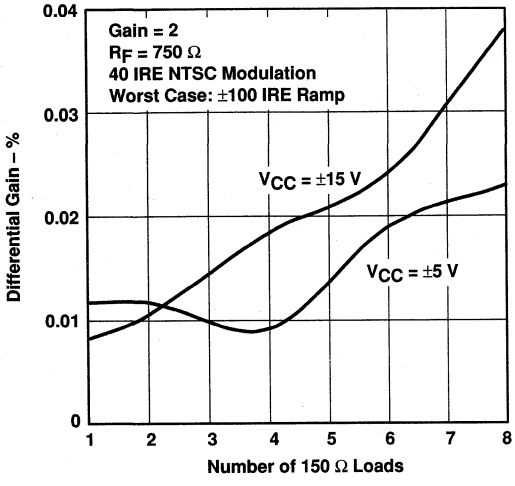


Figure 22

DIFFERENTIAL GAIN
vs
LOADING

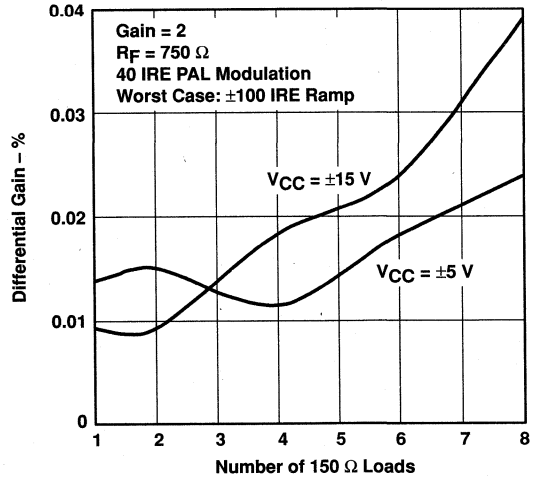


Figure 23

DIFFERENTIAL PHASE
vs
LOADING

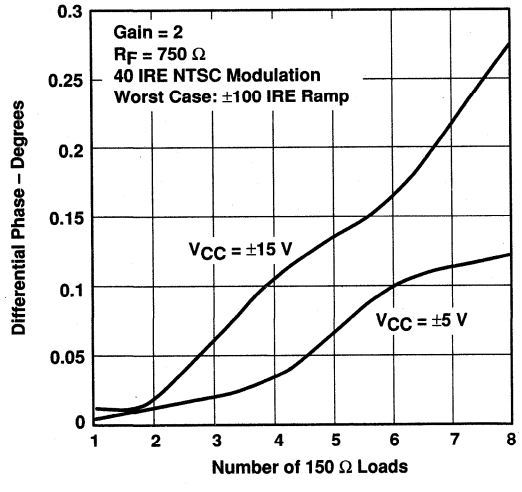


Figure 24

DIFFERENTIAL PHASE
vs
LOADING

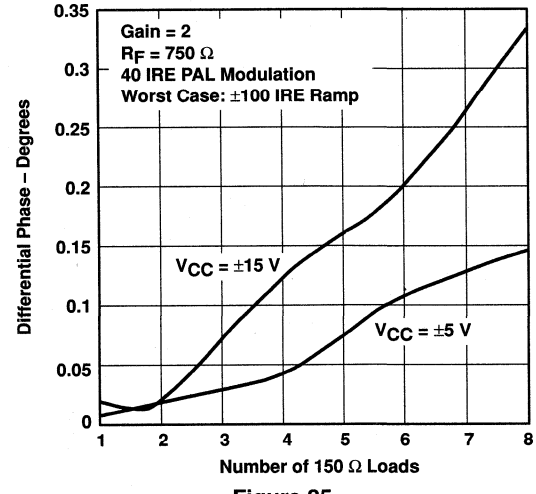


Figure 25

TYPICAL CHARACTERISTICS

OUTPUT AMPLITUDE
vs
FREQUENCY

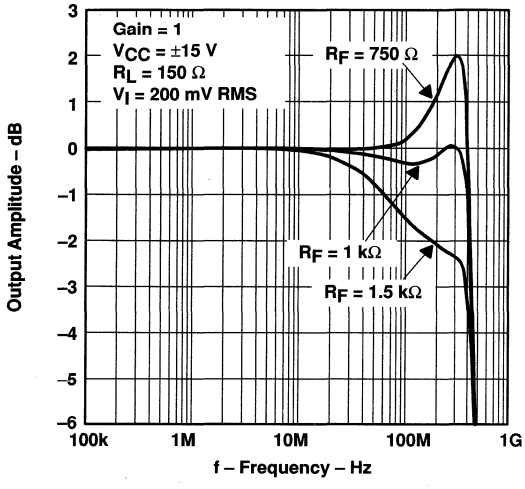


Figure 26

OUTPUT AMPLITUDE
vs
FREQUENCY

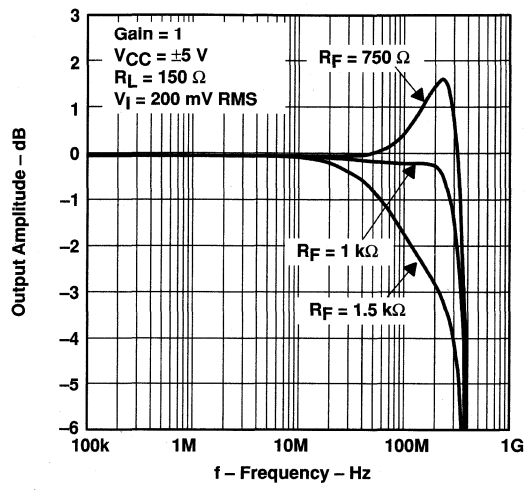


Figure 27

OUTPUT AMPLITUDE
vs
FREQUENCY

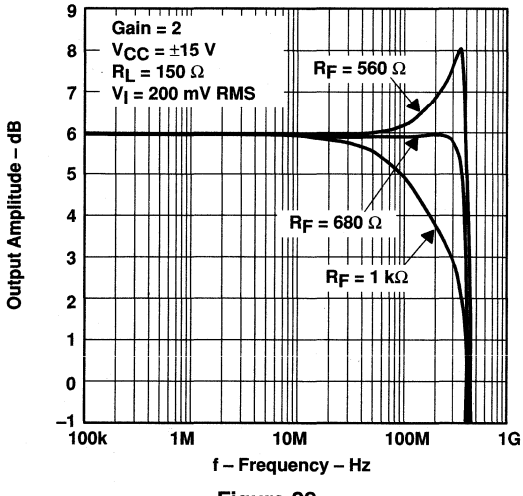


Figure 28

OUTPUT AMPLITUDE
vs
FREQUENCY

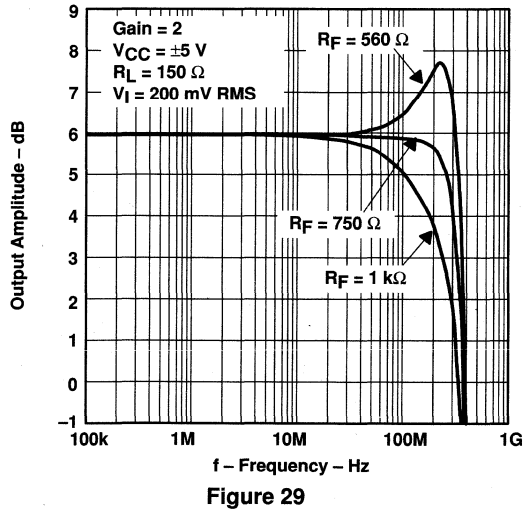


Figure 29

TYPICAL CHARACTERISTICS

OUTPUT AMPLITUDE vs FREQUENCY

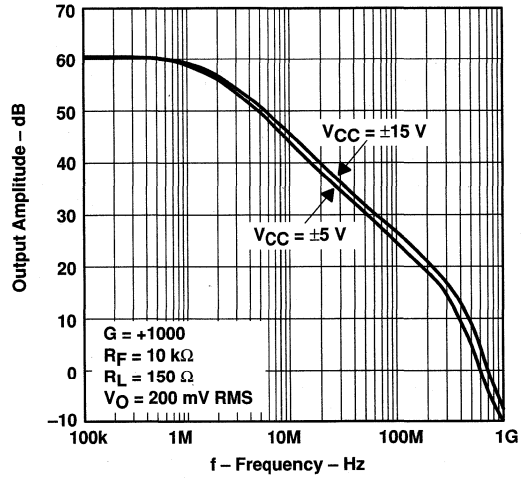


Figure 30

NORMALIZED OUTPUT RESPONSE vs FREQUENCY

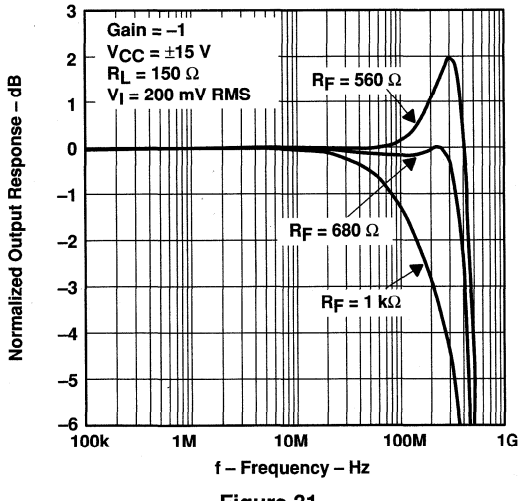


Figure 31

NORMALIZED OUTPUT RESPONSE vs FREQUENCY

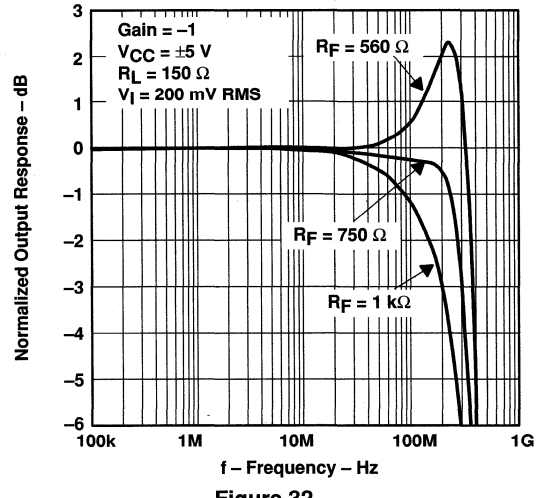


Figure 32

TYPICAL CHARACTERISTICS

NORMALIZED OUTPUT RESPONSE
vs
FREQUENCY

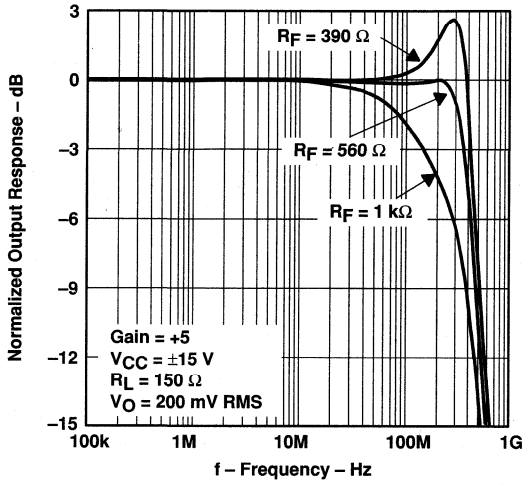


Figure 33

NORMALIZED OUTPUT RESPONSE
vs
FREQUENCY

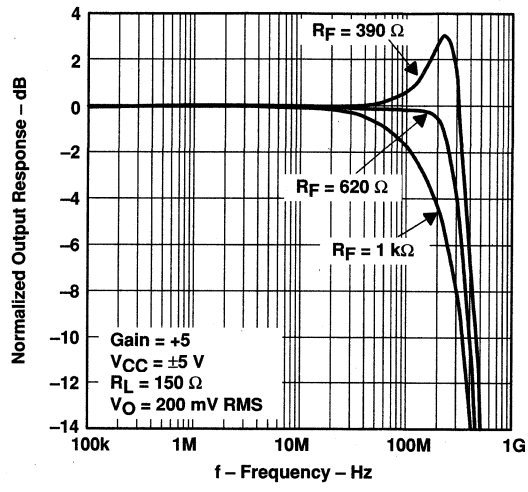


Figure 34

SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

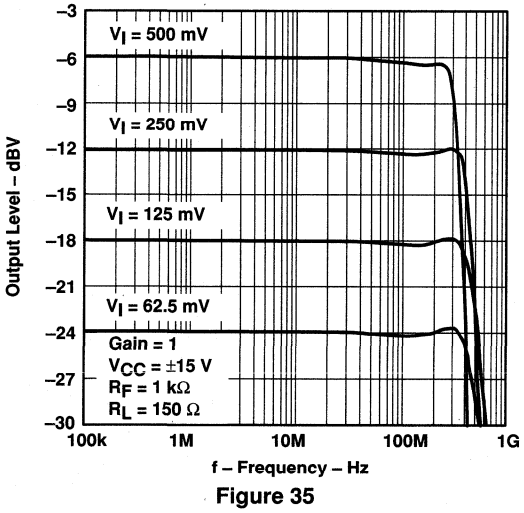


Figure 35

SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

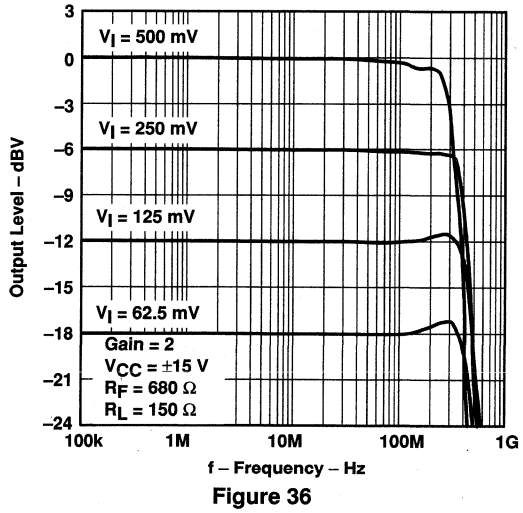


Figure 36

TYPICAL CHARACTERISTICS

SMALL SIGNAL PULSE RESPONSE

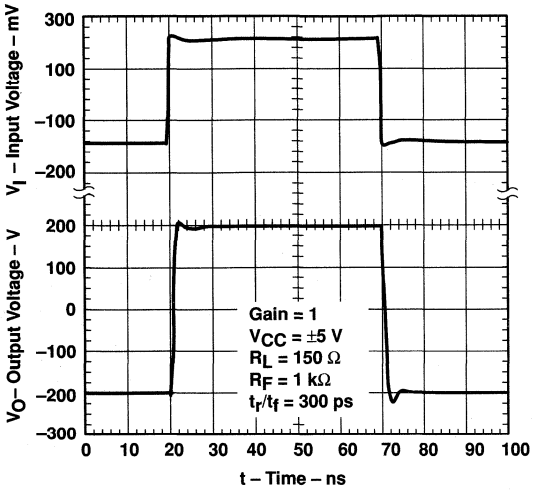


Figure 37

SMALL SIGNAL PULSE RESPONSE

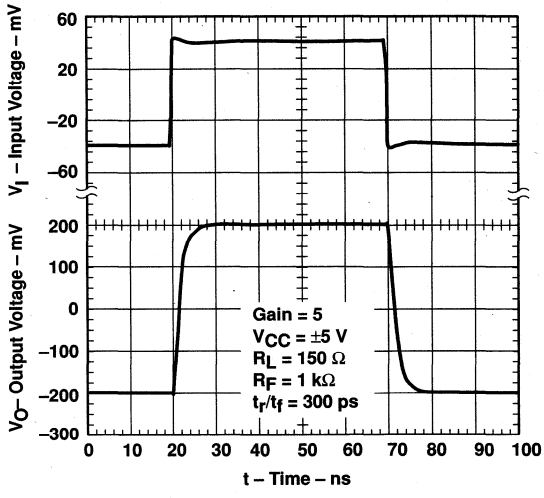


Figure 38

LARGE SIGNAL PULSE RESPONSE

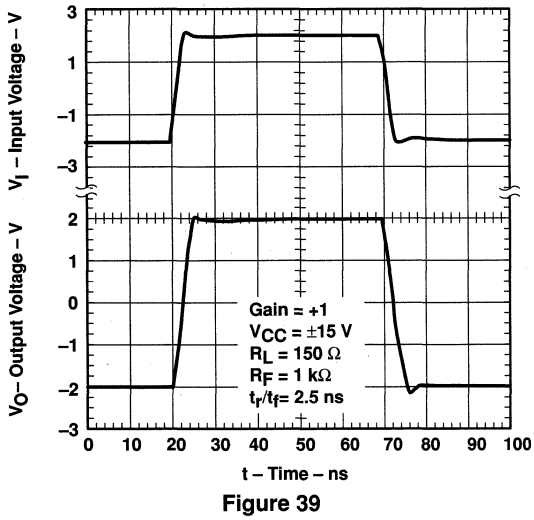


Figure 39

LARGE SIGNAL PULSE RESPONSE

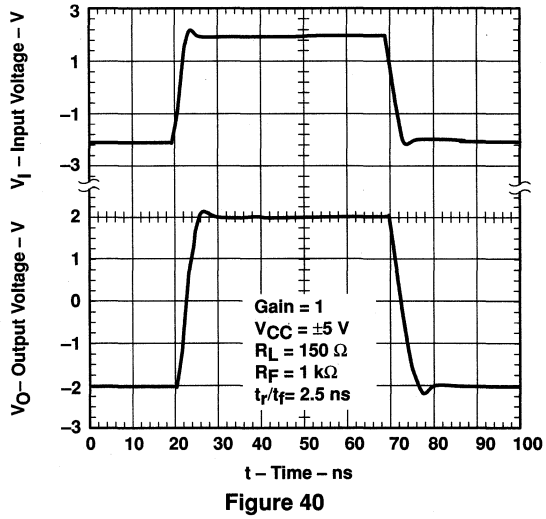


Figure 40

TYPICAL CHARACTERISTICS

LARGE SIGNAL PULSE RESPONSE

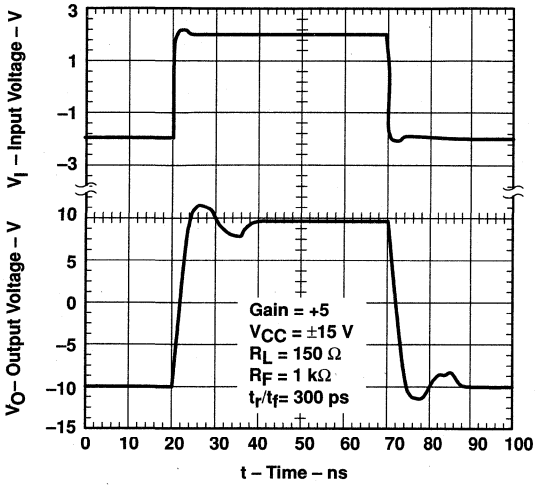


Figure 41

LARGE SIGNAL PULSE RESPONSE

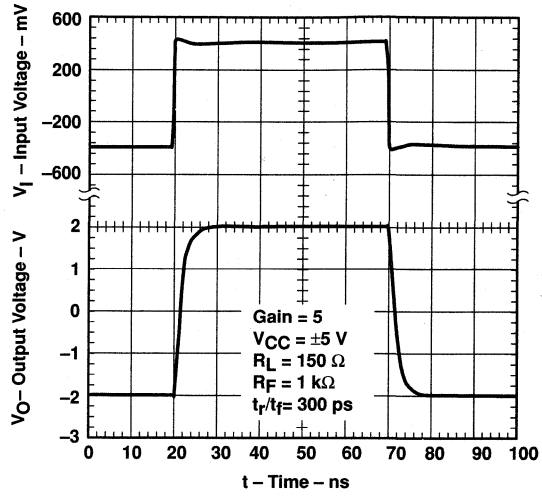


Figure 42

LARGE SIGNAL PULSE RESPONSE

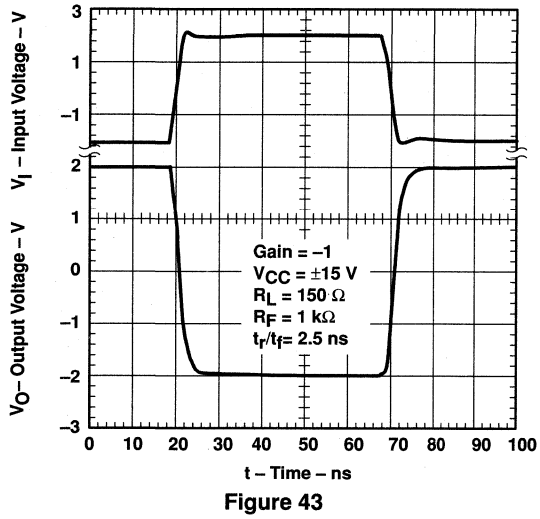


Figure 43

LARGE SIGNAL PULSE RESPONSE

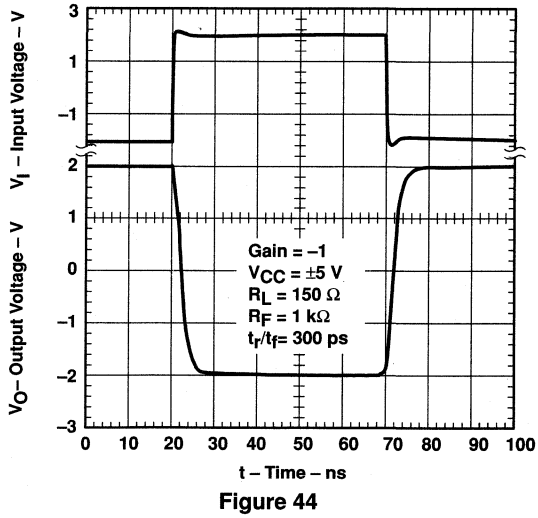


Figure 44

TYPICAL CHARACTERISTICS

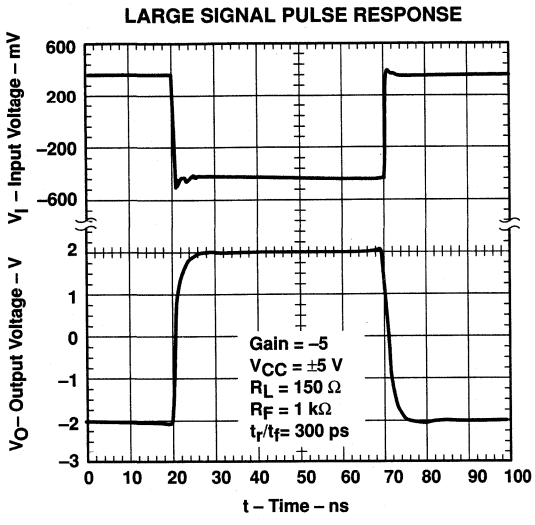


Figure 45

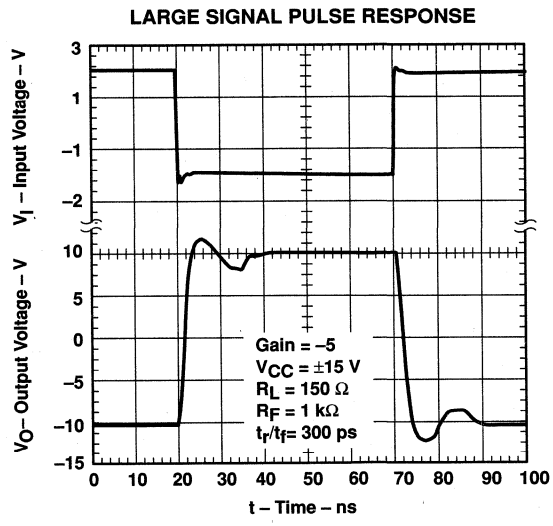


Figure 46

APPLICATION INFORMATION

theory of operation

The THS300x is a high-speed, operational amplifier configured in a voltage-feedback architecture. The device is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This configuration implements an exceptionally high-performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 47.

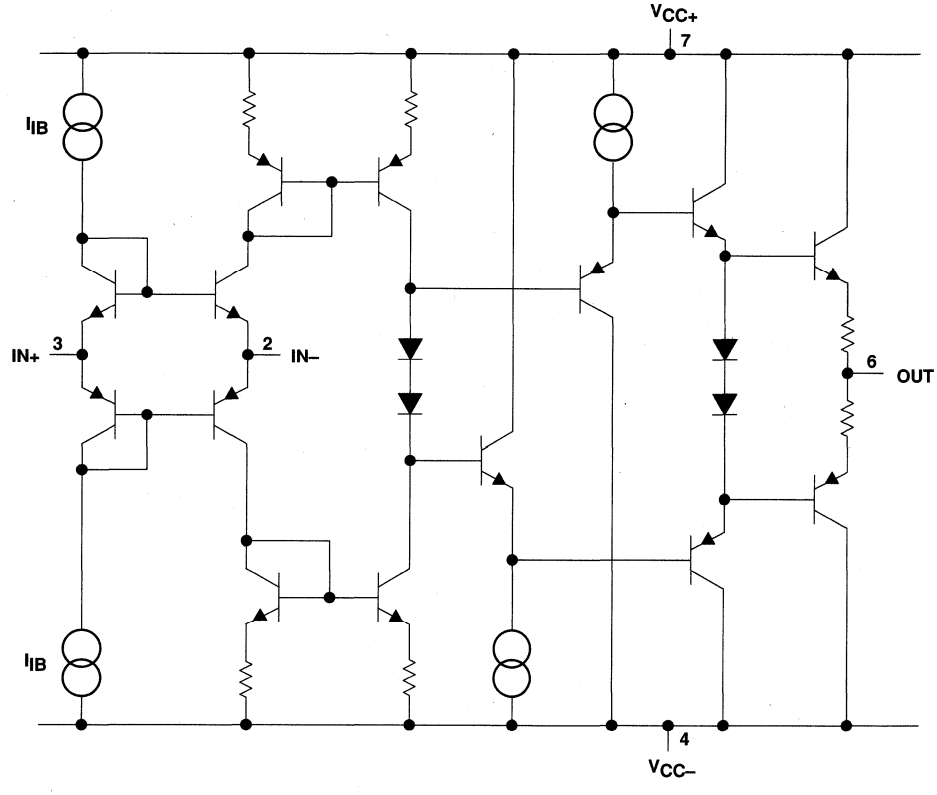


Figure 47. Simplified Schematic

APPLICATION INFORMATION

recommended feedback and gain resistor values

The THS300x is fabricated using Texas Instruments 30-V complementary bipolar process, HVBiCOM. This process provides the excellent isolation and extremely high slew rates that result in superior distortion characteristics.

As with all current-feedback amplifiers, the bandwidth of the THS300x is an inversely proportional function of the value of the feedback resistor (see Figures 26 to 34). The recommended resistors for the optimum frequency response are shown in Table 1. These should be used as a starting point and once optimum values are found, 1% tolerance resistors should be used to maintain frequency response characteristics. For most applications, a feedback resistor value of 1 kΩ is recommended – a good compromise between bandwidth and phase margin that yields a very stable amplifier.

Consistent with current-feedback amplifiers, increasing the gain is best accomplished by changing the gain resistor, not the feedback resistor. This is because the bandwidth of the amplifier is dominated by the feedback resistor value and internal dominant-pole capacitor. The ability to control the amplifier gain independent of the bandwidth constitutes a major advantage of current-feedback amplifiers over conventional voltage-feedback amplifiers. Therefore, once a frequency response is found suitable to a particular application, adjust the value of the gain resistor to increase or decrease the overall amplifier gain.

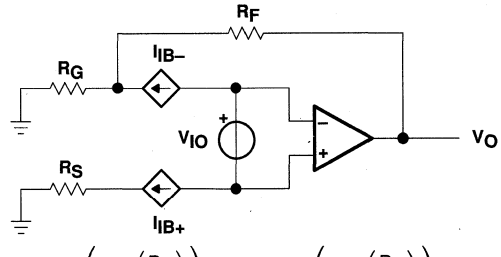
Finally, it is important to realize the effects of the feedback resistance on distortion. Increasing the resistance decreases the loop gain and increases the distortion. It is also important to know that decreasing load impedance increases total harmonic distortion (THD). Typically, the third-order harmonic distortion increases more than the second-order harmonic distortion.

Table 1. Recommended Resistor Values for Optimum Frequency Response

GAIN	R_F for V_{CC} = ±15 V	R_F for V_{CC} = ±5 V
1	1 kΩ	1 kΩ
2, –1	680 Ω	750 Ω
–2	620 Ω	620 Ω
5	560 Ω	620 Ω

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\ R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\ R_F$$

Figure 48. Output Offset Voltage Model

APPLICATION INFORMATION

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true for amplifying small signals coming over a transmission line or an antenna. The noise model for current-feedback amplifiers (CFB) is the same as for voltage feedback amplifiers (VFB). The only difference between the two is that CFB amplifiers generally specify different current-noise parameters for each input, while VFB amplifiers usually only specify one noise-current parameter. The noise model is shown in Figure 49. This model includes all of the noise sources as follows:

- e_n = amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = noninverting current noise (pA/$\sqrt{Hz}$)
- IN– = inverting current noise (pA/$\sqrt{Hz}$)
- e_{Rx} = thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR_x)

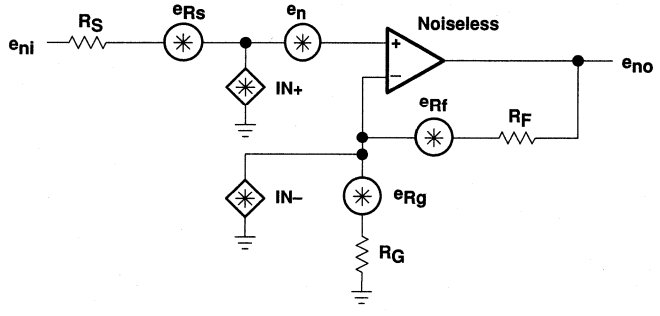


Figure 49. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN+ \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\ kTR_S + 4\ kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\ A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)}$$

APPLICATION INFORMATION

noise calculations and noise figure (continued)

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier.

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^2}{e_{Rs2}}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\ kTR_S}\right]$$

The Figure 50 shows the noise figure graph for the THS300x.

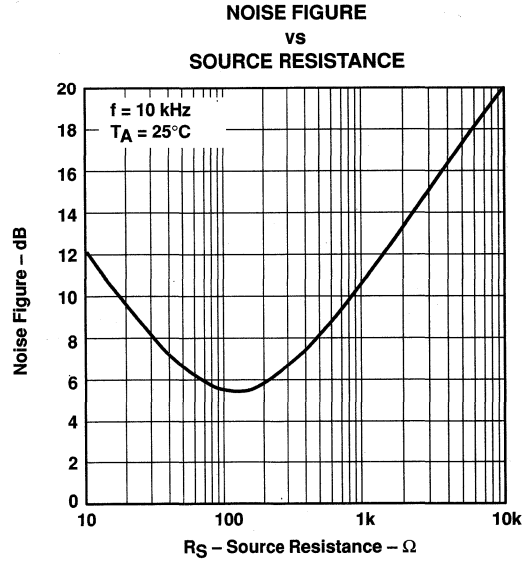


Figure 50. Noise Figure vs Source Resistance

APPLICATION INFORMATION

slew rate

The slew rate performance of a current-feedback amplifier, like the THS300x, is affected by many different factors. Some of these factors are external to the device, such as amplifier configuration and PCB parasitics, and others are internal to the device, such as available currents and node capacitance. Understanding some of these factors should help the PCB designer arrive at a more optimum circuit with fewer problems.

Whether the THS300x is used in an inverting amplifier configuration or a noninverting configuration can impact the output slew rate. As can be seen from the specification tables as well as some of the figures in this data sheet, slew-rate performance in the inverting configuration is faster than in the noninverting configuration. This is because in the inverting configuration the input terminals of the amplifier are at a virtual ground and do not significantly change voltage as the input changes. Consequently, the time to charge any capacitance on these input nodes is less than for the noninverting configuration, where the input nodes actually do change in voltage an amount equal to the size of the input step. In addition, any PCB parasitic capacitance on the input nodes degrades the slew rate further simply because there is more capacitance to charge. Also, if the supply voltage (V_{CC}) to the amplifier is reduced, slew rate decreases because there is less current available within the amplifier to charge the capacitance on the input nodes as well as other internal nodes.

Internally, the THS300x has other factors that impact the slew rate. The amplifier's behavior during the slew-rate transition varies slightly depending upon the rise time of the input. This is because of the way the input stage handles faster and faster input edges. Slew rates (as measured at the amplifier output) of less than about 1500 V/μs are processed by the input stage in a very linear fashion. Consequently, the output waveform smoothly transitions between initial and final voltage levels. This is shown in Figure 51. For slew rates greater than 1500 V/μs, additional slew-enhancing transistors present in the input stage begin to turn on to support these faster signals. The result is an amplifier with extremely fast slew-rate capabilities. Figures 41 and 52 show waveforms for these faster slew rates. The additional aberrations present in the output waveform with these faster-slewing input signals are due to the brief saturation of the internal current mirrors. This phenomenon, which typically lasts less than 20 ns, is considered normal operation and is not detrimental to the device in any way. If for any reason this type of response is not desired, then increasing the feedback resistor or slowing down the input-signal slew rate reduces the effect.

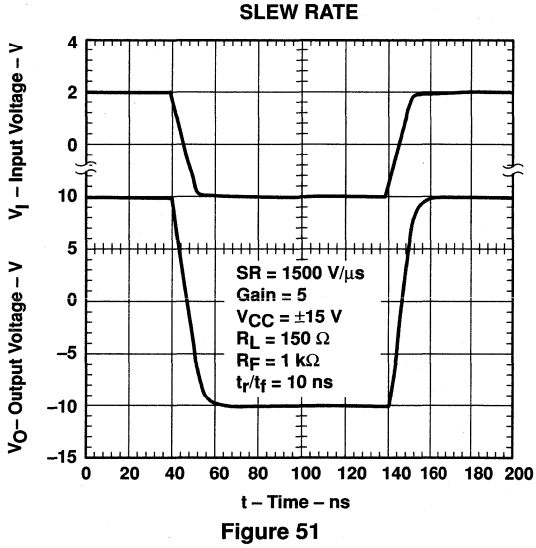


Figure 51

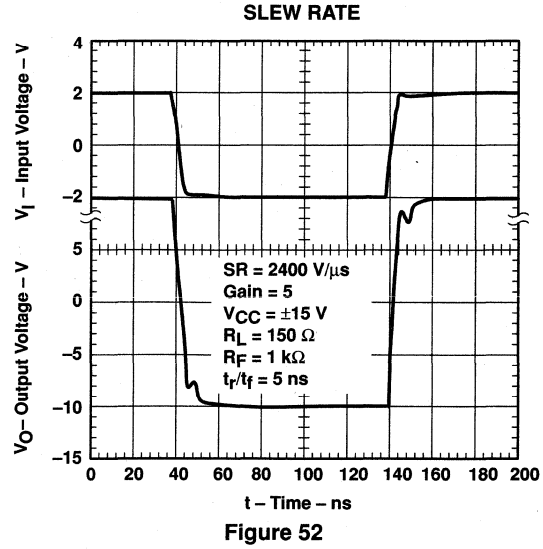


Figure 52

APPLICATION INFORMATION

driving a capacitive load

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS300x has been internally compensated to maximize its bandwidth and slew-rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 53. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

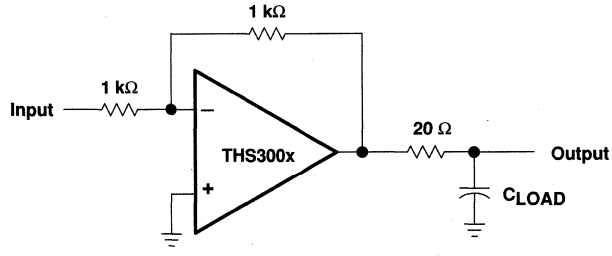


Figure 53. Driving a Capacitive Load

PCB design considerations

Proper PCB design techniques in two areas are important to assure proper operation of the THS300x. These areas are high-speed layout techniques and thermal-management techniques. Because the THS300x is a high-speed part, the following guidelines are recommended.

- Ground plane – It is essential that a ground plane be used on the board to provide all components with a low inductive ground connection. Although a ground connection directly to a terminal of the THS300x is not necessarily required, it is recommended that the thermal pad of the package be tied to ground. This serves two functions: it provides a low inductive ground to the device substrate to minimize internal crosstalk, and it provides the path for heat removal.
- Input stray capacitance – To minimize potential problems with amplifier oscillation, the capacitance at the inverting input of the amplifiers must be kept to a minimum. To do this, PCB trace runs to the inverting input must be as short as possible, the ground plane must be removed under any etch runs connected to the inverting input, and external components should be placed as close as possible to the inverting input. This is especially true in the noninverting configuration. An example of this can be seen in Figure 54, which shows what happens when a 1-pF capacitor is added to the inverting input terminal. The bandwidth increases at the expense of peaking. This is because some of the error current is flowing through the stray capacitor instead of the inverting node of the amplifier. Although, while the device is in the inverting mode, stray capacitance at the inverting input has a minimal effect. This is because the inverting node is at a *virtual ground* and the voltage does not fluctuate nearly as much as in the noninverting configuration. This can be seen in Figure 55, where a 10-pF capacitor adds only 0.35 dB of peaking. In general, as the gain of the system increases, the output peaking due to this capacitor decreases. While this can initially look like a faster and better system, overshoot and ringing are more likely to occur under fast transient conditions. So proper analysis of adding a capacitor to the inverting input node should be performed for stable operation.

APPLICATION INFORMATION

PCB design considerations (continued)

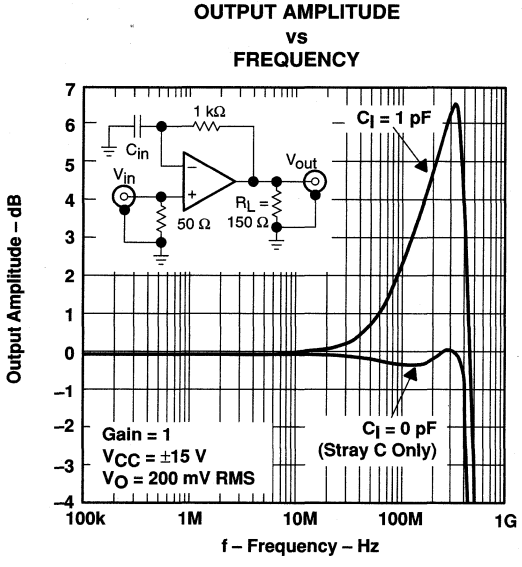


Figure 54

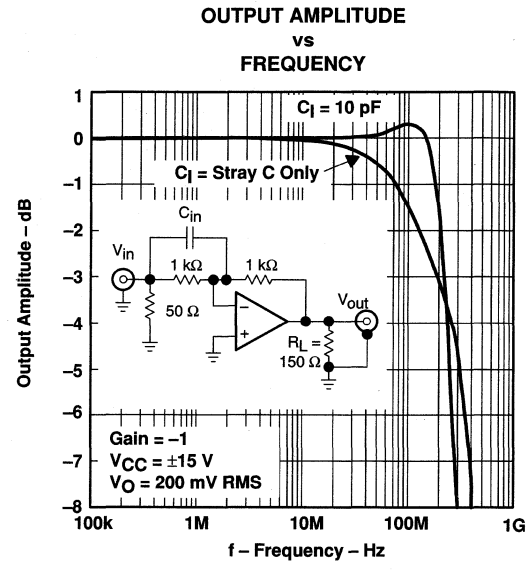


Figure 55

- Proper power-supply decoupling – Use a minimum 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting etch makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminal and the ceramic capacitors.

thermal information

The THS300x incorporates output-current-limiting protection. Should the output become shorted to ground, the output current is automatically limited to the value given in the data sheet. While this protects the output against excessive current, the device internal power dissipation increases due to the high current and large voltage drop across the output transistors. Continuous output shorts are not recommended and could damage the device. Additionally, connection of the amplifier output to one of the supply rails ($\pm V_{CC}$) is not recommended. Failure of the device is possible under this condition and should be avoided. But, the THS300x does not incorporate thermal-shutdown protection. Because of this, special attention must be paid to the device's power dissipation or failure may result.

APPLICATION INFORMATION

thermal information (continued)

The thermal coefficient θ_{JA} is approximately 169°C/W for the SOIC 8-pin D package. For a given θ_{JA}, the maximum power dissipation, shown in Figure 56, is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of THS300x (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
θ_{JA} = Thermal coefficient from die junction to ambient air (°C/W)

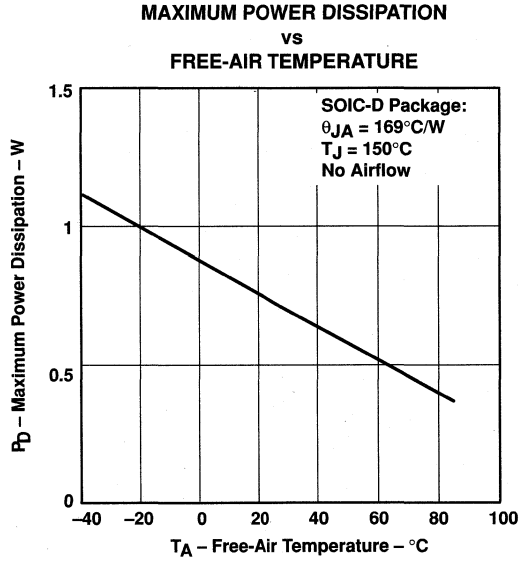
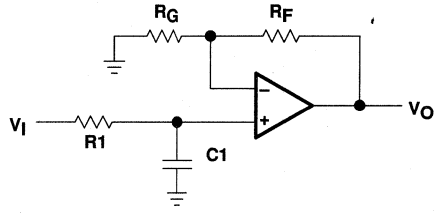


Figure 56. Maximum Power Dissipation vs Free-Air Temperature

APPLICATION INFORMATION

general configurations

A common error for the first-time CFB user is the creation of a unity gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration will oscillate and is **not** recommended. The THS300x, like all CFB amplifiers, **must** have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a very low impedance. This results in an unstable amplifier and should not be considered when using a current-feedback amplifier. Because of this, integrators and simple low-pass filters, which are easily implemented on a VFB amplifier, have to be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see Figure 57).

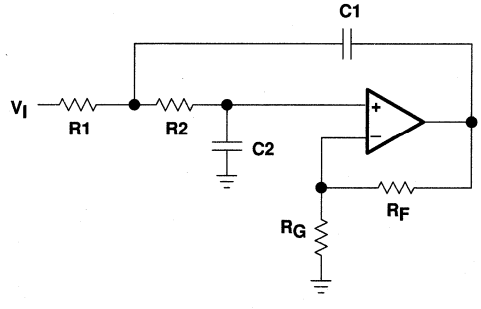


$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 57. Single-Pole Low-Pass Filter

If a multiple-pole filter is required, the use of a Sallen-Key filter can work very well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew-rates and high bandwidths, CFB amplifiers can create very accurate signals and help minimize distortion. An example is shown in Figure 58.



R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

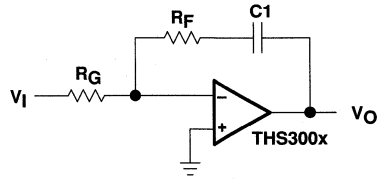
$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 58. 2-Pole Low-Pass Sallen-Key Filter

There are two simple ways to create an integrator with a CFB amplifier. The first, shown in Figure 59, adds a resistor in series with the capacitor. This is acceptable because at high frequencies, the resistor is dominant and the feedback impedance never drops below the resistor value. The second, shown in Figure 60, uses positive feedback to create the integration. Caution is advised because oscillations can occur due to the positive feedback.

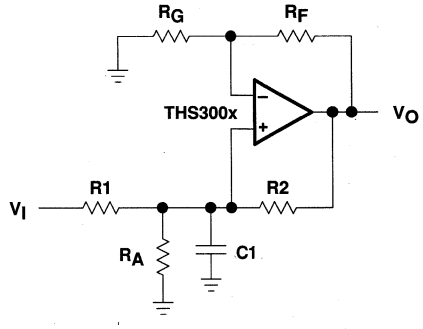
APPLICATION INFORMATION

general configurations (continued)



$$\frac{V_O}{V_I} = \left(\frac{R_F}{R_G}\right)\left[\frac{S + \frac{1}{R_F C1}}{S}\right]$$

Figure 59. Inverting CFB Integrator



For Stable Operation:

$$\frac{R2}{R1 \parallel R_A} \geq \frac{R_F}{R_G}$$

$$V_O \cong V_I \left(1 + \frac{\frac{R_F}{R_G}}{sR1C1}\right)$$

Figure 60. Noninverting CFB Integrator

The THS300x may also be employed as a very good video distribution amplifier. One characteristic of distribution amplifiers is the fact that the differential phase (DP) and the differential gain (DG) are compromised as the number of lines increases and the closed-loop gain increases (see Figures 22 to 25 for more information). Be sure to use termination resistors throughout the distribution system to minimize reflections and capacitive loading.

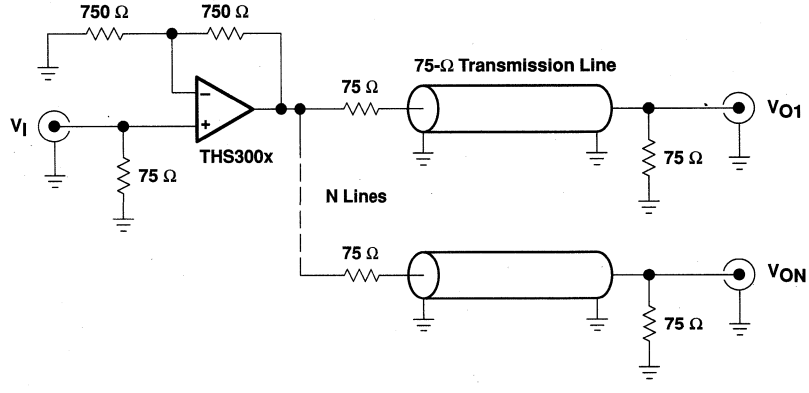


Figure 61. Video Distribution Amplifier Application

APPLICATION INFORMATION

evaluation board

Evaluation boards are available for the THS3001 (literature #SLOP130) and the THS3002 (literature #SLOP241). The boards have been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. Schematics of the evaluation boards are shown in Figures 62 and 63. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. To order the evaluation board contact your local TI sales office or distributor. For more detailed information, refer to the *THS3001 EVM User's Manual* (literature #SLOV021) or the *THS3002 EVM User's Guide* (literature #SLOVxxx). To order the evaluation board, contact your local TI sales office or distributor.

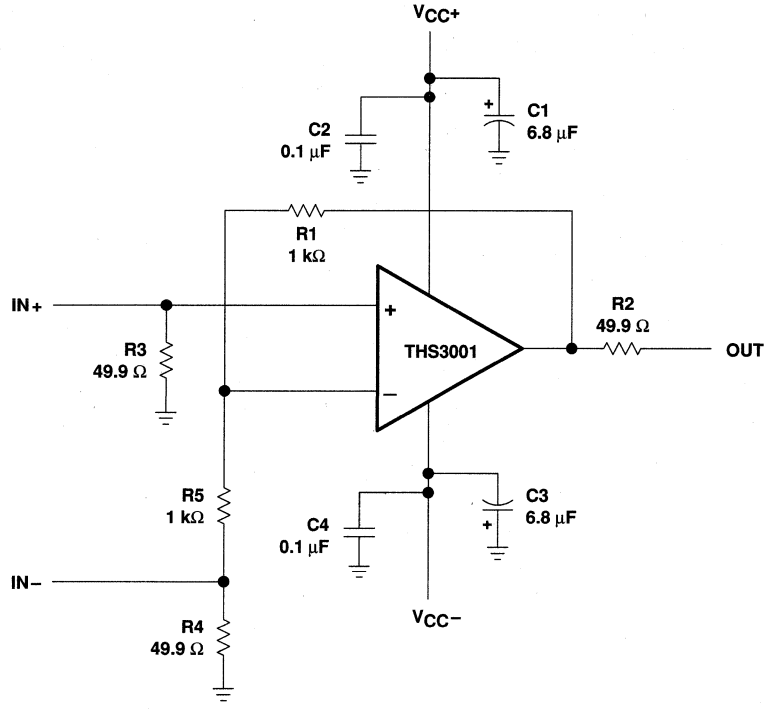


Figure 62. THS3001 Evaluation Board Schematic

APPLICATION INFORMATION

evaluation board (continued)

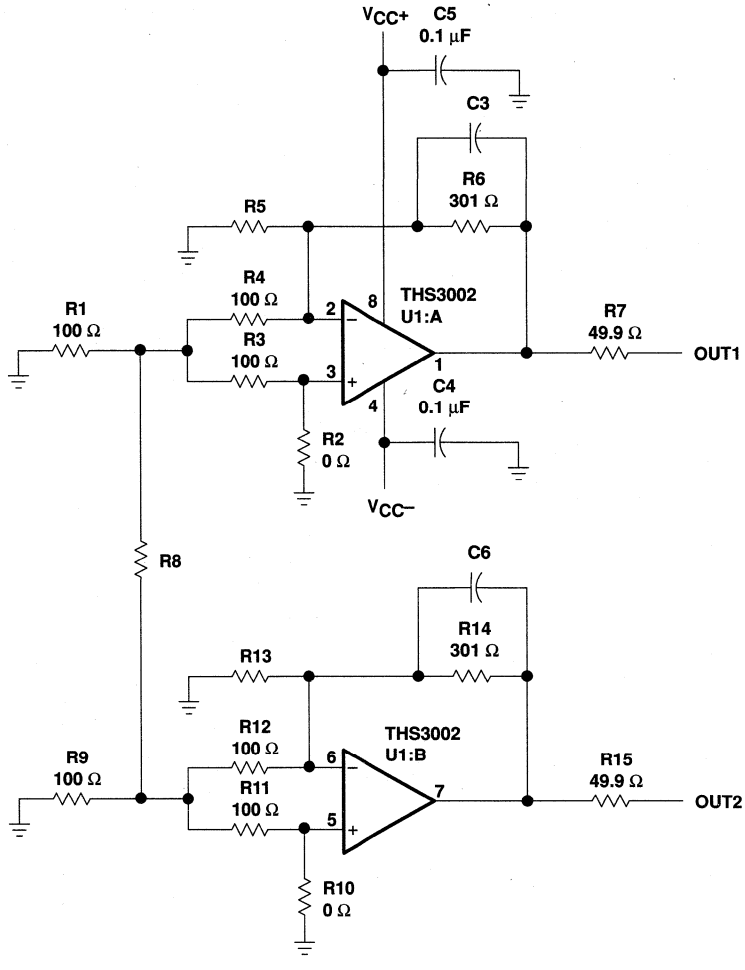
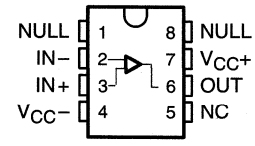


Figure 63. THS3002 Evaluation Board Schematic

SLOS206A– DECEMBER 1997 – REVISED MARCH 1999

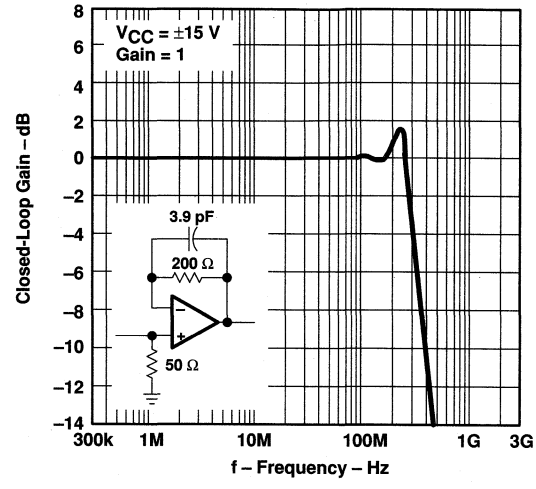
- **Very High Speed**
  - **270 MHz Bandwidth (Gain = 1, –3 dB)**
  - **400 V/μsec Slew Rate**
  - **40-ns Settling Time (0.1%)**
- **High Output Drive, I_O = 100 mA**
- **Excellent Video Performance**
  - **60 MHz Bandwidth (0.1 dB, G = 1)**
  - **0.04% Differential Gain**
  - **0.15° Differential Phase**
- **Very Low Distortion**
  - **THD = –72 dBc at f = 1 MHz**
- **Wide Range of Power Supplies**
  V_{CC} = ± 2.5 V to ± 15 V,
  I_{CC} = 7.5 mA
- **Evaluation Module Available**

D PACKAGE
(TOP VIEW)



NC – No internal connection

CLOSED-LOOP GAIN
vs
FREQUENCY



description

The THS4001 is a very high-performance, voltage-feedback operational amplifier especially suited for a wide range of video applications. The device is specified to operate over a wide range of supply voltages from ± 15 V to ± 2.5 V. With a bandwidth of 270 MHz, a slew rate of over 400 V/μs, and settling times of less than 30 ns, the THS4001 offers the unique combination of high performance in an easy to use voltage feedback configuration over a wide range of power supply voltages.

The THS4001 is stable at all gains for both inverting and noninverting configurations. It has a high output drive capability of 100 mA and draws only 7.5 mA of quiescent current. Excellent professional video results can be obtained with the differential gain/phase performance of 0.04%/0.15° and 0.1 dB gain flatness to 60 MHz. For applications requiring low distortion, the THS4001 is ideally suited with total harmonic distortion of –72 dBc at f = 1 MHz.

HIGH-SPEED AMPLIFIER FAMILY

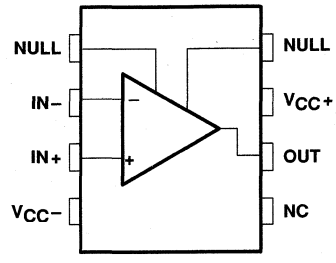
DEVICE	ARCH.		SUPPLY VOLTAGE			BW (MHz)	SR (V/μs)	THD f = 1 MHz (dB)	t_s 0.1% (ns)	DIFF. GAIN	DIFF. PHASE	V_n (nV/√Hz)
	VFB	CFB	5 V	±5 V	±15 V							
THS3001		•		•	•	420	6500	–96	40	0.01%	0.02°	1.6
THS4001	•		•	•	•	270	400	–72	40	0.04%	0.15°	12.5
THS4031/32	•			•	•	100	100	–72	60	0.02%	0.03°	1.6
THS4061/62	•			•	•	180	400	–72	40	0.02%	0.02°	14.5

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	SMALL OUTLINE† (D)	EVALUATION MODULE
0°C to 70°C	THS4001CD	THS4001EVM
–40°C to 85°C	THS4001ID	—

† The D packages are available taped and reeled. Add an R suffix to the device type (i.e., THS4001CDR).

symbol



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC-} to V_{CC+} . . . . . 33 V
Input voltage, V_I . . . . . $\pm V_{CC}$
Output current, I_O . . . . . 175 mA
Differential input voltage, V_{ID} . . . . . ±4 V
Continuous total power dissipation . . . . . See Dissipation Ratings Table
Operating free air temperature, T_A: C suffix . . . . . 0°C to 70 °C
I suffix . . . . . –40°C to 85 °C
Storage temperature, T_{stg} . . . . . –65°C to 150 °C
Lead temperature 1,6 mm (1/16 Inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	740 mW	6 mW/°C	475 mW	385 mW

CAUTION: The THS4001 provides ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}	Dual supply	±2.5		±16	V
	Single supply	5		32	
Quiescent current, I_{CC}	±15 V		7.8	9.5	mA
	±5 V, ±2.5 V		6.7	8	
Operating free-air temperature, T_A	C suffix	0		70	°C
	I suffix	−40		85	

electrical characteristics, V_{CC} = ±15 V, R_L = 150 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
	Differential gain error	Gain = 2, f = 3.58 MHz, R_L = 150 Ω,		±15 V		0.04%		
				±5 V		0.01%		
	Differential phase error			±15 V		0.15°		
				±5 V		0.08°		
V_{IO}	Input offset voltage	T_A = 25°C		±15 V, ±5 V		2	8	mV
		T_A = full range					10	
I_{IB}	Input bias current	T_A = 25°C		±15 V, ±5 V		2.6	5	µA
		T_A = full range					6	
I_{OS}	Input offset current	T_A = 25°C		±15 V, ±5 V		35	200	nA
		T_A = full range					500	
	Open-loop gain	V_O = ±10 V, R_L = 1 kΩ	T_A = 25°C	±15 V	5	10		V/mV
			T_A = full range		3			
		V_O = ±2.5 V, R_L = 500 Ω	T_A = 25°C	±5 V	3	6		
			T_A = full range		2			
CMRR	Common-mode rejection ratio	$V_{(CM)}$ = ±12 V	T_A = 25°C	±15 V	85	100		dB
			T_A = full range		75			
PSRR	Power supply rejection ratio	T_A = 25°C		±15 V, ±5 V	75	85		dB
		T_A = full range			70			
V_{ICR}	Common-mode input voltage range			±15 V	13.5 to −13	14.8 to −14		V
				±5 V	3.6 to −2.7	4.4 to −3.6		
V_O	Output voltage swing	R_L = 500 Ω		±15 V	±13	±13.5		V
				±5 V	±3.3	±3.8		
				±2.5 V	±0.8	±1.3		
I_O	Output current			±15 V	50	100		mA
				±5 V	50	100		
				±2.5 V	50	100		
THD	Total harmonic distortion	V_I = 1 $V_{(PP)}$, f = 1 MHz		±15 V		−72		dBc
R_I	Input resistance					10		MΩ
C_I	Input capacitance					1.5		pF
R_O	Output resistance	Open loop				10		Ω

operating characteristics, V_{CC} = ±15 V, R_L = 150 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
	Slew rate	Gain = –1		±15 V		400		V/μs
				±5 V		400		
				±2.5 V		350		
	Settling time to 0.1%	10 V step (0 to 10 V),	Gain = –1	±15 V		40		ns
		–2.5 V to 2.5 V step,	Gain = –1	±5 V		30		
	–3 dB Bandwidth	Gain = +1, R_f = 150 Ω	R_L = 150 Ω,	±15 V		270		MHz
				±5 V		220		
				±2.5 V		180		
		Gain = –1, R_f = 150 Ω	R_L = 150 Ω,	±15 V		80		MHz
				±5 V		75		
				±2.5 V		70		
	Bandwidth for 0.1 dB flatness	Gain = +1		±15 V		60		MHz
				±5 V		50		
				±2.5 V		40		
V_n	Equivalent input noise voltage	f = 10 kHz		±15 V, ±5 V		12.5		nV/√Hz
I_n	Equivalent input noise current	f = 10 kHz		±15 V, ±5 V		1.5		pA/√Hz

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	1
V_{IO}	Input offset voltage	vs Free-air temperature	2
	Open-loop gain	vs Frequency	3
	Phase	vs Frequency	3
	Differential gain	vs DC voltage	4, 5
	Differential phase	vs DC voltage	4, 5
	Closed-loop gain	vs Frequency	6, 7
CMRR	Common-mode rejection ratio	vs Frequency	8
PSRR	Power-supply rejection ratio	vs Frequency	9
		vs Free-air temperature	10
$V_{O(PP)}$	Output voltage swing	vs Supply voltage	11
		vs Load resistance	12
	Bandwidth (–3 dB)	vs Feedback resistance	13, 14
I_{CC}	Supply current	vs Supply voltage	15
		vs Free-air temperature	16
E_{nv}	Noise spectral density	vs Frequency	17
THD	Total harmonic distortion	vs Frequency	18

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

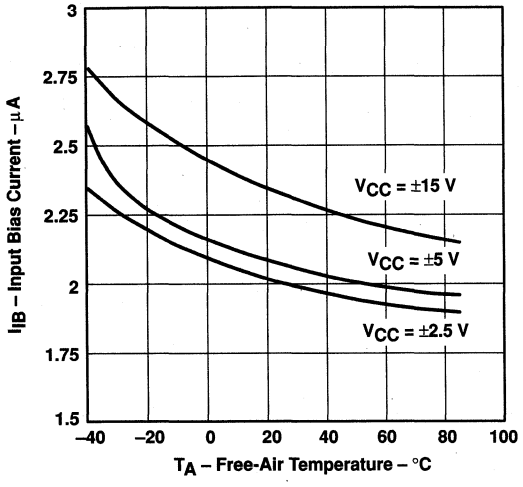


Figure 1

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

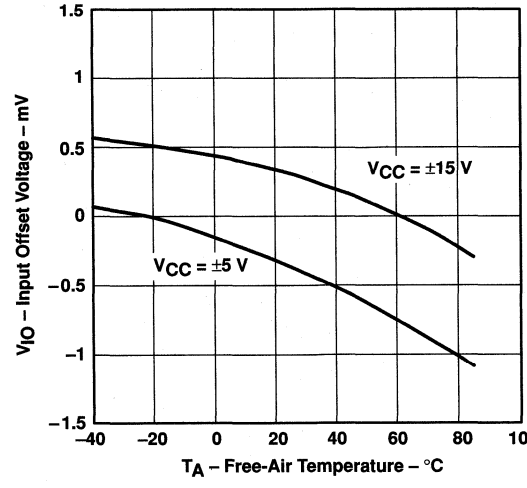


Figure 2

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

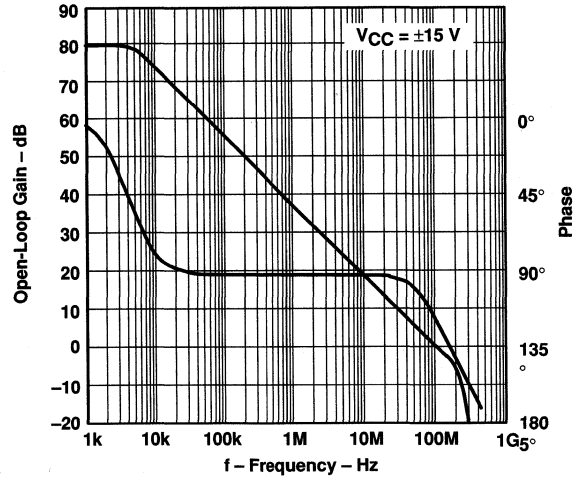


Figure 3

TYPICAL CHARACTERISTICS

DIFFERENTIAL GAIN AND
DIFFERENTIAL PHASE
vs
DC VOLTAGE

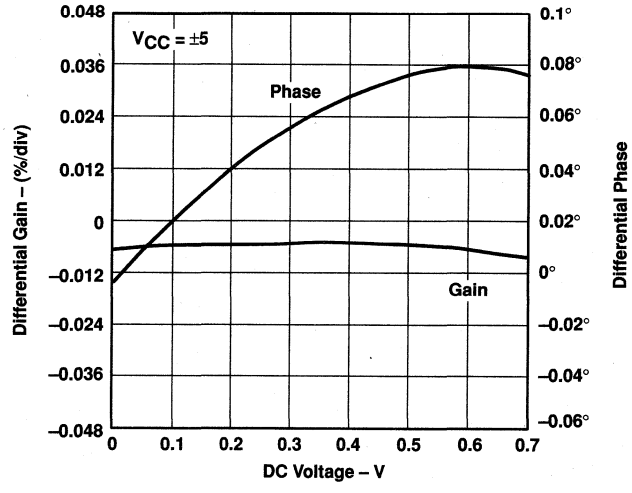


Figure 4

DIFFERENTIAL GAIN AND
DIFFERENTIAL PHASE
vs
DC VOLTAGE

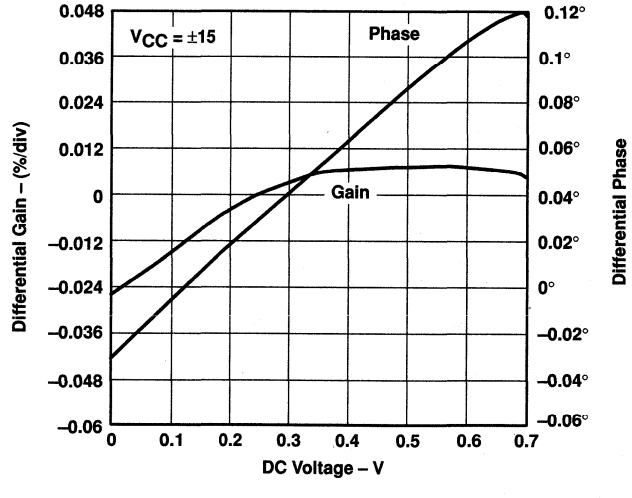


Figure 5

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN
vs
FREQUENCY

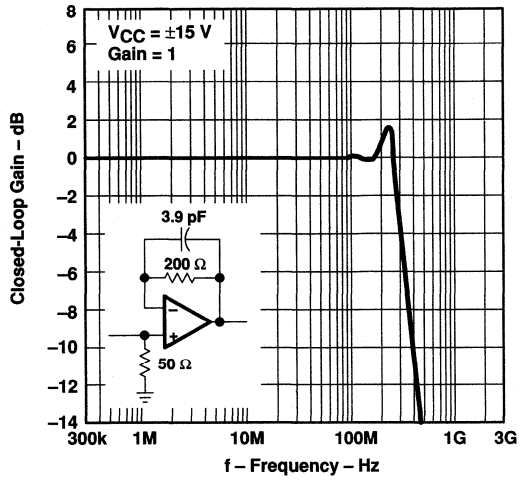


Figure 6

CLOSED-LOOP GAIN
vs
FREQUENCY

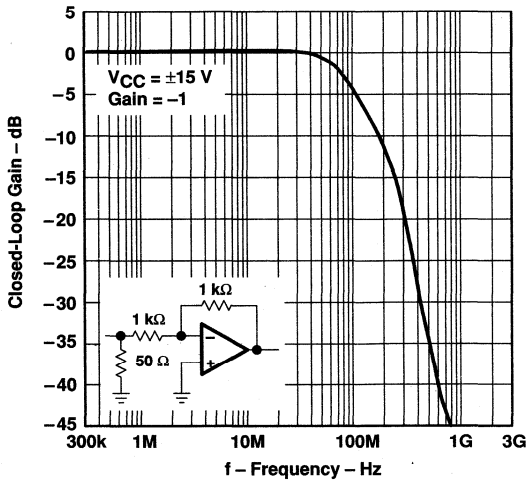


Figure 7

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

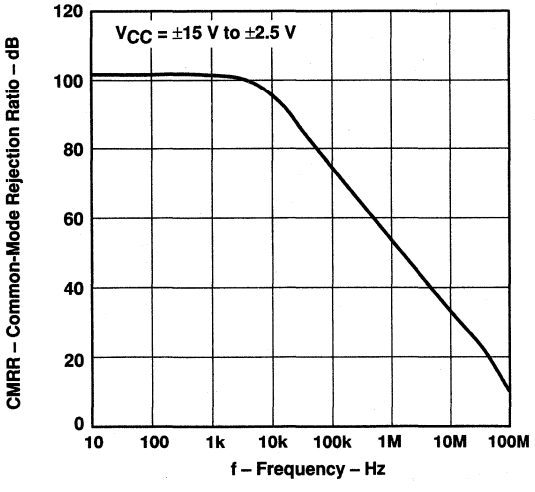


Figure 8

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

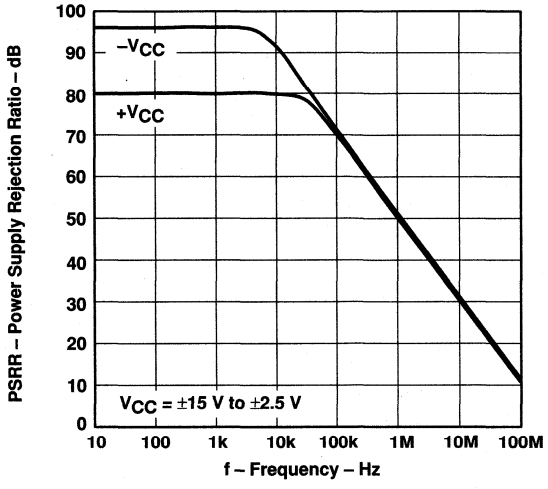


Figure 9

TYPICAL CHARACTERISTICS

POWER SUPPLY REJECTION RATIO
vs
FREE-AIR TEMPERATURE

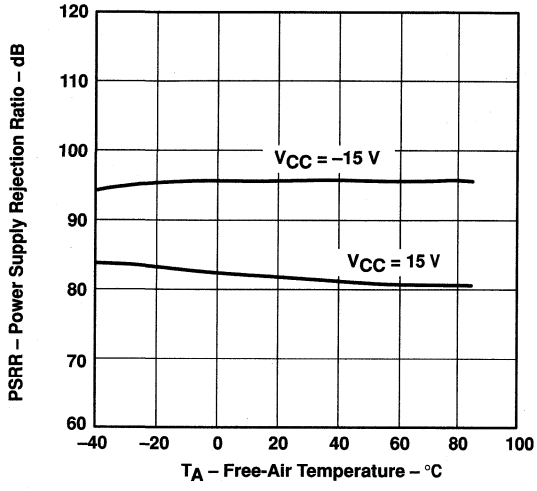


Figure 10

OUTPUT VOLTAGE SWING
vs
SUPPLY VOLTAGE

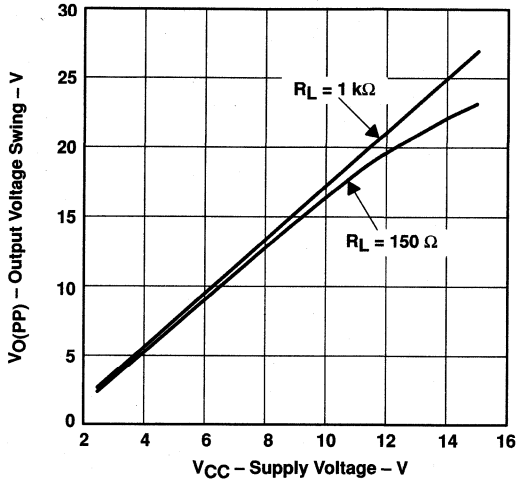


Figure 11

OUTPUT VOLTAGE SWING
vs
LOAD RESISTANCE

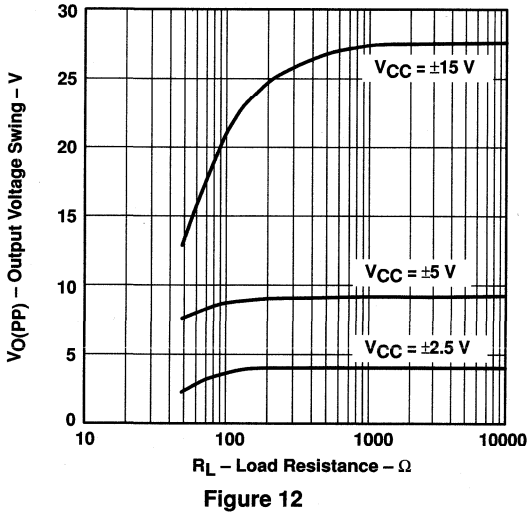


Figure 12

BANDWIDTH (–3 dB)
vs
FEEDBACK RESISTANCE

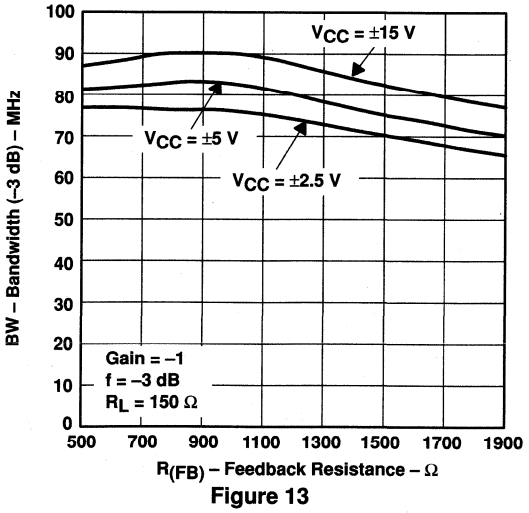


Figure 13

TYPICAL CHARACTERISTICS

BANDWIDTH (–3 dB)
vs
FEEDBACK RESISTANCE

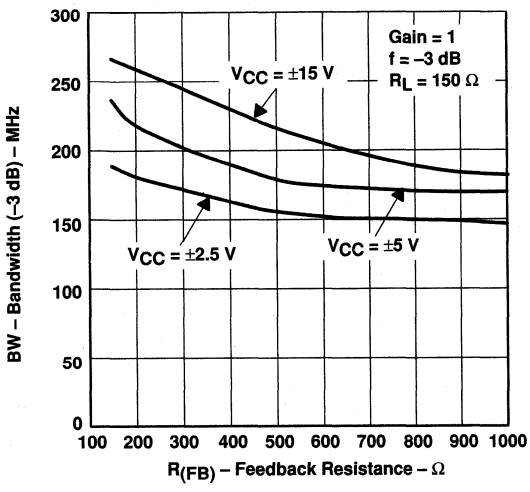


Figure 14

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

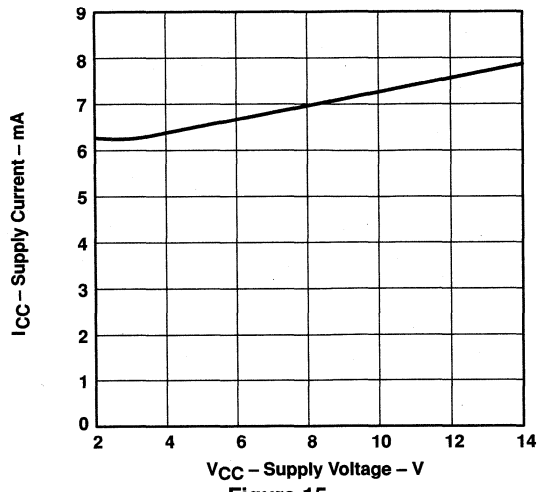


Figure 15

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

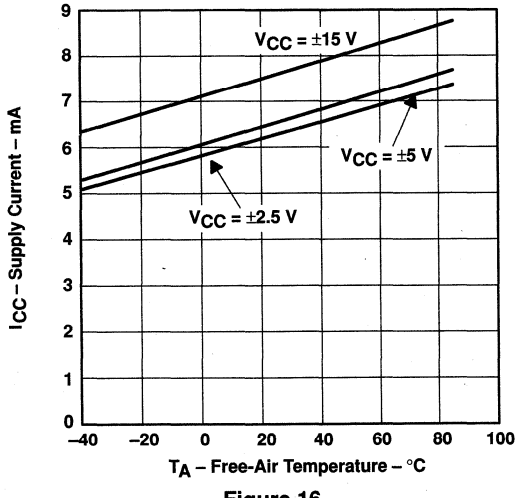


Figure 16

NOISE SPECTRAL DENSITY
vs
FREQUENCY

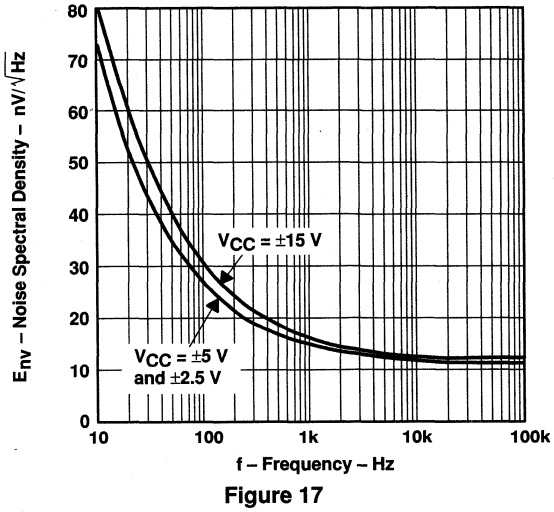


Figure 17

TYPICAL CHARACTERISTICS

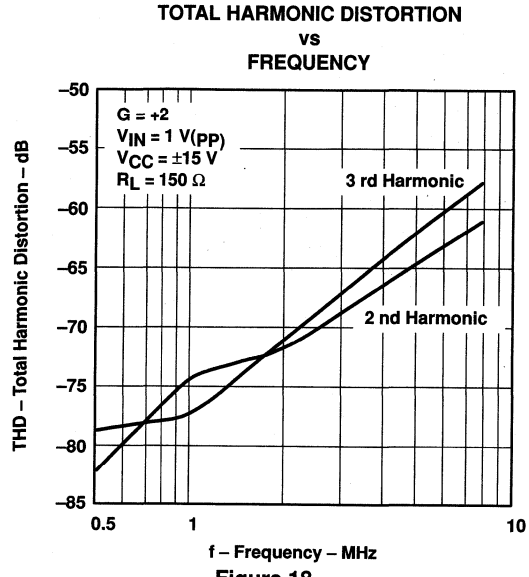


Figure 18

TEXAS INSTRUMENTS
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APPLICATION INFORMATION

theory of operation

The THS4001 is a high speed, operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This results in an exceptionally high performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 19.

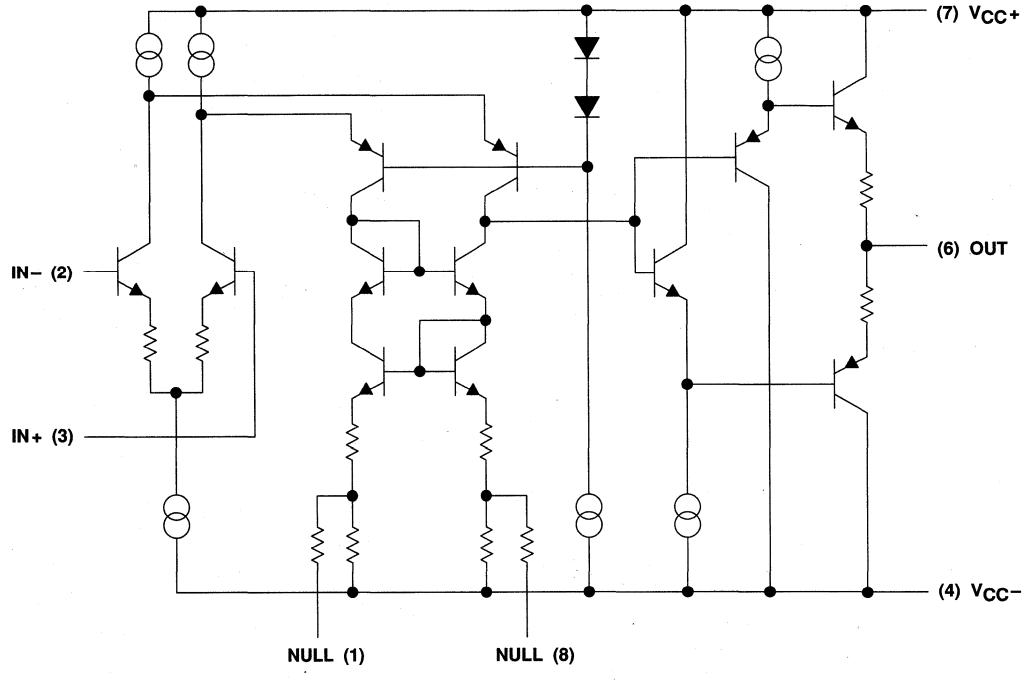


Figure 19. THS4001 Simplified Schematic

APPLICATION INFORMATION

offset nulling

The THS4001 has very low input offset voltage for a high-speed amplifier. However, if additional correction is required, an offset nulling function has been provided. By placing a potentiometer between terminals 1 and 8 of the device and tying the wiper to the negative supply, the input offset can be adjusted. This is shown in Figure 20.

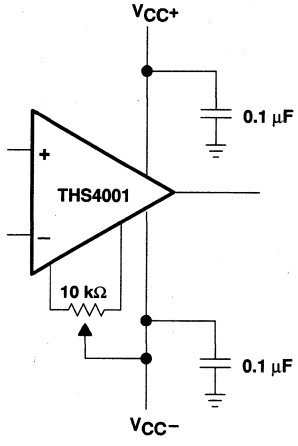


Figure 20. Offset Nulling Schematic

optimizing unity gain response

Internal frequency compensation of the THS4001 was selected to provide very wideband performance yet still maintain stability when operated in a noninverting unity gain configuration. When amplifiers are compensated in this manner there is usually peaking in the closed loop response and some ringing in the step response for very fast input edges, depending upon the application. This is because a minimum phase margin is maintained for the G=+1 configuration. For optimum settling time and minimum ringing, a feedback resistor of 200 Ω should be used as shown in Figure 21. Additional capacitance can also be used in parallel with the feedback resistance if even finer optimization is required.

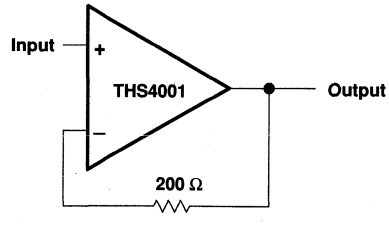


Figure 21. Noninverting, Unity Gain Schematic

APPLICATION INFORMATION

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS4001 has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 22. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

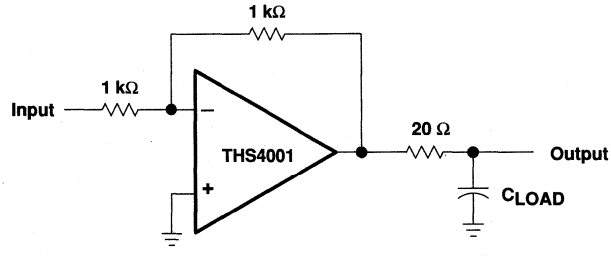


Figure 22. Driving a Capacitive Load

circuit layout considerations

In order to achieve the levels of high frequency performance of the THS4001, it is essential that proper printed-circuit board high frequency design techniques be followed. A general set of guidelines is given below. In addition, a THS4001 evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets are not recommended for high speed op amps. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.

APPLICATION INFORMATION

circuit layout considerations (continued)

- Surface-mount passive components – Using surface mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

evaluation board

An evaluation board is available for the THS4001 (literature number SLOP119). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 23. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. To order the evaluation board contact your local TI sales office or distributor. For more detailed information, refer to the *THS4001 EVM User's Manual* (literature number SLOU017).

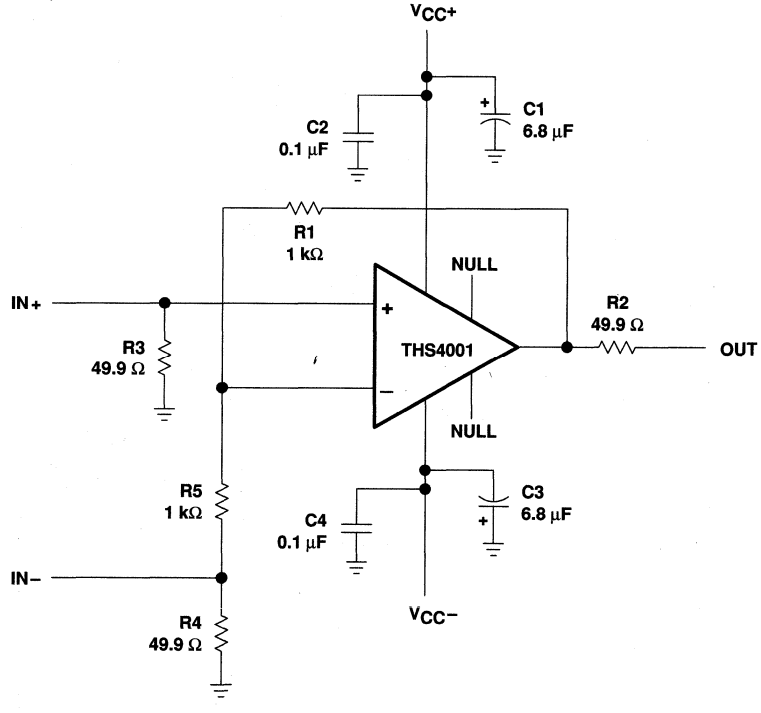
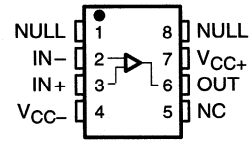


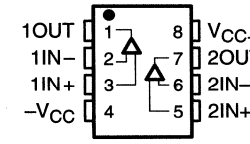
Figure 23.

- **Very High Speed**
  - **290 MHz Bandwidth (G = 1, –3 dB)**
  - **310 V/μs Slew Rate**
  - **37 ns Settling Time (0.1%)**
- **Very Low Distortion**
  - **THD = –80 dBc (f = 1 MHz, R_L = 150 Ω)**
- **110 mA Output Current Drive (Typical)**
- **7.5 nV/√Hz Voltage Noise**
- **Excellent Video Performance**
  - **70 MHz Bandwidth (0.1 dB, G = 1)**
  - **0.006% Differential Gain Error**
  - **0.01° Differential Phase Error**
- **±5 V to ±15 V Supply Voltage**
- **Available in Standard SOIC, MSOP PowerPAD, JG, or FK Packages**
- **Evaluation Module Available**

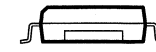
THS4011
JG, D AND DGN PACKAGE
(TOP VIEW)



THS4012
D AND DGN† PACKAGE
(TOP VIEW)



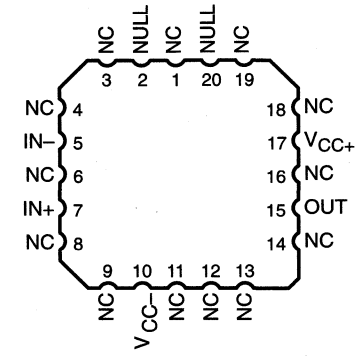
NC – No internal connection



Cross Section View Showing
PowerPAD Option (DGN)

† This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

THS4011
FK PACKAGE
(TOP VIEW)



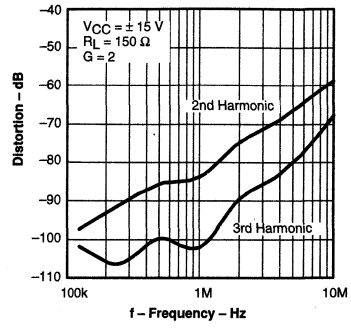
description

The THS4011 and THS4012 are very high speed, single/dual, voltage feedback amplifiers ideal for a wide range of applications. The devices offer very good ac performance with 290-MHz bandwidth, 310-V/μs slew rate, and 37-ns settling time (0.1%). These amplifiers have a high output drive capability of 110 mA and draw only 7.8-mA supply current per channel. For applications requiring low distortion, the THS4011/12 operate with a total harmonic distortion (THD) of –80 dBc at f = 1 MHz. For video applications, the THS4011/12 offer 0.1 dB gain flatness to 70-MHz, 0.006% differential gain error, and 0.01° differential phase error.

RELATED DEVICES	
DEVICE	**DESCRIPTION**
THS4011/2	290-MHz Low Distortion High-Speed Amplifiers
THS4031/2	100-MHz Low Noise High Speed-Amplifiers
THS4061/2	180-MHz High-Speed Amplifiers

CAUTION: THE THS4011 AND THS4012 provide ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

DISTORTION vs FREQUENCY



AVAILABLE OPTIONS

T_A	NUMBER OF CHANNELS	PACKAGED DEVICES				MSOP SYMBOL	EVALUATION MODULE
		PLASTIC SMALL OUTLINE† (D)	PLASTIC MSOP† (DGN)	CERAMIC DIP (JG)	CHIP CARRIER (FK)		
0°C to 70°C	1	THS4011CD	THS4011CDGN	—	—	TIACM	THS4011EVM
	2	THS4012CD	THS4012CDGN‡	—	—	TIABD	THS4012EVM
–40°C to 85°C	1	THS4011ID	THS4011IDGN	—	—	TIACN	—
	2	THS4012ID	THS4012IDGN‡	—	—	TIABZ	—
–55°C to 125°C	1	—	—	THS4011MJG	THS4011MFK	—	—

† The D and DGN packages are available taped and reeled. Add an R suffix to the device type (i.e., THS4011CDGNR).
‡ This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

functional block diagram

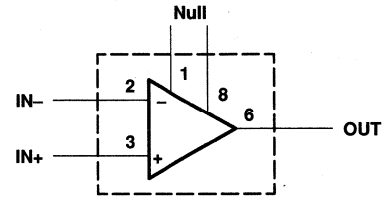


Figure 1. THS4011 – Single Channel

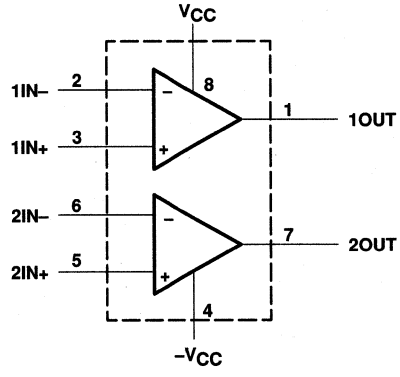


Figure 2. THS4012 – Dual Channel

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} ..... ±16.5 V
Input voltage, V_I ..... $\pm V_{CC}$
Output current, I_O ..... 175 mA
Differential input voltage, V_{ID} ..... ±4 V
Continuous total power dissipation ..... See Dissipation Rating Table
Maximum junction temperature, T_J ..... 150°C
Operating free-air temperature, T_A, THS401xC ..... 0°C to 70°C
THS401xI ..... –40°C to 85°C
THS4011M ..... –55°C to 125°C
Storage temperature, T_{stg} ..... –65°C to 150°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds, D, DGN package ..... 300°C
Lead temperature, 1,6 mm (1/16 inch) from case for 60 seconds, JG package ..... 300°C
Case temperature for 60 seconds, FK package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING
D	167†	38.3	740 mW
DGN‡	58.4	4.7	2.14 W
JG	119	28	1050 mW
FK	87.7	20	1375 mW

† This data was taken using the JEDEC standard Low-K test PCB. For the JEDEC Proposed High-K test PCB, the θ_{JA} is 95°C/W with a power rating at T_A = 25°C of 1.32 W.
‡ This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3 in. × 3 in. PC. For further information, refer to *Application Information* section of this data sheet.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	Split supply	±4.5		±16	V
	Single supply	9		32	
Operating free-air temperature, T_A	C suffix	0		70	°C
	I suffix	–40		85	
	M suffix	–55		125	

electrical characteristics, V_{CC} = ±15 V, R_L = 150 Ω, T_A = 25°C, (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS†		THS4011C/I, THS4012C/I MIN	TYP	MAX	UNIT
BW	Unity-gain bandwidth (–3 dB)	Gain = 1	V_{CC} = ±15 V		290		MHz
			V_{CC} = ±5 V		270		
	Bandwidth for 0.1 dB flatness	Gain = 1	V_{CC} = ±15 V		70		MHz
			V_{CC} = ±5 V		35		
	Full power bandwidth (see Note 2)	V_{CC} = ±15 V, R_L = 150 Ω	$V_{O(PP)}$ = 20 V,		4.9		MHz
		V_{CC} = ±5 V, R_L = 150 Ω,	$V_{O(PP)}$ = 5 V,		16		
SR	Slew rate	Gain = –1, R_L = 150 Ω	V_{CC} = ±15 V		310		V/μs
			V_{CC} = ±5 V		260		
t_s	Settling time to 0.1%	V_I = –2.5 V to 2.5 V, Gain = –1	V_{CC} = ±15 V		37		ns
			V_{CC} = ±5 V		35		
	Settling time to 0.01%	V_I = –2.5 V to 2.5 V, Gain = –1	V_{CC} = ±15 V		90		ns
			V_{CC} = ±5 V		70		

† Full range = 0°C to 70°C for the C suffix and –40°C to 85°C for the I suffix.

noise/distortion performance

PARAMETER		TEST CONDITIONS†		THS4011C/I, THS4012C/I MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	V_{CC} = ±15 V, $V_{O(PP)}$ = 2 V	f_c = 1 MHz,		–80		dBc
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz		7.5		nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz		1		pA/√Hz
	Differential gain error	Gain = 2, R_L = 150 Ω, NTSC	V_{CC} = ±15 V		0.01%		
			V_{CC} = ±5 V		0.01%		
	Differential phase error	Gain = 2, R_L = 150 Ω, NTSC	V_{CC} = ±15 V		0.01°		
			V_{CC} = ±5 V		0.001°		

† Full range = 0°C to 70°C for the C suffix and –40°C to 85°C for the I suffix.

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

dc performance

PARAMETER		TEST CONDITIONS†		THS4011C/I, THS4012C/I MIN	TYP	MAX	UNIT
	Open loop gain	V_{CC} = ±15 V, V_O = ±10 V, R_L = 1 kΩ	T_A = 25°C	10	25		V/mV
			T_A = full range	8			
		V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 250 Ω	T_A = 25°C	7	12		V/mV
			T_A = full range	5			
V_{IO}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		1	6	mV
			T_A = full range			8	
	Input offset voltage drift					15	μV/°C

I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V	T_A = 25°C	2	6	µA
			T_A = full range		8	
I_{IO}	Input offset current	V_{CC} = ±5 V or ±15 V	T_A = 25°C	25	250	nA
			T_A = full range		400	
	Offset current drift	V_{CC} = ±5 V or ±15 V		0.3		nA/°C

† Full range = 0°C to 70°C for the C suffix and –40°C to 85°C for the I suffix.

input characteristics

PARAMETER		TEST CONDITIONS†		THS4011C/I, THS4012C/I			UNIT
				MIN	TYP	MAX	
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V		±13	±14.1		V
		V_{CC} = ±5 V		±3.8	±4.3		
CMRR	Common-mode rejection ratio	V_{CC} = ±15 V, V_{IC} = ±12 V	T_A = 25°C	82	110		dB
			T_A = full range	77			dB
		V_{CC} = ±5 V, V_{IC} = ±2.5 V	T_A = 25°C	90	95		dB
			T_A = full range	83			
R_I	Input resistance				2		MΩ
C_I	Input capacitance				1.2		pF

† Full range = 0°C to 70°C for the C suffix and –40°C to 85°C for the I suffix.

output characteristics

PARAMETER		TEST CONDITIONS†		THS4011C/I, THS4012C/I			UNIT
				MIN	TYP	MAX	
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.5		V
		V_{CC} = ±5 V		±3.4	±3.7		
		V_{CC} = ±15 V	R_L = 250 Ω	±12	±13		
		V_{CC} = ±5 V	R_L = 150 Ω	±3	±3.4		
I_O	Output current	R_L = 20 Ω,	V_{CC} = ±15 V	70	110		mA
			V_{CC} = ±5 V	50	75		
I_{OS}	Short-circuit output current	V_{CC} = ±15 V			150		mA
R_O	Output resistance	Open loop			12		Ω

† Full range = 0°C to 70°C for the C suffix and –40°C to 85°C for the I suffix.

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

power supply

PARAMETER		TEST CONDITIONS†		THS4011C/I, THS4012C/I			UNIT
				MIN	TYP	MAX	
V_{CC}	Supply voltage	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (each amplifier)	V_{CC} = ±15 V	T_A = 25°C		7.8	9.5	mA
			T_A = full range			11	
		V_{CC} = ±5 V	T_A = 25°C		6.9	8.5	
			T_A = full range			10	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V to ±15 V	T_A = 25°C	75	83		dB
			T_A = full range	68			

† Full range = 0°C to 70°C for the C suffix and –40°C to 85°C for the I suffix.

electrical characteristics, V_{CC} = ±15 V, R_L = 150 Ω, T_A = 25°C, (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS†		THS4011M MIN	THS4011M TYP	THS4011M MAX	UNIT
BW	Unity-gain bandwidth	Closed loop, R_L = 1 kΩ	V_{CC} = ±15 V	*160	200		MHz
	Bandwidth for 0.1 dB flatness	Gain = 1	V_{CC} = ±15 V		70		MHz
			V_{CC} = ±5 V		35		
			V_{CC} = ±2.5 V		30		
	Full power bandwidth (see Note 1)	V_{CC} = ±15 V, R_L = 150 Ω,	$V_{O(PP)}$ = 20 V		2.5		MHz
		V_{CC} = ±5 V, R_L = 150 Ω,	$V_{O(PP)}$ = 20 V		8		
SR	Slew rate	V_{CC} = ±15 V, R_L = 1 kΩ		*300	400		V/μs
t_s	Settling time to 0.1%	V_I = –2.5 V to 2.5 V, Gain = –1	V_{CC} = ±15 V		37		ns
			V_{CC} = ±5 V		35		
	Settling time to 0.01%	V_I = –2.5 V to 2.5 V, Gain = –1	V_{CC} = ±15 V		90		ns
			V_{CC} = ±5 V		70		

† Full range = –55°C to 125°C for the M suffix.
*This parameter is not tested.
NOTE 1: Full pwer bandwidth = slew rate/2π $V_{(PP)}$.

noise/distortion performance

PARAMETER		TEST CONDITIONS†		THS4011M MIN	THS4011M TYP	THS4011M MAX	UNIT
THD	Total harmonic distortion	V_{CC} = ±15 V, $V_{O(PP)}$ = 1 V	f_c = 1 MHz,		–80		dBc
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz		7.5		nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz		1		pA/√Hz
	Differential gain error	Gain = 2, R_L = 150 Ω, NTSC	V_{CC} = ±15 V		0.006		%
			V_{CC} = ±5 V		0.001		
	Differential phase error	Gain = 2, R_L = 150 Ω, NTSC	V_{CC} = ±15 V		0.01°		
			V_{CC} = ±5 V		0.002°		

† Full range = –55°C to 125°C for the M suffix.

electrical characteristics at T_A = full range, V_{CC} = ±15 V, R_L = 1 kΩ (unless otherwise noted) (continued)

dc performance

PARAMETER		TEST CONDITIONS†		THS4011M MIN	THS4011M TYP	THS4011M MAX	UNIT
	Open loop gain	V_{CC} = ±15 V, R_L = 1 kΩ	V_O = ±10 V, T_A = full range	6	14		V/mV
		V_{CC} = ±5 V, R_L = 1 kΩ	V_O = ±2.5 V, T_A = full range	5	10		V/mV
V_{IO}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		2	6	mV
			T_A = full range		2	8	
	Input offset voltage drift	V_{CC} = ±5 V or ±15 V			15		μV/°C
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		2	6	μA
			T_A = full range		4	8	

I_{IO}	Input offset current	V_{CC} = ±5 V or ±15 V			25 250	nA
	Offset current drift	V_{CC} = ±5 V or ±15 V	T_A = 25°C		0.3	nA/°C

† Full range = –55°C to 125°C for the M suffix.

input characteristics

PARAMETER		TEST CONDITIONS†		THS4011M			UNIT
				MIN	TYP	MAX	
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V		±13	±14.1		V
		V_{CC} = ±5 V		±3.8	±4.3		
CMRR	Common-mode rejection ratio	V_{CC} = ±15 V,	V_{IC} = ±12 V	75	90		dB
		V_{CC} = ±5 V,	V_{IC} = ±2.5 V	84	95		
R_I	Input resistance				2		MΩ
C_I	Input capacitance				1.2		pF

† Full range = –55°C to 125°C for the M suffix.

output characteristics

PARAMETER		TEST CONDITIONS†		THS4011M			UNIT
				MIN	TYP	MAX	
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.5		V
		V_{CC} = ±5 V		±3.4	±3.7		
		V_{CC} = ±15 V	R_L = 250 Ω	±12	±13		
		V_{CC} = ±5 V	R_L = 150 Ω	±3	±3.4		
I_O	Output current	V_{CC} = ±15 V	R_L = 20 Ω	70	115		mA
		V_{CC} = ±5 V		50	75		
I_{OS}	Short-circuit output current	V_{CC} = ±15 V	T_A = 25°C		150		mA
R_O	Output resistance	Open loop			12		Ω

† Full range = –55°C to 125°C for the M suffix.

electrical characteristics at T_A = full range, V_{CC} = ±15 V, R_L = 1 kΩ (unless otherwise noted) (continued)

power supply

PARAMETER		TEST CONDITIONS†		THS4011M			UNIT
				MIN	TYP	MAX	
V_{CC}	Supply voltage	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Quiescent current	V_{CC} = ±15 V	T_A = 25°C		7.8	9.5	mA
			T_A = full range			11	
		V_{CC} = ±5 V	T_A = 25°C		6.9	8.5	
			T_A = full range			10	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V to ±15 V	T_A = 25°C	80	86		dB
			T_A = full range	78	83		

† Full range = –55°C to 125°C for the M suffix.

PARAMETER MEASUREMENT INFORMATION

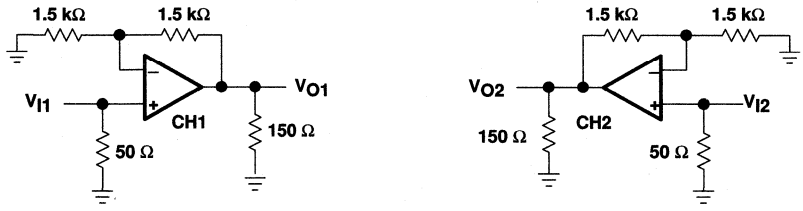


Figure 3. THS4012 Crosstalk Test Circuit

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

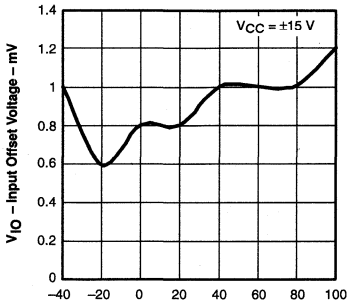


Figure 4

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

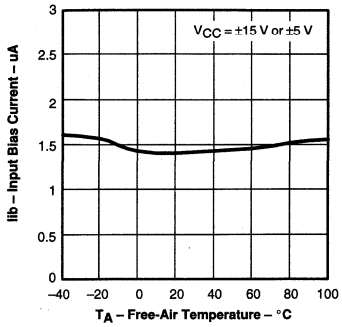


Figure 5

OUPUT VOLTAGE
vs
SUPPLY VOLTAGE

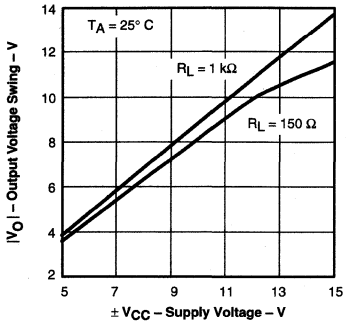


Figure 6

MAXIMUM OUTPUT VOLTAGE SWING
vs
FREE-AIR TEMPERATURE

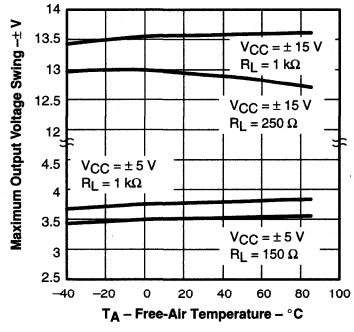


Figure 7

COMMON-MODE INPUT VOLTAGE
vs
SUPPLY VOLTAGE

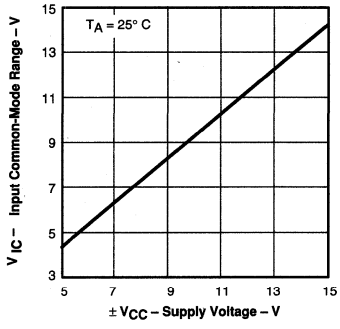


Figure 8

PSRR
vs
FREQUENCY

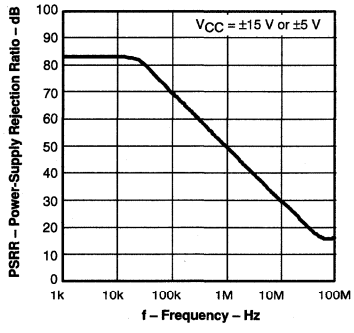


Figure 9

CMRR
vs
FREQUENCY

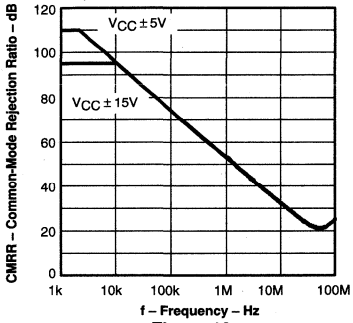


Figure 10

CROSSTALK
vs
FREQUENCY

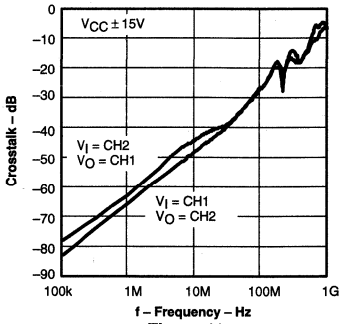


Figure 11

OPEN-LOOP GAIN RESPONSE

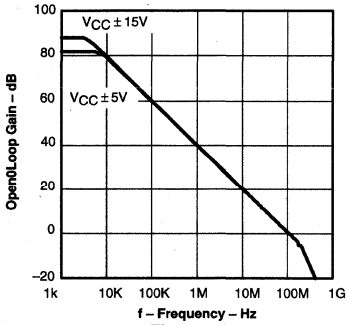


Figure 12

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

DISTORTION vs FREQUENCY

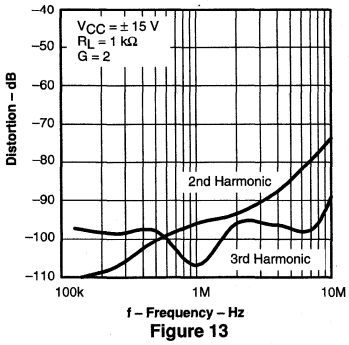

Figure 13

DISTORTION vs FREQUENCY

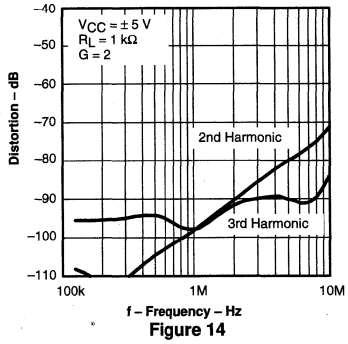

Figure 14

DISTORTION vs FREQUENCY

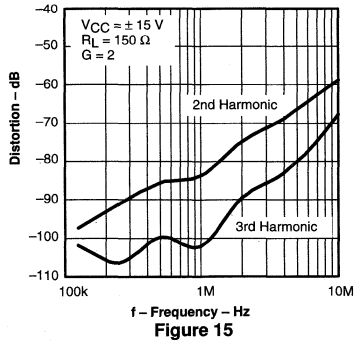

Figure 15

DISTORTION vs FREQUENCY

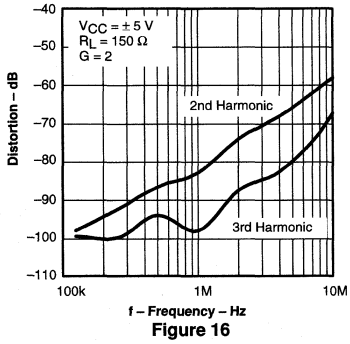

Figure 16

OUTPUT AMPLITUDE vs FREQUENCY

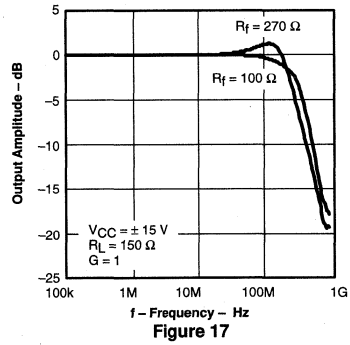

Figure 17

OUTPUT AMPLITUDE vs FREQUENCY

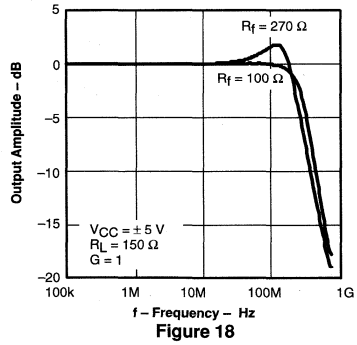

Figure 18

NOISE SPECTRAL DENSITY vs FREQUENCY

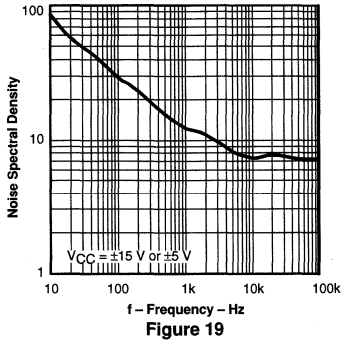

Figure 19

DIFFERENTIAL PHASE vs NUMBER OF 150-Ω LOADS

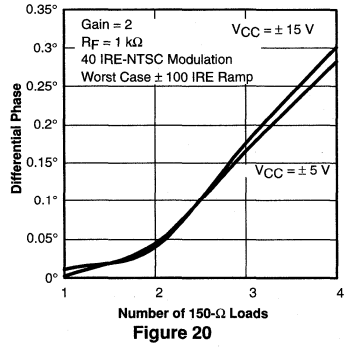

Figure 20

TYPICAL CHARACTERISTICS

DIFFERENTIAL PHASE vs NUMBER OF 150-Ω LOADS

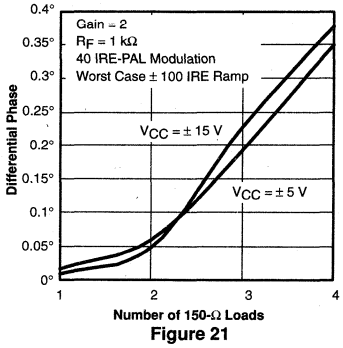

Figure 21

DIFFERENTIAL GAIN vs NUMBER OF 150-Ω LOADS

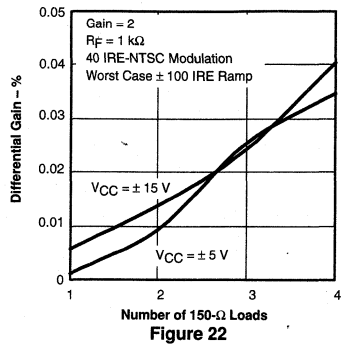

Figure 22

DIFFERENTIAL GAIN vs NUMBER OF 150-Ω LOADS

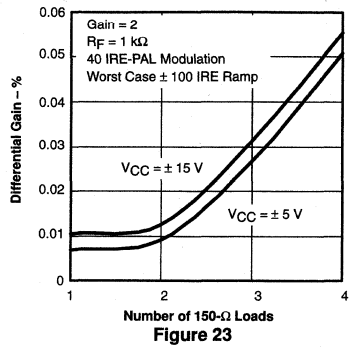

Figure 23

APPLICATION INFORMATION

theory of operation

The THS401x is a high-speed, operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This results in an exceptionally high performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 24.

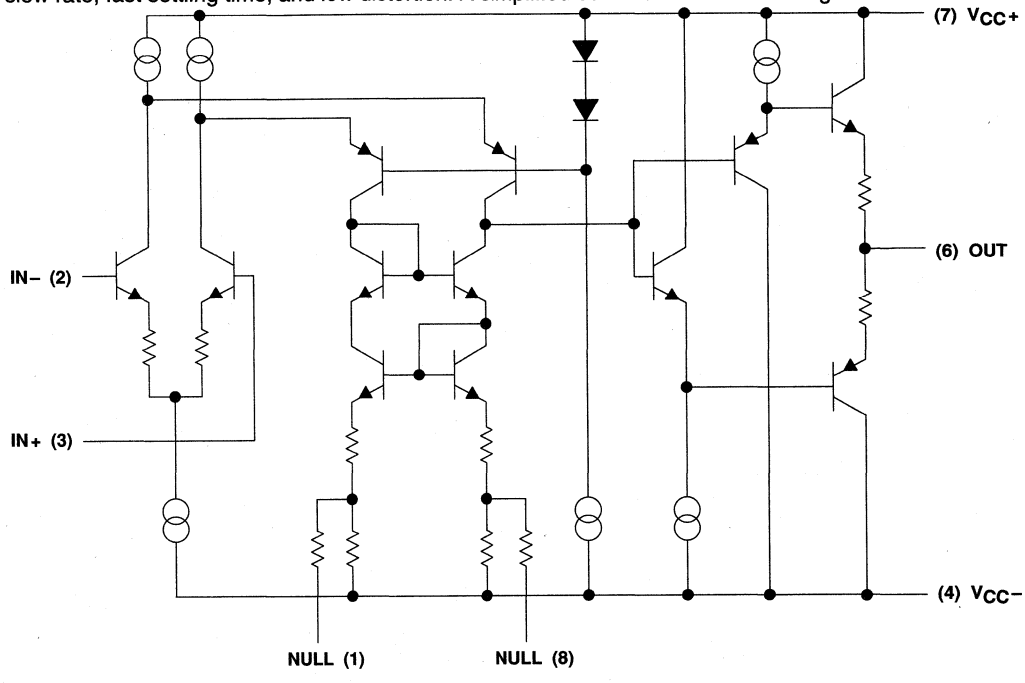

Figure 24. THS4011 Simplified Schematic

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true when amplifying small signals. The noise model for the THS401x is shown in Figure 25. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise ($nV/\sqrt{Hz}$)
- IN+ = Noninverting current noise ($pA/\sqrt{Hz}$)
- IN– = Inverting current noise ($pA/\sqrt{Hz}$)
- e_{Rx} = Thermal voltage noise associated with each resistor ($e_{Rx} = 4\ kTR_x$)

APPLICATION INFORMATION

noise calculations and noise figure (continued)

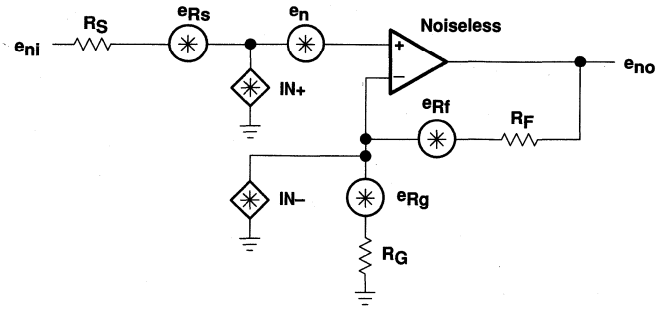

Figure 25. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN + \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\ kTR_S + 4\ kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\ A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (noninverting case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

For more information on noise analysis, please refer to the *Noise Analysis* section in *Operational Amplifier Circuits Applications Report* (literature number SLVA043).

APPLICATION INFORMATION

noise calculations and noise figure (continued)

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^{\,2}}{\left(e_{Rs}\right)^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\ kTR_S}\right]$$

Figure 26 shows the noise figure graph for the THS401x.

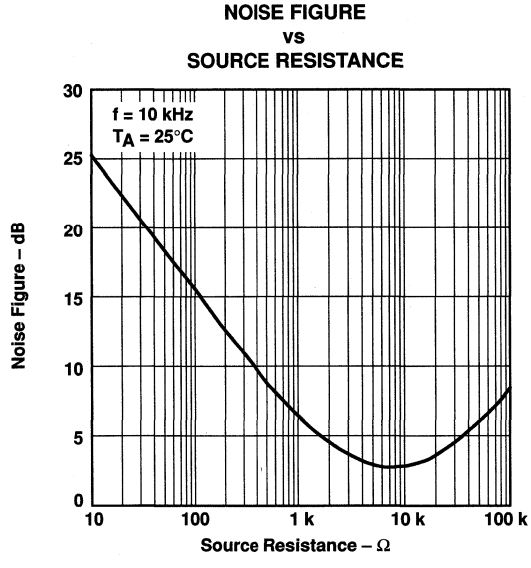

Figure 26. Noise Figure vs Source Resistance

APPLICATION INFORMATION

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS401x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 27. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

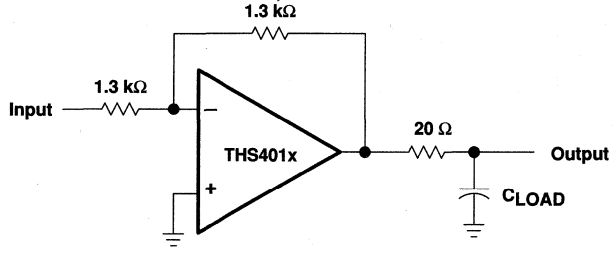

Figure 27. Driving a Capacitive Load

offset nulling

The THS401x has very low input offset voltage for a high-speed amplifier. However, if additional correction is required, an offset nulling function has been provided on the THS4011. The input offset can be adjusted by placing a potentiometer between terminals 1 and 8 of the device and tying the wiper to the negative supply. This is shown in Figure 28.

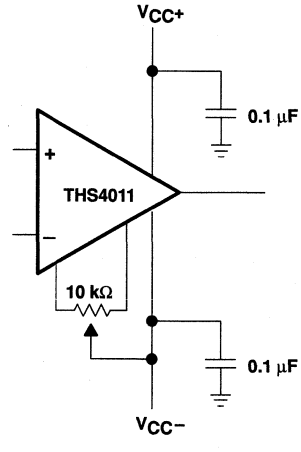

Figure 28. Offset Nulling Schematic

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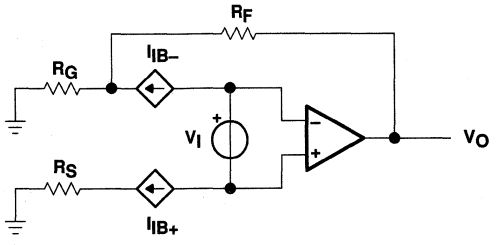
APPLICATION INFORMATION

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\ R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\ R_F$$

Figure 29. Output Offset Voltage Model

optimizing unity gain response

Internal frequency compensation of the THS401x was selected to provide very wideband performance yet still maintain stability when operated in a noninverting unity gain configuration. When amplifiers are compensated in this manner there is usually peaking in the closed loop response and some ringing in the step response for very fast input edges, depending upon the application. This is because a minimum phase margin is maintained for the G=+1 configuration. For optimum settling time and minimum ringing, a feedback resistor of 100 Ω should be used as shown in Figure 30. Additional capacitance can also be used in parallel with the feedback resistance if even finer optimization is required.

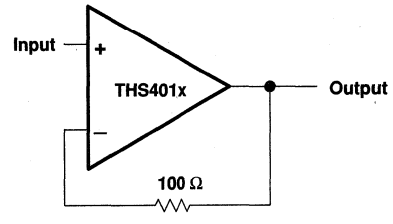
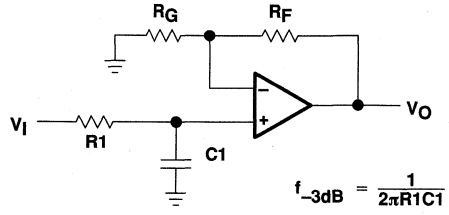


Figure 30. Noninverting, Unity Gain Schematic

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifer (see Figure 31).

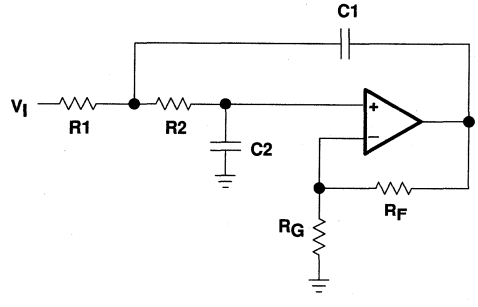


$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 31. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.



R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 32. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high frequency performance of the THS401x, follow proper printed-circuit board high frequency design techniques. A general set of guidelines is given below. In addition, a THS401x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

general PowerPAD design considerations

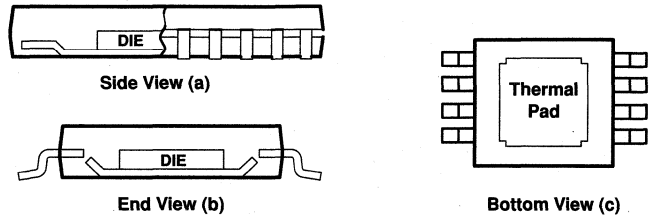
The THS401x is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 33(a) and Figure 33(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 33(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.

APPLICATION INFORMATION

general PowerPAD design considerations (continued)



NOTE A. The thermal pad is electrically isolated from all terminals in the package.

Figure 33. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach.

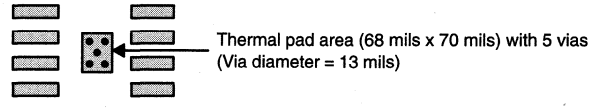


Figure 34. PowerPAD PCB Etch and Via Pattern

1. Prepare the PCB with a top side etch pattern as shown in Figure 34. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS401xDGN IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS401xDGN package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the THS401xDGN IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

APPLICATION INFORMATION

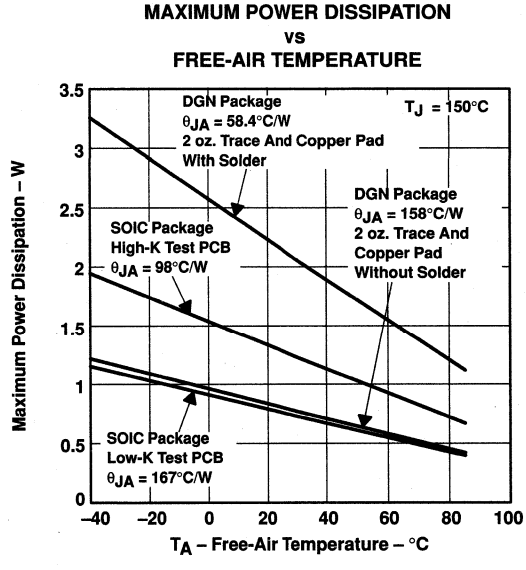
general PowerPAD design considerations (continued)

The actual thermal performance achieved with the THS401xDGN in its PowerPAD package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA}, is about 58.4°C/W. For comparison, the non-PowerPAD version of the THS401x IC (SOIC) is shown. For a given θ_{JA}, the maximum power dissipation is shown in Figure 35 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of THS401x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A. Results are with no air flow and PCB size = 3"× 3"

Figure 35. Maximum Power Dissipation vs Free-Air Temperature

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially muti-amplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 36 to Figure 39 show this effect, along with the quiescent heat, with an ambient air temperature of 50°C. When using V_{CC} = ±5 V, there is generally not a heat problem, even with SOIC packages. But, when using V_{CC} = ±15 V, the SOIC package is severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual amplifier package (THS4012), the sum of the RMS output currents and voltages should be used to choose the proper package.

THS4011
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

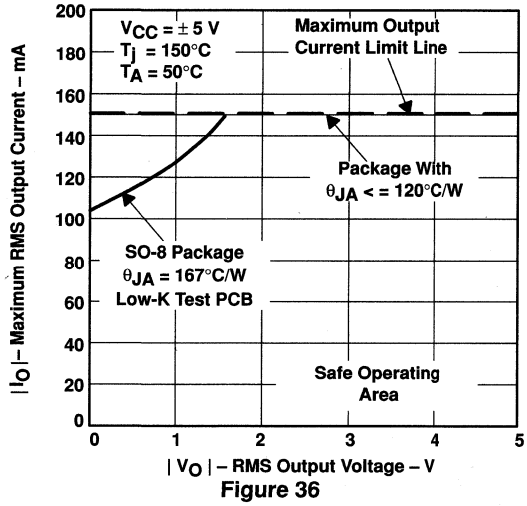


Figure 36

THS4011
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

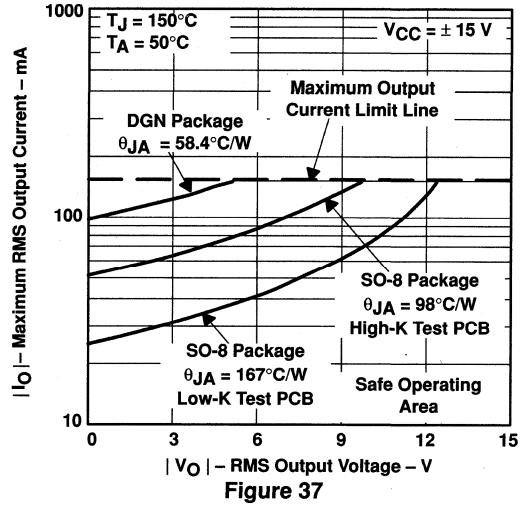


Figure 37

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

THS4012
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

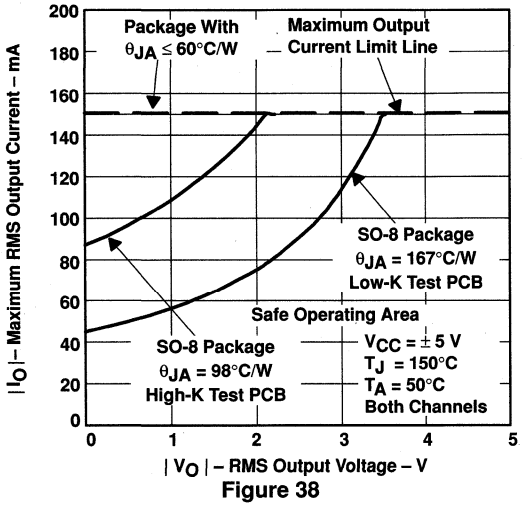


Figure 38

THS4012
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

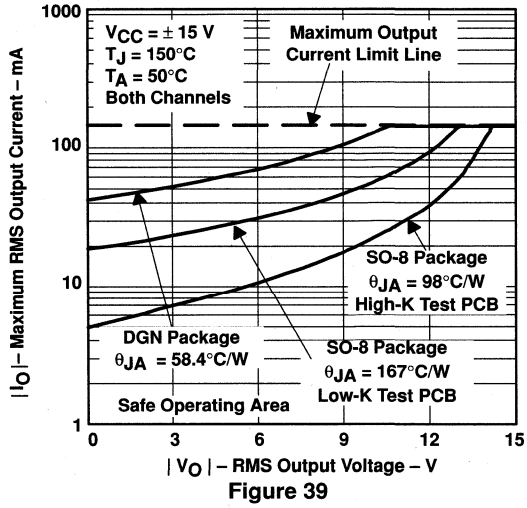


Figure 39

APPLICATION INFORMATION

evaluation board

An evaluation board is available for the THS4011 (literature number SLOP128) and THS4012 (literature number SLOP230). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the THS4011 evaluation board is shown in Figure 40. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. For more information, please refer to the *THS4011 EVM User's Guide* (literature number SLOU028) or the *THS4012 EVM User's Guide* (literature number SLOU041) To order the evaluation board contact your local TI sales office or distributor.

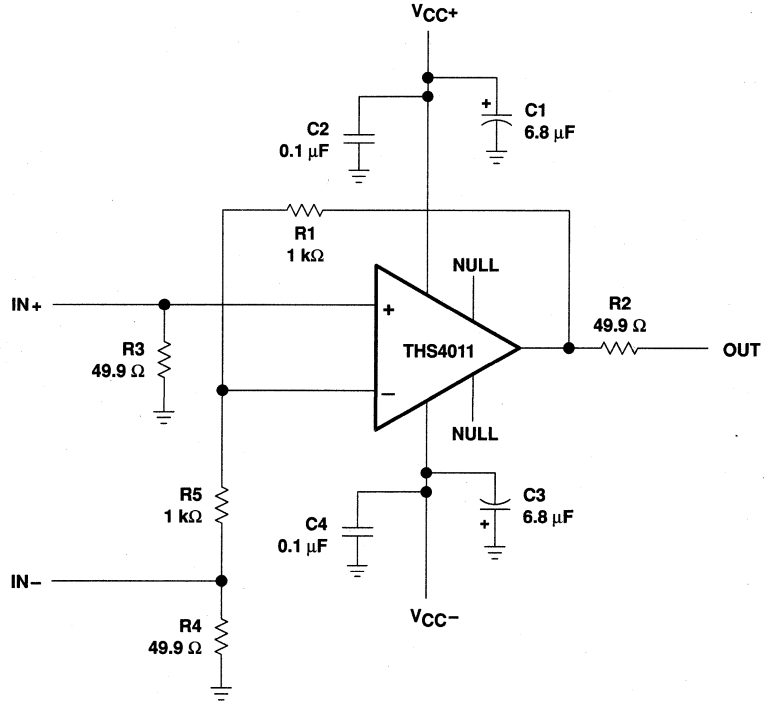
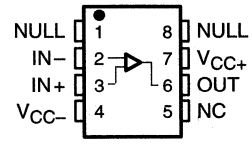


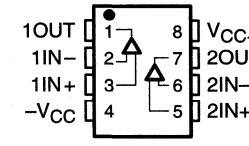
Figure 40. THS4011 Evaluation Board

- **Ultra-Low 1.5 nV/√Hz Voltage Noise**
- **High Speed**
  - **350 MHz Bandwidth (G = 10, –3 dB)**
  - **470 V/μs Slew Rate**
  - **40 ns Settling Time (0.1%)**
- **Stable at a Gain of 10 (–9) or Greater**
- **High Output Drive, I_O = 100 mA (typ)**
- **Excellent Video Performance**
  - **17 MHz Bandwidth (0.1 dB, G = 10)**
  - **0.02% Differential Gain**
  - **0.08° Differential Phase**
- **Very Low Distortion**
  - **THD = –68 dBc (f = 1 MHz, R_L = 150 Ω)**
- **Wide Range of Power Supplies**
  - **V_{CC} = ±5 V to ±15 V**
- **Available in Standard SOIC or MSOP PowerPAD™ Package**
- **Evaluation Module Available**

THS4021
D AND DGN PACKAGE
(TOP VIEW)



THS4022
D AND DGN PACKAGE
(TOP VIEW)



NC – No internal connection

Cross Section View Showing
PowerPAD Option (DGN)

VOLTAGE & CURRENT NOISE
vs
FREQUENCY

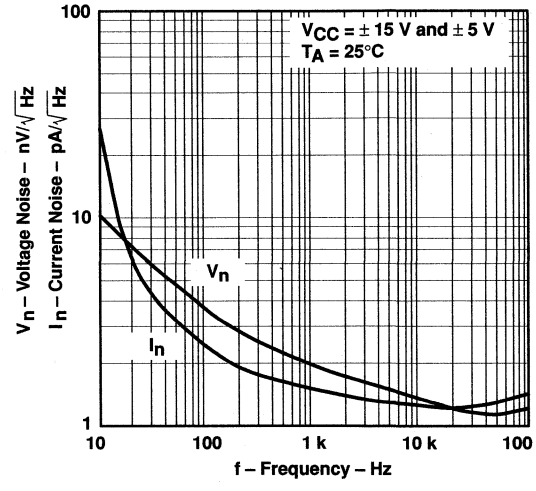


Figure 1

description

The THS4021 and THS4022 are ultra-low voltage noise, high-speed voltage feedback amplifiers that are ideal for applications requiring low voltage noise, including communication and imaging. The signal-amplifier THS4021 and the dual-amplifier THS4022 offer very good ac performance with 350-MHz bandwidth, 470-V/μs slew rate, and 40-ns settling time (0.1%). The THS4021 and THS4022 are stable at gains of 10 (–9) or greater. These amplifiers have a high drive capability of 100 mA and draw only 7.8-mA supply current per channel. With total harmonic distortion (THD) of –68 dBc at f = 1 MHz, the THS4021 and THS4022 are ideally suited for applications requiring low distortion.

RELATED DEVICES	
DEVICE	**DESCRIPTION**
THS4011/2	290-MHz Low Distortion High-Speed Amplifiers
THS4031/2	100-MHz Low Noise High-Speed Amplifiers
THS4061/2	180-MHz High-Speed Amplifiers

CAUTION: The THS4021 and THS4022 provide ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

PowerPAD is a trademark of Texas Instruments Incorporated.

AVAILABLE OPTIONS

T_A	NUMBER OF CHANNELS	PACKAGED DEVICES		MSOP SYMBOL	EVALUATION MODULE
		PLASTIC SMALL OUTLINE† (D)	PLASTIC MSOP† (DGN)		
0°C to 70°C	1	THS4021CD	THS4021CDGN	ACK	THS4021EVM
	2	THS4022CD	THS4022CDGN	ACL	THS4022EVM
–40°C to 85°C	1	THS4021ID	THS4021IDGN	ACA	—
	2	THS4022ID	THS4022IDGN	ACB	—

† The D and DGN packages are available taped and reeled. Add an R suffix to the device type (i.e., THS4021CDGN).

functional block diagram

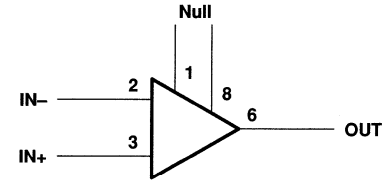


Figure 2. THS4021 – Single Channel

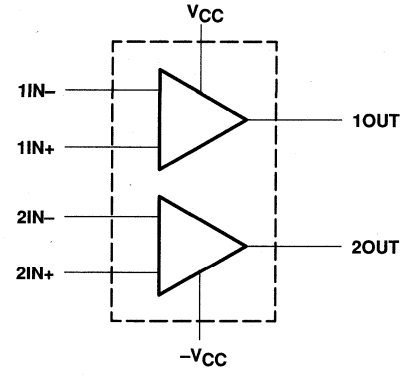


Figure 3. THS4022 – Dual Channel

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} ..... ±16.5 V
Input voltage, V_I ..... $\pm V_{CC}$
Output current, I_O ..... 150 mA
Differential input voltage, V_{IO} ..... ±4 V
Continuous total power dissipation ..... See Dissipation Rating Table
Maximum junction temperature, T_J ..... 150°C
Operating free-air temperature, T_A: C-suffix ..... 0°C to 70°C
I-suffix ..... −40°C to 85°C
Storage temperature, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING
D	167‡	38.3	740 mW
DGN§	58.4	4.7	2.14 W

‡ This data was taken using the JEDEC standard Low-K test PCB. For the JEDEC Proposed High-K test PCB, the θ_{JA} is 95°C/W with a power rating at T_A = 25°C of 1.32 W.
§ This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3 in. × 3 in. PC. For further information, refer to *Application Information* section of this data sheet.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} and V_{CC-}	Dual supply	±4.5		±16	V
	Single supply	9		32	
Operating free-air temperature, T_A	C-suffix	0		70	°C
	I-suffix	−40		85	

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
BW	Small-signal bandwidth (–3 dB)	V_{CC} = ±15 V		Gain = 10		350		MHz
		V_{CC} = ±5 V				280		
		V_{CC} = ±15 V		Gain = 20		80		MHz
		V_{CC} = ±5 V				70		
	Bandwidth for 0.1 dB flatness	V_{CC} = ±15 V		Gain = 10		17		MHz
		V_{CC} = ±5 V				17		
	Full power bandwidth†	$V_{O(pp)}$ = 20 V,	V_{CC} = ±15 V			3.7		MHz
		$V_{O(pp)}$ = 5 V,	V_{CC} = ±5 V			11.8		
SR	Slew rate‡	V_{CC} = ±15 V,	10-V step,	Gain = 10		470		V/µs
		V_{CC} = ±5 V,	5-V step			370		
t_s	Settling time to 0.1%	V_{CC} = ±15 V,	5-V step	Gain = –10		40		ns
		V_{CC} = ±5 V,	2-V step			50		
	Settling time to 0.01%	V_{CC} = ±15 V,	5-V step	Gain = –10		145		ns
		V_{CC} = ±5 V,	2-V step			150		

† Slew rate is measured from an output level range of 25% to 75%.
‡ Full power bandwidth = slew rate / 2π $V_{O(Peak)}$.

noise/distortion performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	$V_{O(pp)}$ = 2 V, f = 1 MHz, Gain = 2	V_{CC} = ±15 V	R_L = 150 Ω		–68		dBc
				R_L = 1 kΩ		–77		
			V_{CC} = ±5 V	R_L = 150 Ω		–69		
				R_L = 1 kΩ		–78		
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz			1.5		nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz			2		pA/√Hz
	Differential gain error	Gain = 2, 40 IRE modulation,	NTSC, ±100 IRE ramp	V_{CC} = ±15 V		0.02%		
				V_{CC} = ±5 V				
	Differential phase error	Gain = 2, 40 IRE modulation,	NTSC, ±100 IRE ramp	V_{CC} = ±15 V		0.08°		
				V_{CC} = ±5 V		0.06°		
X_T	Channel-to-channel crosstalk (THS4022 only)	V_{CC} = ±5 V or ±15 V,	f = 1 MHz			–60		dB

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

dc performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
	Open loop gain	V_{CC} = ±15 V, R_L = 1 kΩ	V_O = ±10 V,	T_A = 25°C	40	60		V/mV
				T_A = full range	35			
		V_{CC} = ±5 V, R_L = 250 Ω	V_O = ±2.5 V,	T_A = 25°C	20	35		V/mV
				T_A = full range	15			
V_{OS}	Input offset voltage	V_{CC} = ±5 V or ±15 V		T_A = 25°C		0.5	2	mV
				T_A = full range			3	
	Offset voltage drift			T_A = full range		15		µV/°C
I_{IB}	Input bias current			T_A = 25°C		3	6	µA
				T_A = full range			6	
I_{OS}	Input offset current			T_A = 25°C		30	250	nA
				T_A = full range			400	
	Offset current drift	T_A = full range				0.3		nA/°C

input characteristics

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V			±13.8	±14.3		V
		V_{CC} = ±5 V			±3.8	±4.3		
CMRR	Common mode rejection ratio	V_{CC} = ±15 V,	V_{ICR} = ±12 V,	T_A = full range	74	95		dB
r_i	Input resistance					1		MΩ
C_i	Input capacitance					1.5		pF

output characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 250 Ω	±12	±12.5		V
		V_{CC} = ±5 V	R_L = 150 Ω	±3	±3.3		
		V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.5		V
		V_{CC} = ±5 V		±3.4	±3.8		
I_O	Output current	V_{CC} = ±15 V	R_L = 20 Ω	80	100		mA
		V_{CC} = ±5 V		50	75		
I_{SC}	Short-circuit current†	V_{CC} = ±15 V			150		mA
R_O	Output resistance†	Open loop			13		Ω

† Observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the absolute maximum ratings section of this data sheet for more information.

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (per amplifier)	V_{CC} = ±15 V	T_A = 25°C		7.8	10	mA
			T_A = full range			11	
		V_{CC} = ±5 V	T_A = 25°C		6.7	9	
			T_A = full range			10.5	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = full range	80	95		dB

TYPICAL CHARACTERISTICS

CROSSTALK vs FREQUENCY

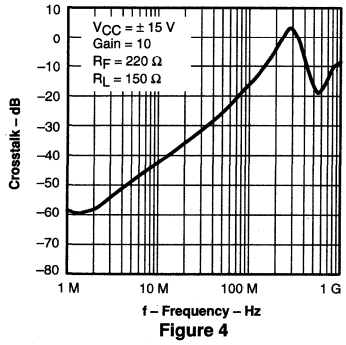


Figure 4

OPEN LOOP GAIN AND PHASE RESPONSE vs FREQUENCY

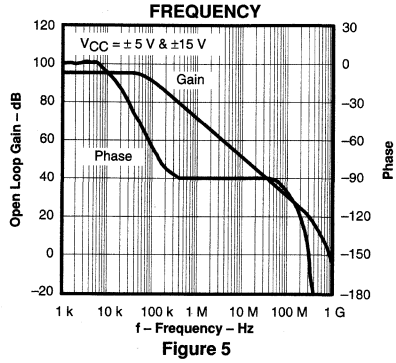


Figure 5

TOTAL HARMONIC DISTORTION vs FREQUENCY

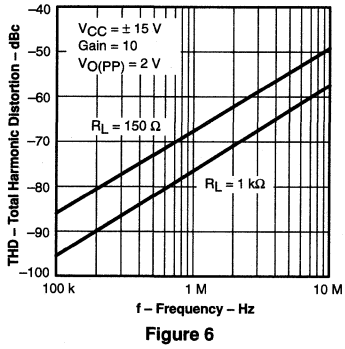


Figure 6

DISTORTION vs OUTPUT VOLTAGE

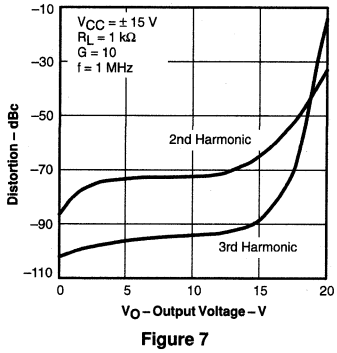


Figure 7

DISTORTION vs OUTPUT VOLTAGE

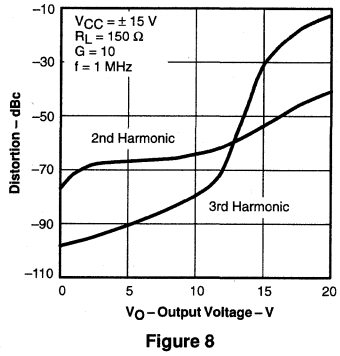


Figure 8

DISTORTION vs FREQUENCY

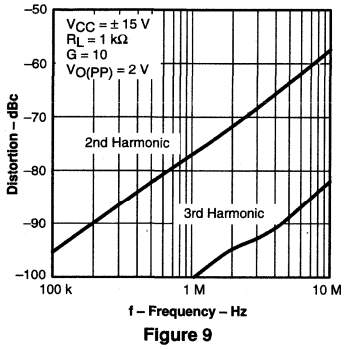


Figure 9

DISTORTION vs FREQUENCY

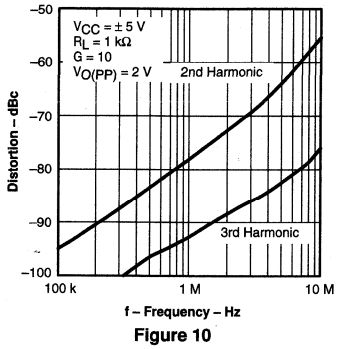


Figure 10

DISTORTION vs FREQUENCY

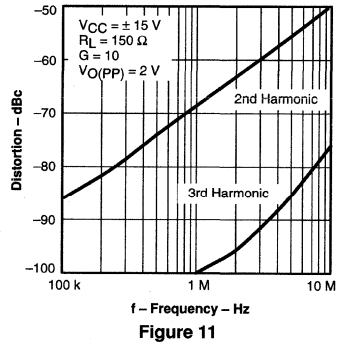


Figure 11

TYPICAL CHARACTERISTICS

DISTORTION vs FREQUENCY

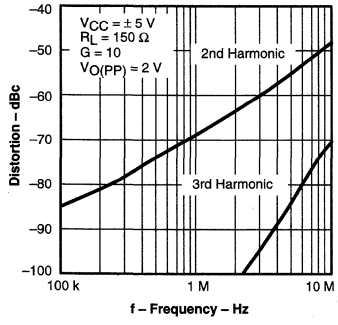


Figure 12

OUTPUT AMPLITUDE vs FREQUENCY

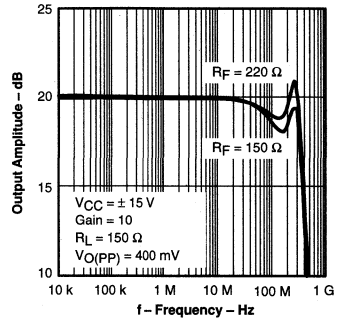


Figure 13

OUTPUT AMPLITUDE vs FREQUENCY

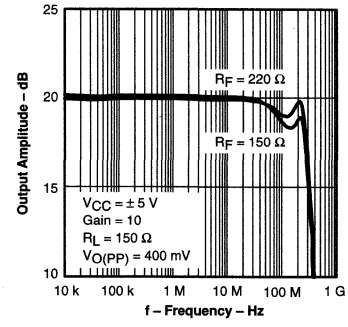


Figure 14

OUTPUT AMPLITUDE vs FREQUENCY

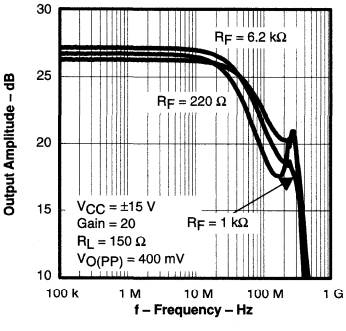


Figure 15

OUTPUT AMPLITUDE vs FREQUENCY

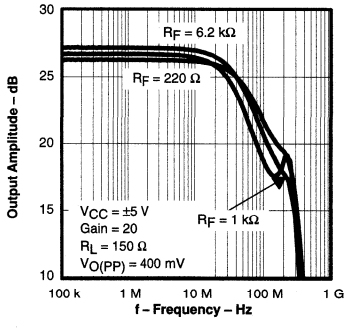


Figure 16

1-V STEP RESPONSE

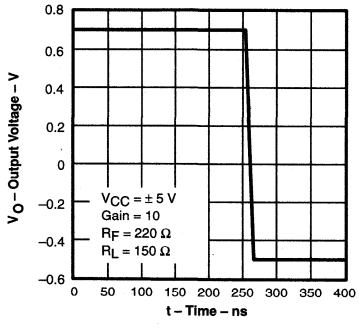


Figure 17

5-V STEP RESPONSE

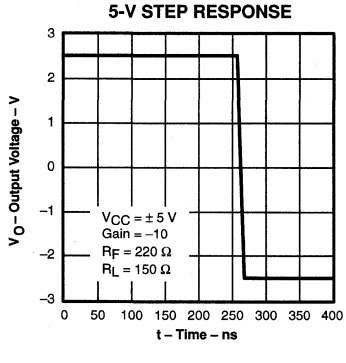


Figure 18

1-V STEP RESPONSE

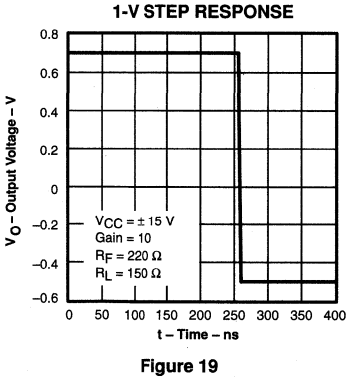


Figure 19

10-V STEP RESPONSE

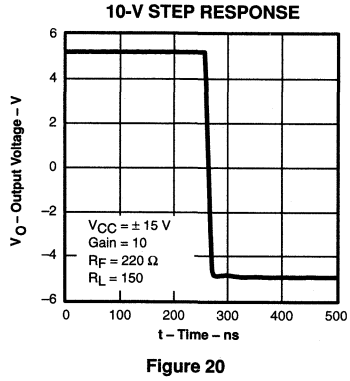


Figure 20

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

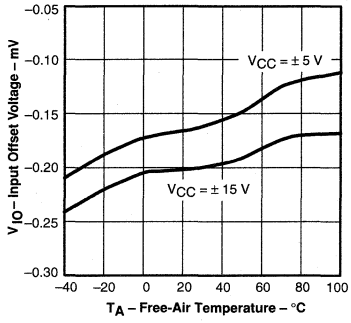


Figure 21

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

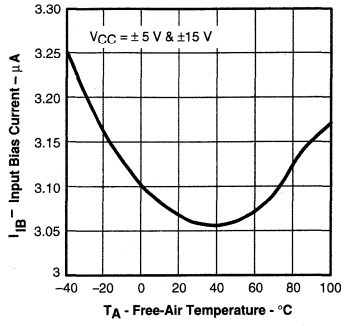


Figure 22

OUTPUT VOLTAGE vs SUPPLY VOLTAGE

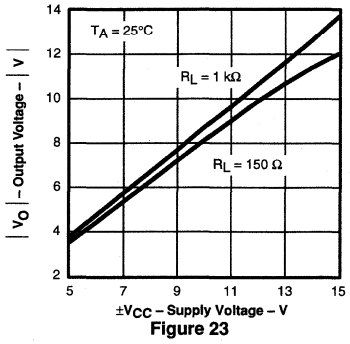


Figure 23

COMMON-MODE INPUT VOLTAGE vs SUPPLY VOLTAGE

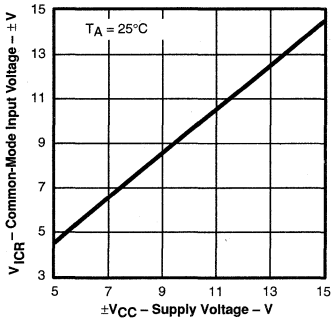


Figure 24

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

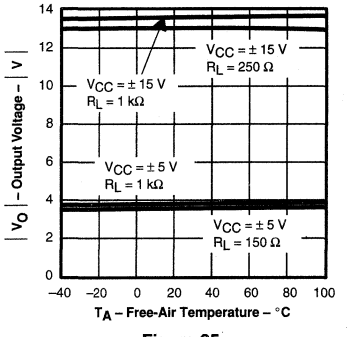


Figure 25

SUPPLY CURRENT vs SUPPLY VOLTAGE

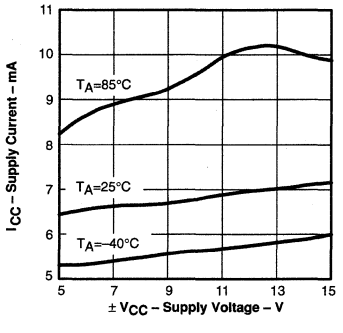


Figure 26

VOLTAGE & CURRENT NOISE vs FREQUENCY

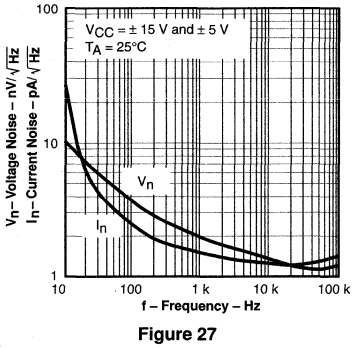


Figure 27

POWER SUPPLY REJECTION RATIO vs FREQUENCY

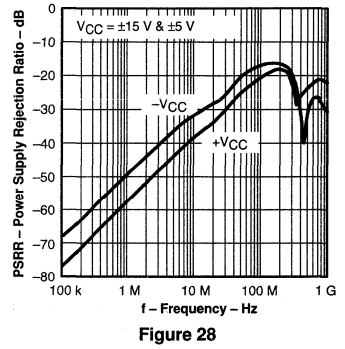


Figure 28

CMRR vs FREQUENCY

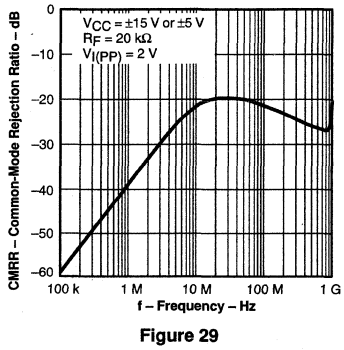


Figure 29

APPLICATION INFORMATION

theory of operation

The THS402x is a high-speed, operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This results in an exceptionally high performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 30.

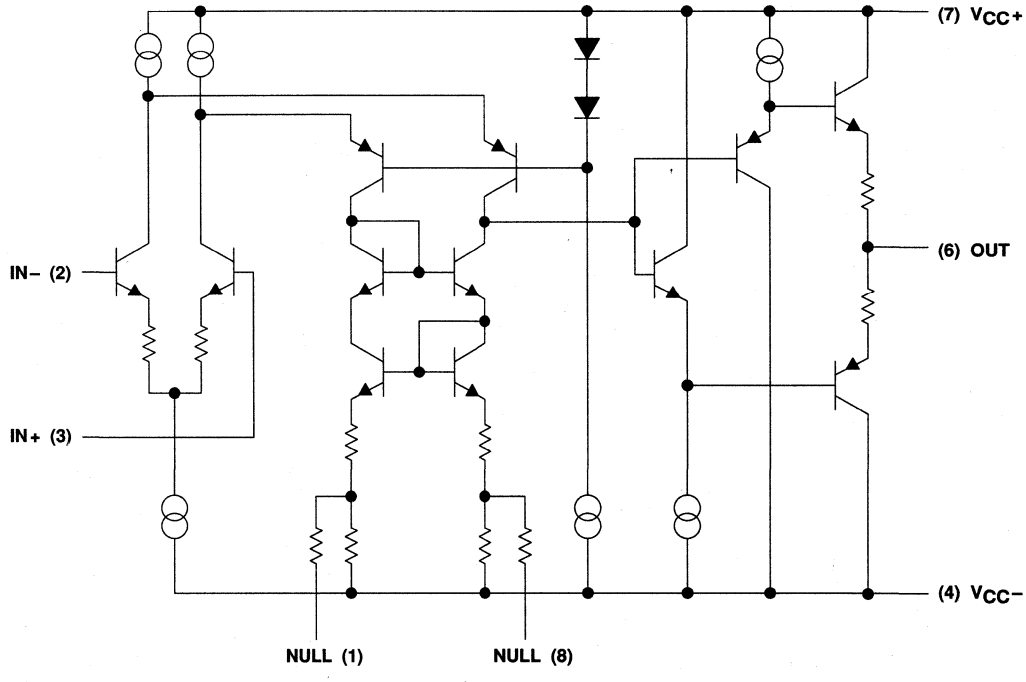


Figure 30. THS4021 Simplified Schematic

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true when amplifying small signals, where signal-to-noise ratio (SNR) is very important. The noise model for the THS402x is shown in Figure 31. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{\text{Hz}}$)
- IN+ = Noninverting current noise (pA/$\sqrt{\text{Hz}}$)
- IN– = Inverting current noise (pA/$\sqrt{\text{Hz}}$)
- e_{Rx} = Thermal voltage noise associated with each resistor ($e_{Rx} = 4\ kTR_x$)

APPLICATION INFORMATION

noise calculations and noise figure (continued)

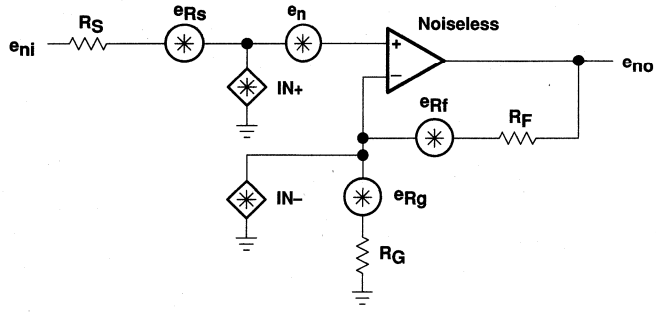


Figure 31. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN+ \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\ kTR_S + 4\ kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\ A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (noninverting case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

For more information on noise analysis, please refer to the *Noise Analysis* section in *Operational Amplifier Circuits Applications Report* (literature number SLVA043).

APPLICATION INFORMATION

noise calculations and noise figure (continued)

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^2}{\left(e_{Rs}\right)^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\ kTR_S}\right]$$

Figure 32 shows the noise figure graph for the THS402x.

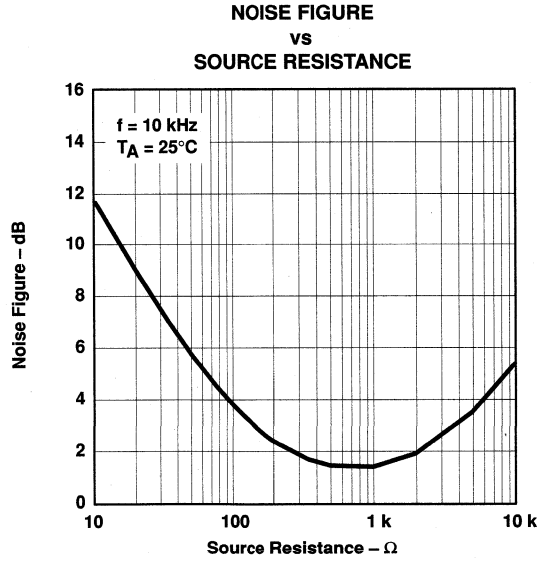


Figure 32. Noise Figure vs Source Resistance

APPLICATION INFORMATION

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS402x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 33. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

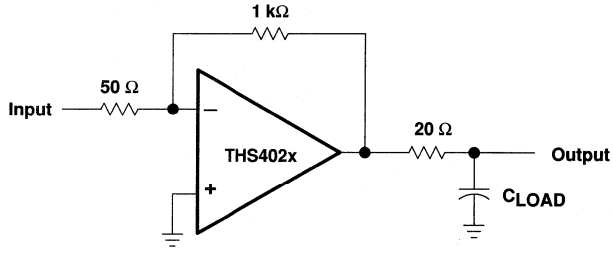


Figure 33. Driving a Capacitive Load

offset nulling

The THS402x has very low input offset voltage for a high-speed amplifier. However, if additional correction is required, an offset nulling function has been provided on the THS4021. The input offset can be adjusted by placing a potentiometer between terminals 1 and 8 of the device and tying the wiper to the negative supply. This is shown in Figure 34.

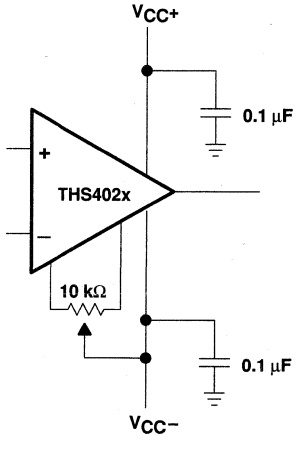
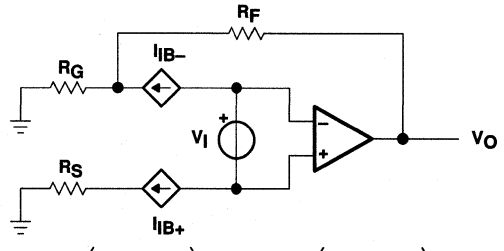


Figure 34. Offset Nulling Schematic

APPLICATION INFORMATION

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

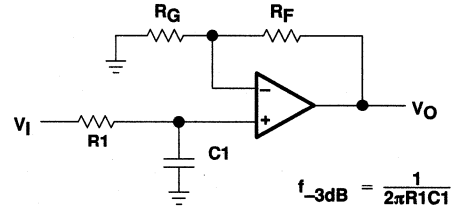


$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\ R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\ R_F$$

Figure 35. Output Offset Voltage Model

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 36).



$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 36. Single-Pole Low-Pass Filter

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high frequency performance of the THS402x, follow proper printed-circuit board high frequency design techniques. A general set of guidelines is given below. In addition, a THS402x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

general PowerPAD design considerations

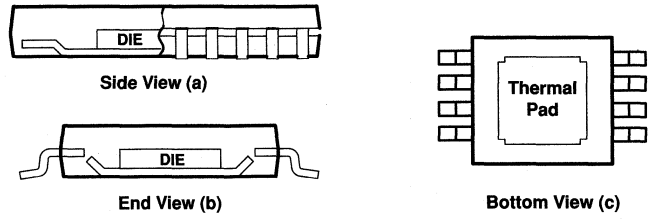
The THS402x is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 37(a) and Figure 37(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 37(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the, heretofore, awkward mechanical methods of heatsinking.

APPLICATION INFORMATION

general PowerPAD design considerations (continued)



NOTE A. The thermal pad is electrically isolated from all terminals in the package.

Figure 37. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach.

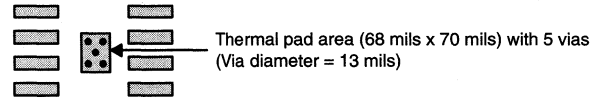


Figure 38. PowerPAD PCB Etch and Via Pattern

1. Prepare the PCB with a top side etch pattern as shown in Figure 38. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS402xDGN IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered, so wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS402xDGN package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the THS402xDGN IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

APPLICATION INFORMATION

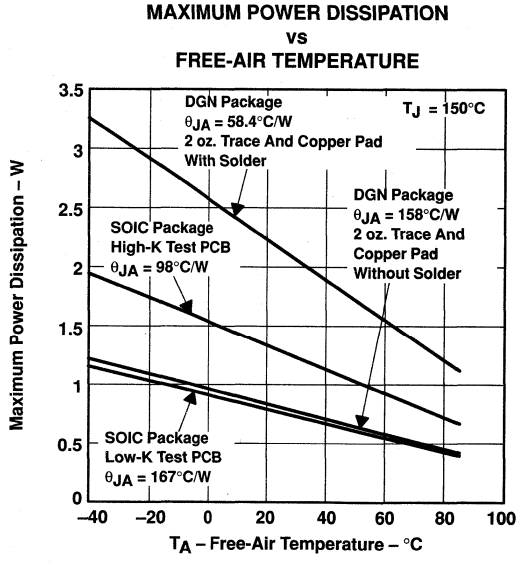
general PowerPAD design considerations (continued)

The actual thermal performance achieved with the THS402xDGN in its PowerPAD package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA}, is about 58.4°C/W. For comparison, the non-PowerPAD version of the THS402x IC (SOIC) is shown. For a given θ_{JA}, the maximum power dissipation is shown in Figure 39 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS402x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A. Results are with no air flow and PCB size = 3"× 3"

Figure 39. Maximum Power Dissipation vs Free-Air Temperature

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multiamplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 40 to Figure 43 show this effect, along with the quiescent heat, with an ambient air temperature of 50°C. Obviously, as the ambient temperature increases, the limit lines shown will drop accordingly. The area under each respective limit line is considered the safe operating area. Any condition above this line will exceed the amplifier's limits and failure may result. When using V_{CC} = ±5 V, there is generally not a heat problem, even with SOIC packages. But, when using V_{CC} = ±15 V, the SOIC package is severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual amplifier package (THS4022), the sum of the RMS output currents and voltages should be used to choose the proper package. The graphs shown assume that both amplifier's outputs are identical.

THS4021
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

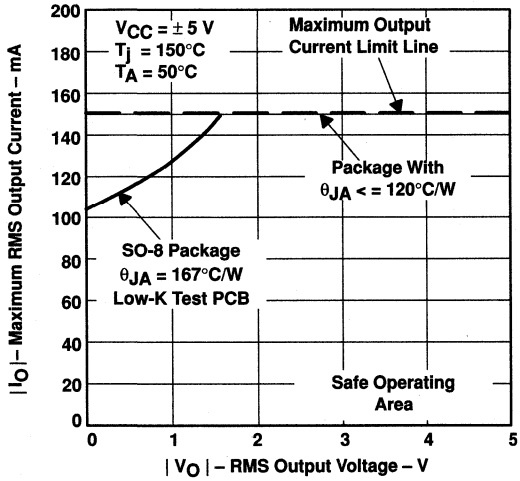


Figure 40

THS4021
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

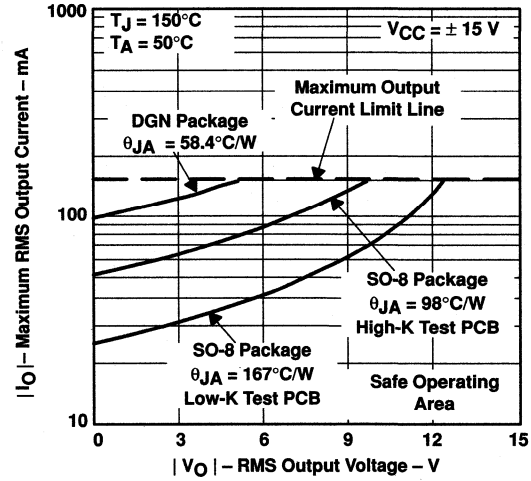


Figure 41

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

THS4022
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

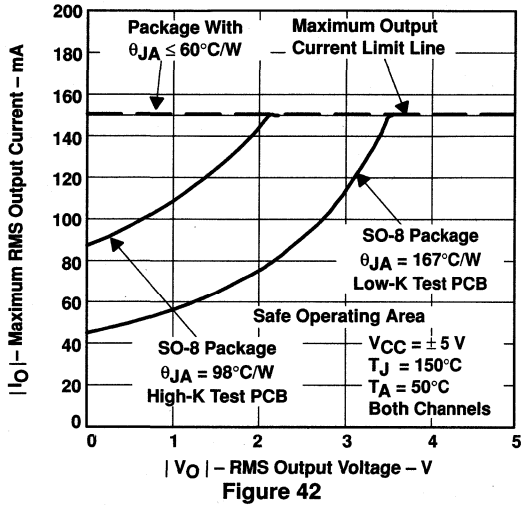


Figure 42

THS4022
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

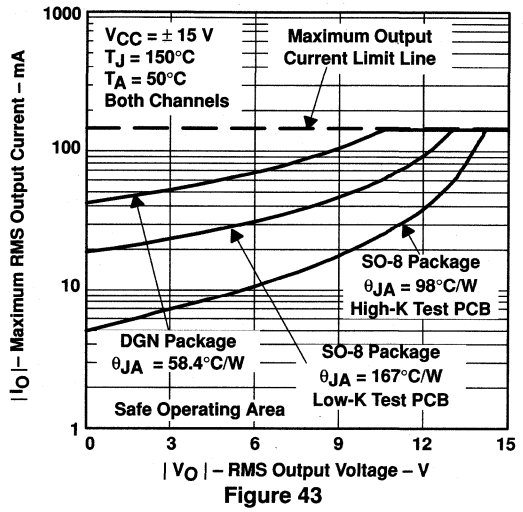


Figure 43

APPLICATION INFORMATION

evaluation board

An evaluation board is available for the THS4021 (literature number SLOP129) and THS4022 (literature number SLOP231). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 44. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. For more information, please refer to the *THS4021 EVM User's Guide* or the *THS4022 EVM User's Guide*. To order the evaluation board, contact your local TI sales office or distributor.

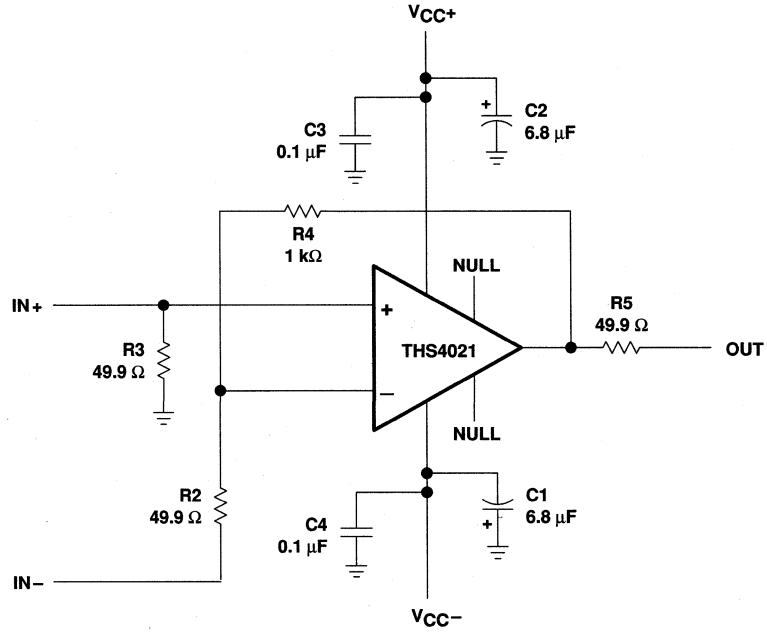
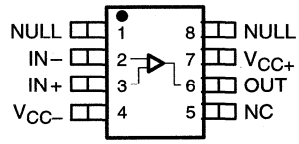


Figure 44. THS4021 Evaluation Board

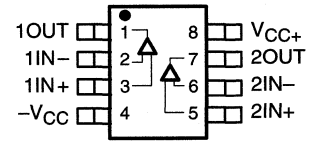
- **Ultra-low 1.6 nV/√Hz Voltage Noise**
- **High Speed**
  - **100 MHz Bandwidth (G = 2 (–1), –3 dB)**
  - **100 V/μs Slew Rate**
- **Stable in Gains of 2 (–1) or greater**
- **Very Low Distortion**
  - **THD = –72 dBc (f = 1 MHz, R_L = 150 Ω)**
  - **THD = –90 dBc (f = 1 MHz, R_L = 1 kΩ)**
- **Low 0.5 mV (Typ) Input Offset Voltage**
- **90 mA Output Current Drive (Typical)**
- **±5 V to ±15 V Typical Operation**
- **Available in Standard SOIC or MSOP PowerPAD™ Package**
- **Evaluation Module Available**

THS4031
D AND DGN PACKAGE
(TOP VIEW)



NC – No internal connection

THS4032
D AND DGN PACKAGE
(TOP VIEW)



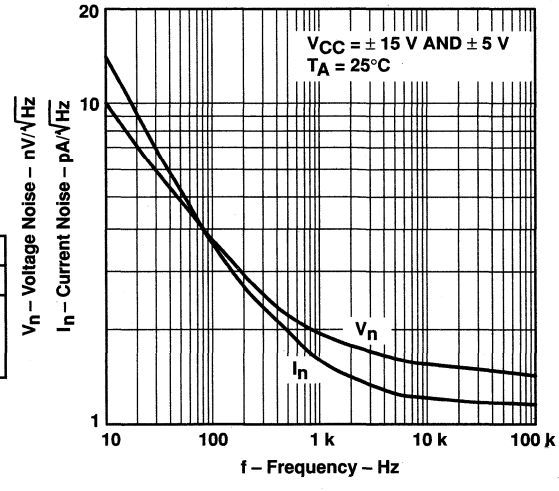
Cross-Section View Showing
PowerPAD Option (DGN)

description

The THS4031 and THS4032 are ultralow voltage noise, high-speed voltage feedback amplifiers that are ideal for applications requiring low voltage noise, including communication and imaging. The single-amplifier THS4031 and the dual-amplifier THS4032 offer very good ac performance with 100-MHz bandwidth, 100-V/μs slew rate, and 60-ns settling time (0.1%). The THS4031 and THS4032 are stable at gains of 2 (–1) or greater. These amplifiers have a high drive capability of 90 mA and draw only 8.5-mA supply current per channel. With total harmonic distortion (THD) of –72 dBc at f = 1 MHz, the THS4031 and THS4032 are ideally suited for applications requiring low distortion.

RELATED DEVICES	
DEVICE	**DESCRIPTION**
THS4011/12	240-MHz Low Distortion High-Speed Amplifiers
THS4021/2	350-MHz Low Noise High-Speed Amplifiers
THS4081/2	175-MHz Low Power High-Speed Amplifiers

VOLTAGE NOISE AND CURRENT NOISE
vs
FREQUENCY



CAUTION: The THS4031 and THS4032 provide ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

PowerPAD is a trademark of Texas Instruments Incorporated.

AVAILABLE OPTIONS

T_A	NUMBER OF CHANNELS	PACKAGED DEVICES			EVALUATION MODULE
		PLASTIC SMALL OUTLINE† (D)	PLASTIC MSOP† (DGN)		
			DEVICE	SYMBOL	
0°C to 70°C	1	THS4031CD	THS4031CDGN	TIACM	THS4031EVM
	2	THS4032CD	THS4032CDGN	TIABD	THS4032EVM
–40°C to 85°C	1	THS4031ID	THS4031IDGN	TIACN	—
	2	THS4032ID	THS4032IDGN	TIABG	—

† The D and DGN packages are available taped and reeled. Add an R suffix to the device type (i.e., THS4031CDGNR).

functional block diagram

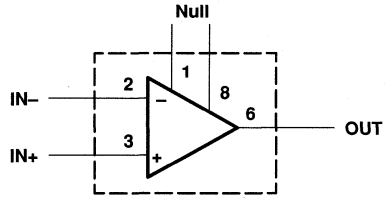


Figure 1. THS4031 – Single Channel

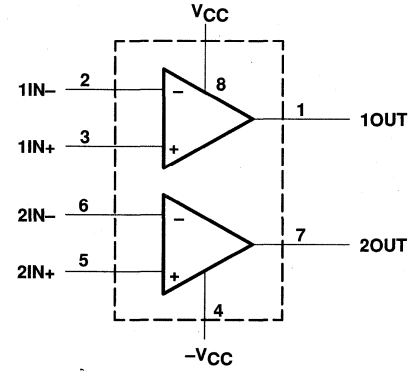


Figure 2. THS4032 – Dual Channel

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC+} to V_{CC-} . . . . . 33 V
Input voltage, V_I . . . . . $\pm V_{CC}$
Output current, I_O . . . . . 150 mA
Differential input voltage, V_{IO} . . . . . ±4 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature, T_A: C-suffix . . . . . 0°C to 70°C
I-suffix . . . . . –40°C to 85°C
Maximum junction temperature, T_J . . . . . 150°C
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING
D	167†	38.3	740 mW
DGN‡	58.4	4.7	2.14 W

† This data was taken using the JEDEC standard Low-K test PCB. For the JEDEC Proposed High-K test PCB, the θ_{JA} is 95°C/W with a power rating at T_A = 25°C of 1.32 W.
‡ This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3-in. × 3-in. PC. For further information, refer to *Application Information* section of this data sheet.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} and V_{CC-}	Dual supply	±4.5		±16	V
	Single supply	9		32	
Operating free-air temperature, T_A	C-suffix	0		70	°C
	I-suffix	–40		85	

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
BW	Small-signal bandwidth (–3 dB)	V_{CC} = ±15 V	Gain = –1 or 2		100		MHz
		V_{CC} = ±5 V			90		
	Bandwidth for 0.1 dB flatness	V_{CC} = ±15 V	Gain = –1 or 2		50		MHz
		V_{CC} = ±5 V			45		
	Full power bandwidth§	$V_{O(pp)}$ = 20 V, V_{CC} = ±15 V	R_L = 1 kΩ		1.6		MHz
		$V_{O(pp)}$ = 5 V, V_{CC} = ±5 V			5		
SR	Slew rate‡	V_{CC} = ±15 V, 20-V step	Gain = –1		100		V/μs
		V_{CC} = ±5 V, 5-V step			80		
t_s	Settling time to 0.1%	V_{CC} = ±15 V, 5-V step	Gain = –1		60		ns
		V_{CC} = ±5 V, 2.5-V step			45		
	Settling time to 0.01%	V_{CC} = ±15 V, 5-V step	Gain = –1		90		ns
		V_{CC} = ±5 V, 2.5-V step			80		

† Full range = 0°C to 70°C for the THS403xC and –40°C to 85°C for the THS403xI.
‡ Slew rate is measured from an output level range of 25% to 75%.
§ Full power bandwidth = slew rate/2 $\pi V_{O(Peak)}$.

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

noise/distortion performance

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	THS4031	V_{CC} = ±5 V or ±15 V, $V_{O(pp)}$ = 2 V, f = 1 MHz, Gain = 2	R_L = 150 Ω		–81		dBc
				R_L = 1 kΩ		–96		
		THS4032		R_L = 150 Ω		–72		
				R_L = 1 kΩ		–90		
V_n	Input voltage noise		V_{CC} = ±5 V or ±15 V, f = 10 kHz			1.6		nV/√Hz
I_n	Input current noise		V_{CC} = ±5 V or ±15 V, f = 10 kHz			1.2		pA/√Hz

Differential gain error	Gain = 2, 40 IRE modulation, NTSC and PAL, ±100 IRE ramp	V_{CC} = ±15 V	0.015%		
		V_{CC} = ±5 V	0.02%		
Differential phase error		V_{CC} = ±15 V	0.025°		
		V_{CC} = ±5 V	0.03°		
Channel-to-channel crosstalk (THS4032 only)	V_{CC} = ±5 V or ±15 V, f = 1 MHz		–61		dBc

† Full range = 0°C to 70°C for the THS403xC and –40°C to 85°C for the THS403xI.

dc performance

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
	Open loop gain	V_{CC} = ±15 V, R_L = 1 kΩ, V_O = ±10 V		T_A = 25°C	45	75		V/mV
				T_A = full range	40			
		V_{CC} = ±5 V, R_L = 1 kΩ, V_O = ±2.5 V		T_A = 25°C	35	55		
				T_A = full range	30			
V_{OS}	Input offset voltage	V_{CC} = ±5 V or ±15 V		T_A = 25°C		0.5	2	mV
				T_A = full range			3	
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V		T_A = 25°C		3	6	µA
				T_A = full range			8	
I_{OS}	Input offset current	V_{CC} = ±5 V or ±15 V		T_A = 25°C		30	250	nA
				T_A = full range			400	
	Offset voltage drift	V_{CC} = ±5 V or ±15 V		T_A = full range		10		µV/°C
	Input offset current drift	V_{CC} = ±5 V or ±15 V		T_A = full range		0.2		nA/°C

† Full range = 0°C to 70°C for the THS403xC and –40°C to 85°C for the THS403xI.

input characteristics

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V			±13.5	±14.3		V
		V_{CC} = ±5 V			±3.8	±4.3		
CMRR	Common mode rejection ratio	V_{CC} = ±15 V,	V_{ICR} = ±12 V	T_A = 25°C	85	95		dB
				T_A = full range	80			
		V_{CC} = ±5 V,	V_{ICR} = ±2.5 V	T_A = 25°C	90	100		
				T_A = full range	85			
r_i	Input resistance					2		MΩ
C_i	Input capacitance					1.5		pF

† Full range = 0°C to 70°C for the THS403xC and –40°C to 85°C for the THS403xI.

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

output characteristics

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.6		V
		V_{CC} = ±5 V		±3.4	±3.8		
		V_{CC} = ±15 V	R_L = 250 Ω	±12	±12.9		
		V_{CC} = ±5 V	R_L = 150 Ω	±3	±3.5		
I_O	Output current‡	V_{CC} = ±15 V	R_L = 20 Ω	60	90		mA
		V_{CC} = ±5 V		50	70		
I_{SC}	Short-circuit current‡	V_{CC} = ±15 V			150		mA
R_O	Output resistance	Open loop			13		Ω

† Full range = 0°C to 70°C for the THS403xC and –40°C to 85°C for the THS403xI.

‡ Observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the absolute maximum ratings section of this data sheet for more information.

power supply

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (each amplifier)	V_{CC} = ±15 V	T_A = 25°C		8.5	10	mA
			T_A = full range			11	
		V_{CC} = ±5 V	T_A = 25°C		7.5	9	
			T_A = full range			10.5	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	85	95		dB
			T_A = full range	80			

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

PARAMETER MEASUREMENT INFORMATION

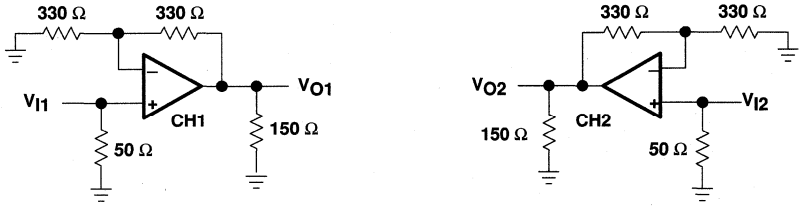


Figure 3. THS4032 Crosstalk Test Circuit

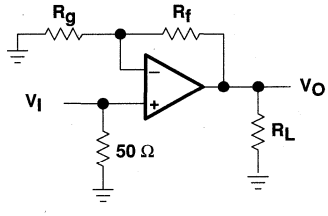


Figure 4. Step Response Test Circuit

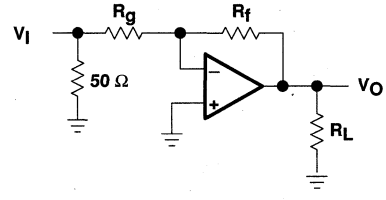


Figure 5. Step Response Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Input offset voltage distribution		6, 7
V_{IO}	Input offset voltage	vs Free-air temperature	8
I_{IB}	Input bias current	vs Free-air temperature	9
V_O	Output voltage swing	vs Supply voltage	10
V_{OM}	Maximum output voltage swing	vs Free-air temperature	11
I_O	Maximum output current	vs Free-air temperature	12
I_{CC}	Supply current	vs Free-air temperature	13
V_{IC}	Common-mode input voltage	vs Supply voltage	14
Z_O	Closed-loop output impedance	vs Frequency	15
	Open-loop gain		16
	Phase response		
PSRR	Power-supply rejection ratio	vs Frequency	17
CMRR	Common-mode rejection ratio	vs Frequency	18
	Crosstalk	vs Frequency	19
	Harmonic distortion	vs Frequency	20, 21
	Harmonic distortion	vs Peak-to-peak output voltage	22, 23
SR	Slew rate	vs Free-air temperature	24
	0.1% settling time	vs Output voltage step size	25
	Output amplitude	vs Frequency	26 – 30
	Small and large signal frequency response		31 – 34
	Differential phase	vs Number of 150-Ω loads	35, 36
	Differential gain	vs Number of 150-Ω loads	37, 38
	1-V step response		39, 40
	4-V step response		41
	20-V step response		42

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE DISTRIBUTION

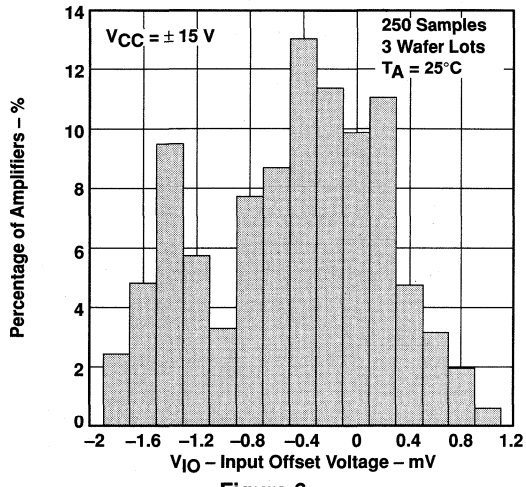


Figure 6

INPUT OFFSET VOLTAGE DISTRIBUTION

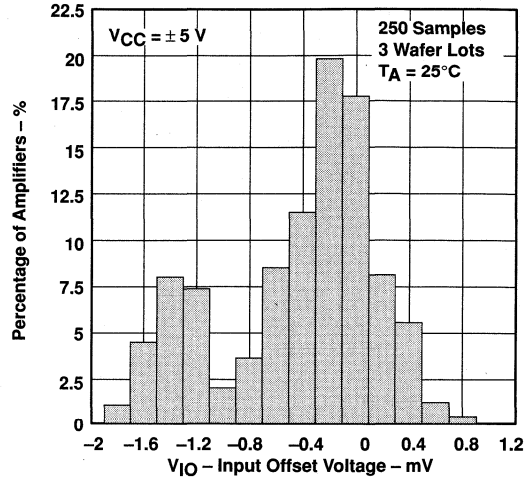


Figure 7

INPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

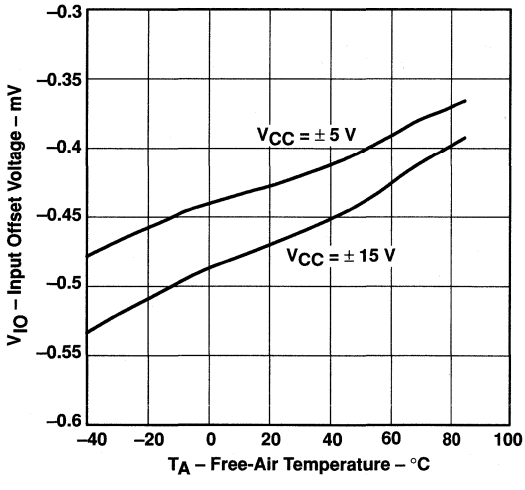


Figure 8

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

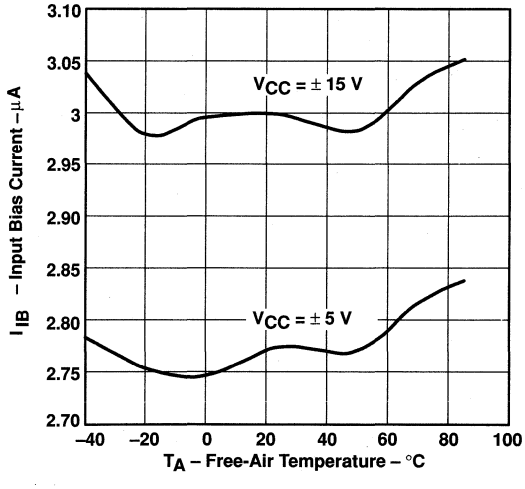


Figure 9

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

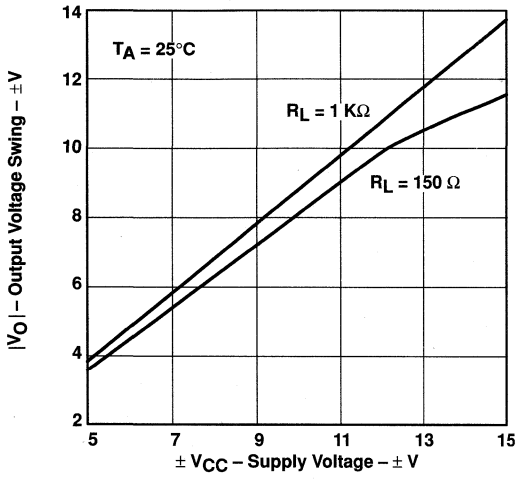


Figure 10

MAXIMUM OUTPUT VOLTAGE SWING vs FREE–AIR TEMPERATURE

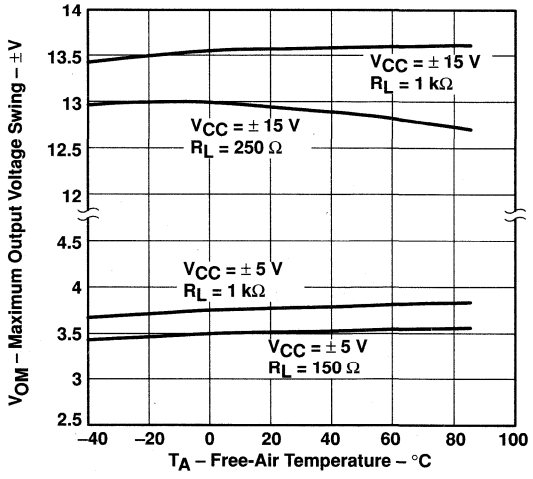


Figure 11

MAXIMUM OUTPUT CURRENT vs FREE-AIR TEMPERATURE

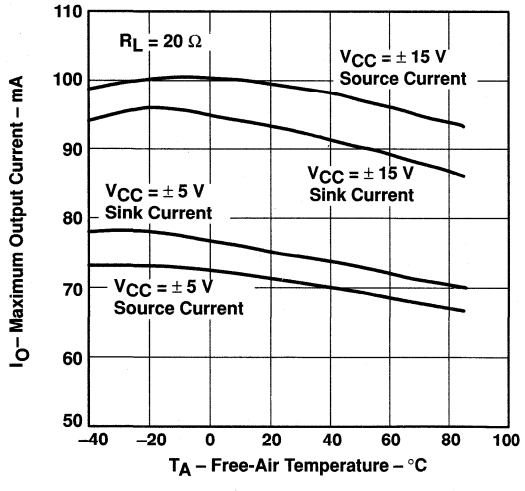


Figure 12

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

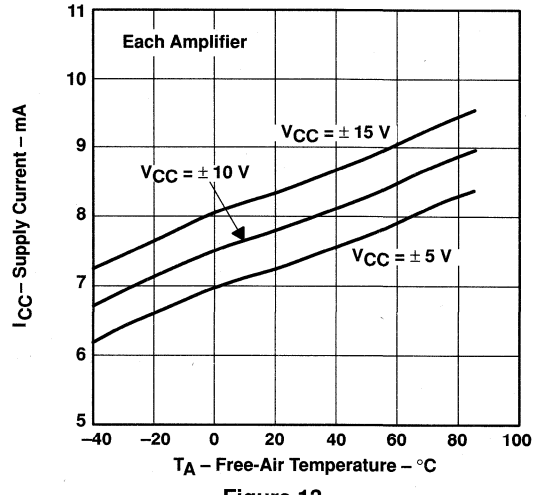


Figure 13

TYPICAL CHARACTERISTICS

COMMON-MODE INPUT VOLTAGE
vs
SUPPLY VOLTAGE

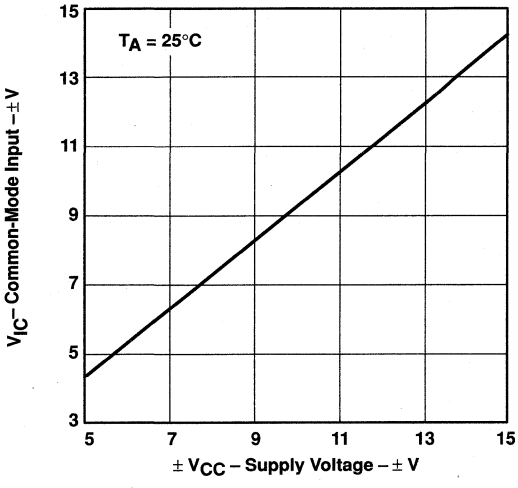


Figure 14

CLOSED-LOOP OUTPUT IMPEDANCE
vs
FREQUENCY

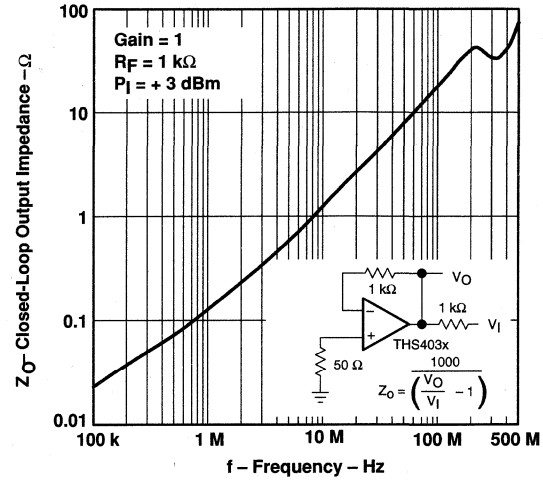


Figure 15

OPEN-LOOP GAIN AND PHASE RESPONSE

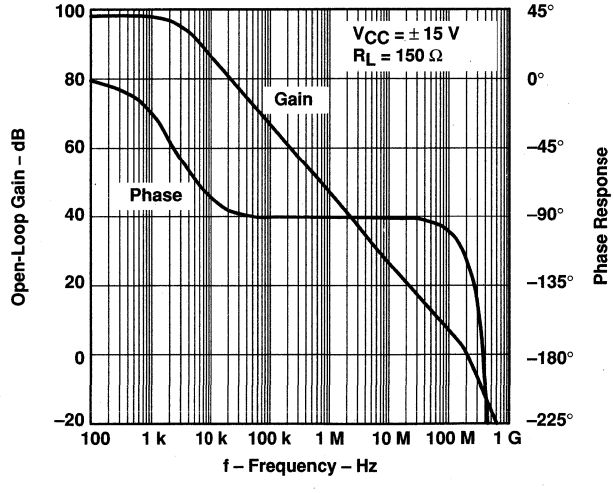


Figure 16

TYPICAL CHARACTERISTICS

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

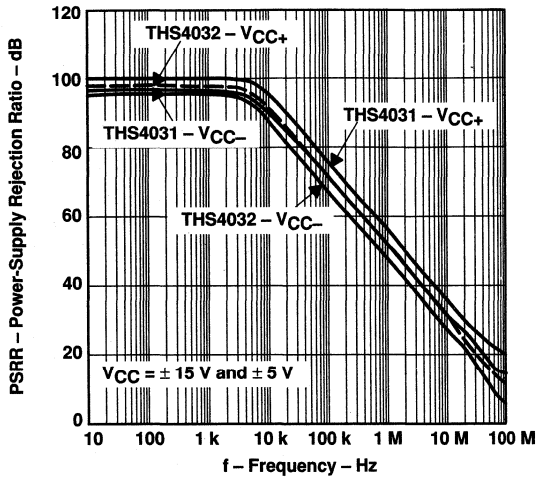


Figure 17

COMMON-MODE REJECTION RATIO vs FREQUENCY

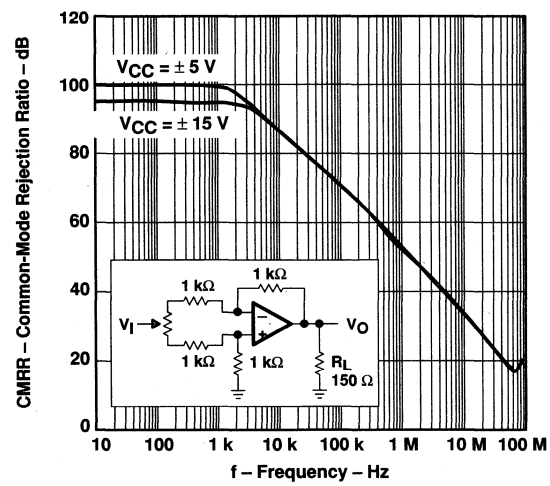


Figure 18

THS4032 CROSSTALK vs FREQUENCY

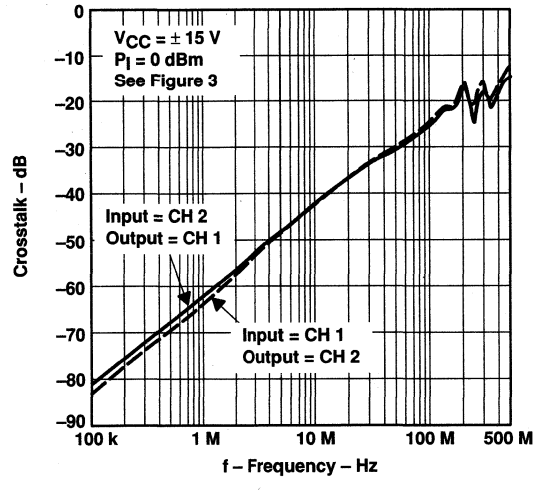


Figure 19

TYPICAL CHARACTERISTICS

HARMONIC DISTORTION
vs
FREQUENCY

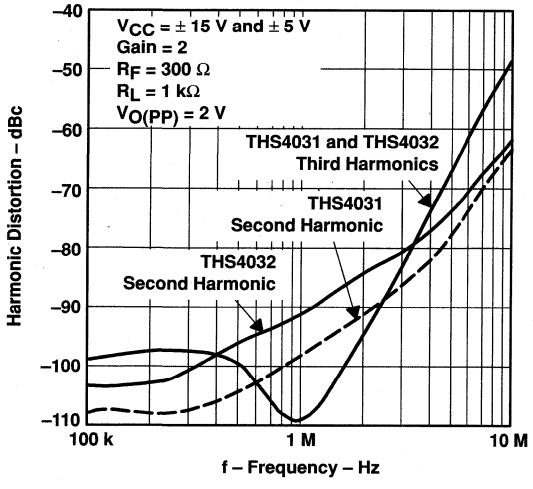


Figure 20

HARMONIC DISTORTION
vs
FREQUENCY

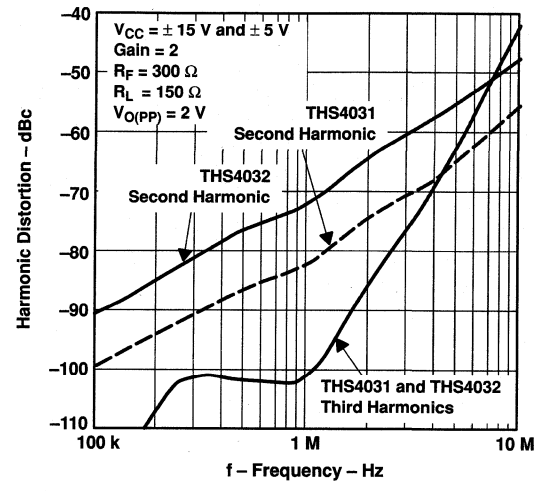


Figure 21

HARMONIC DISTORTION
vs
PEAK-TO-PEAK OUTPUT VOLTAGE

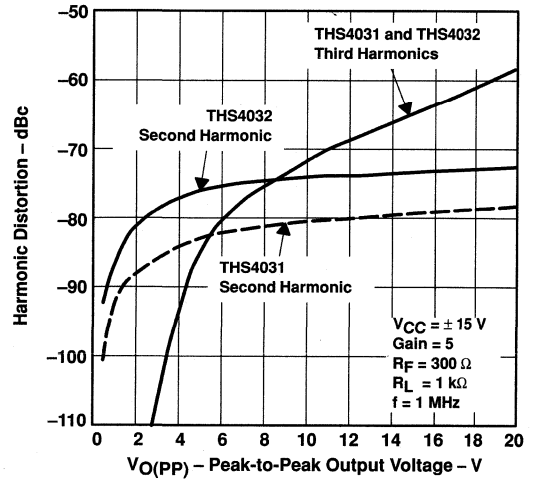


Figure 22

HARMONIC DISTORTION
vs
PEAK-TO-PEAK OUTPUT VOLTAGE

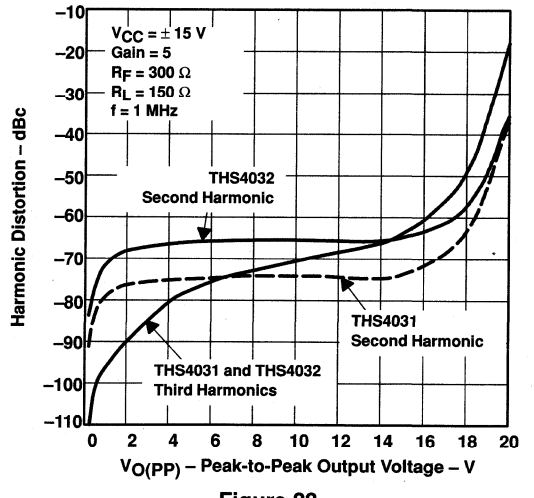


Figure 23

TYPICAL CHARACTERISTICS

SLEW RATE vs FREE-AIR TEMPERATURE

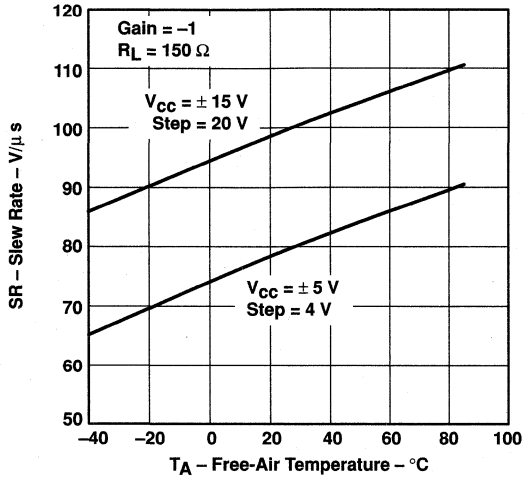


Figure 24

0.1% SETTLING TIME vs STEP SIZE

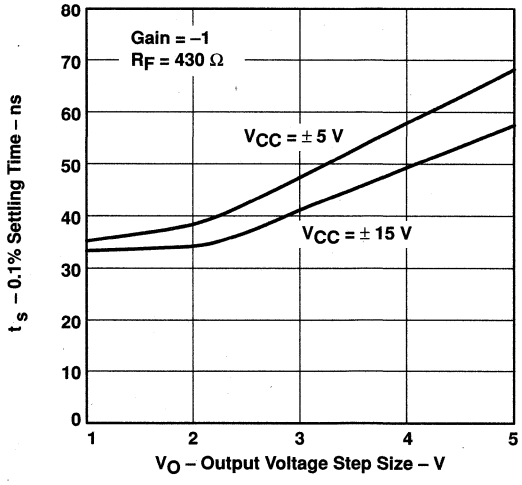


Figure 25

OUTPUT AMPLITUDE vs FREQUENCY

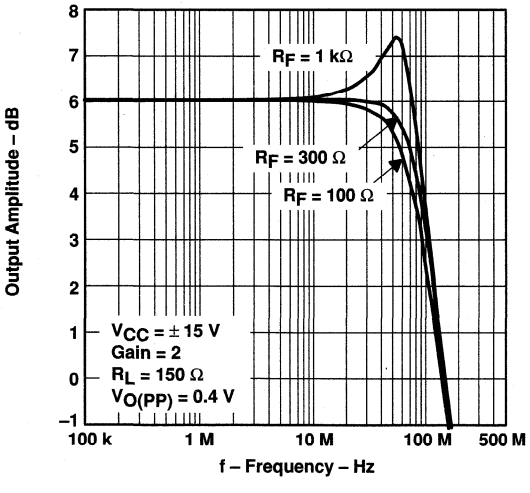


Figure 26

OUTPUT AMPLITUDE vs FREQUENCY

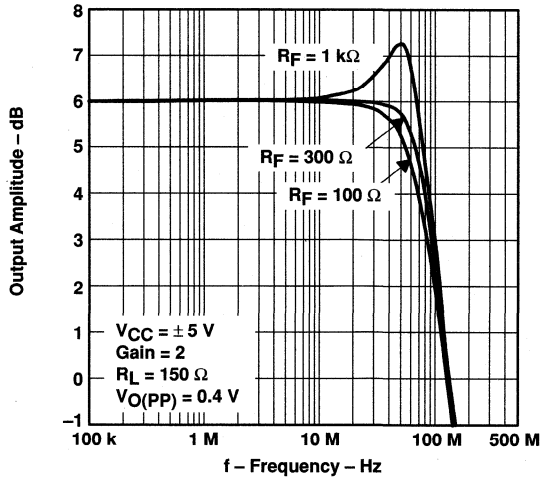


Figure 27

TYPICAL CHARACTERISTICS

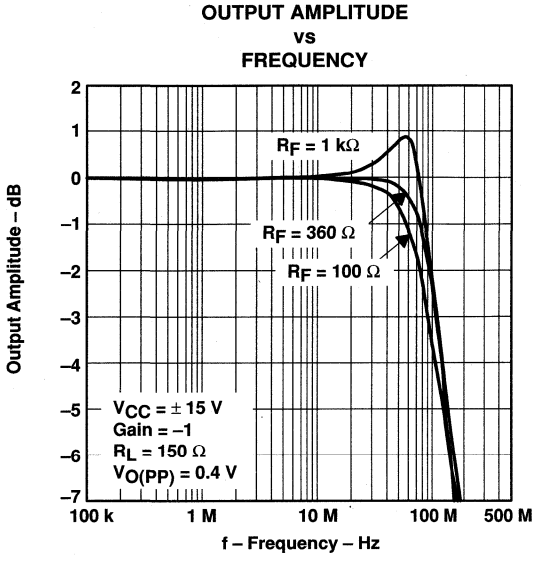


Figure 28

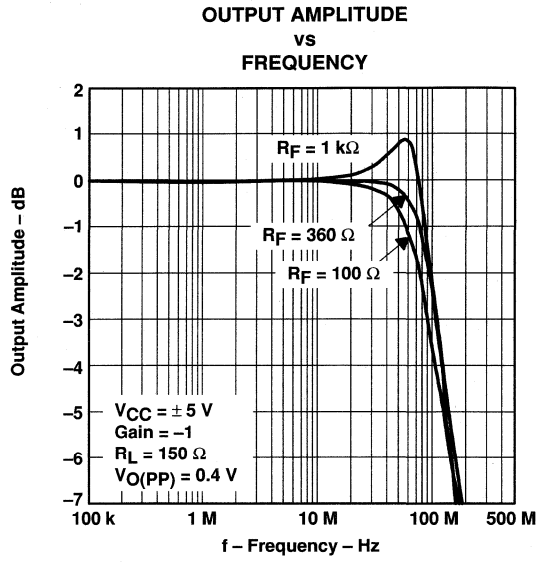


Figure 29

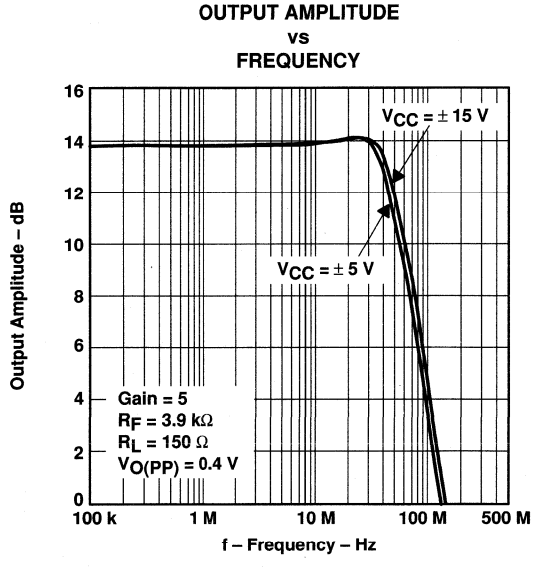


Figure 30

TYPICAL CHARACTERISTICS

SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

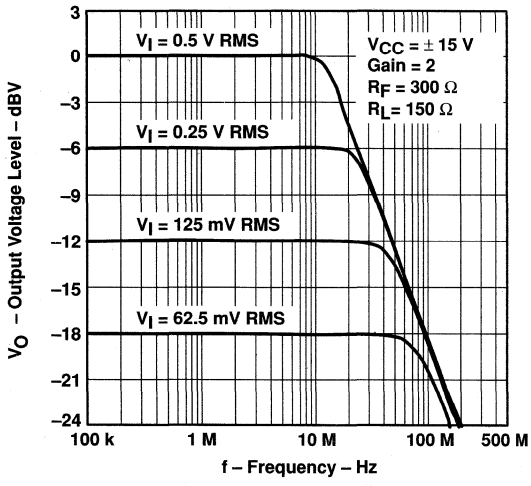


Figure 31

SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

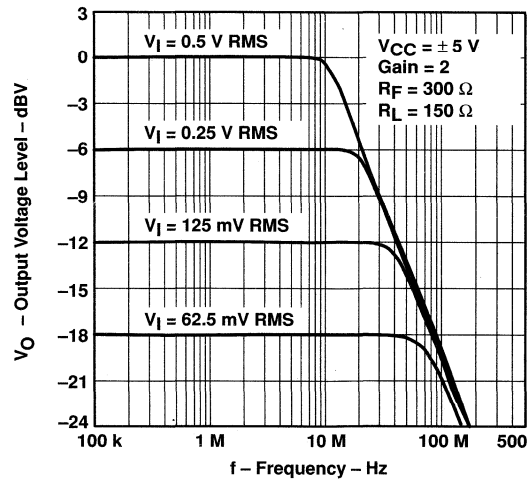


Figure 32

SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

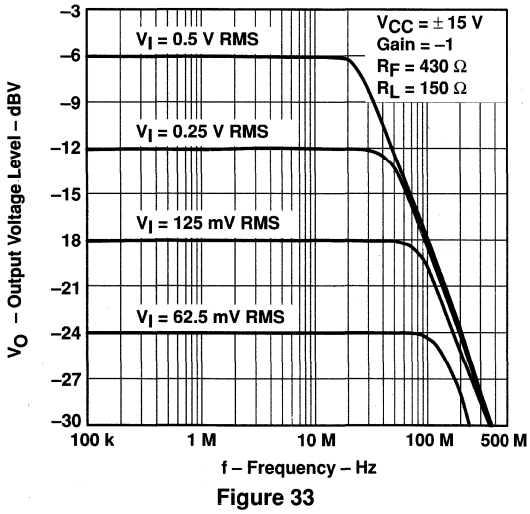


Figure 33

SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

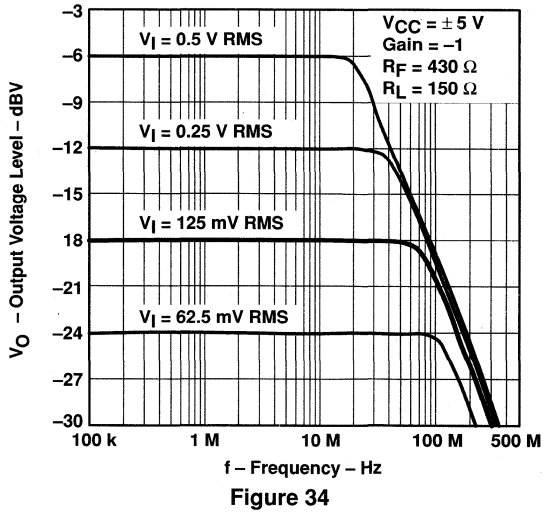


Figure 34

TYPICAL CHARACTERISTICS

DIFFERENTIAL PHASE
vs
NUMBER OF 150-Ω LOADS

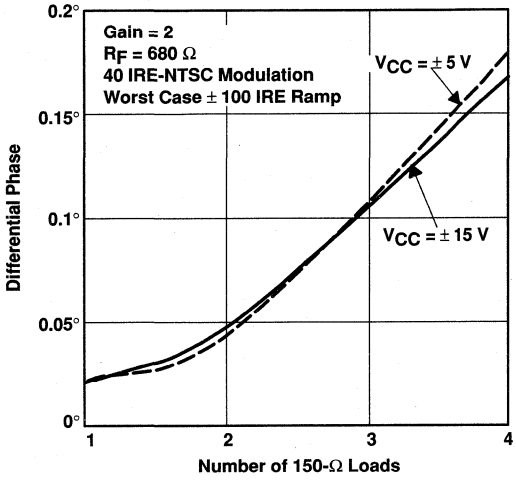


Figure 35

DIFFERENTIAL PHASE
vs
NUMBER OF 150-Ω LOADS

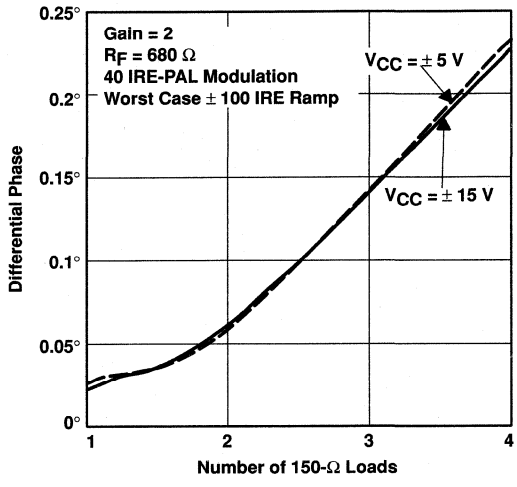


Figure 36

DIFFERENTIAL GAIN
vs
NUMBER OF 150-Ω LOADS

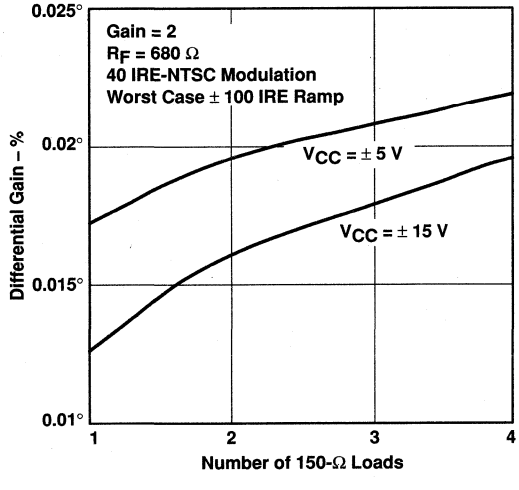


Figure 37

DIFFERENTIAL GAIN
vs
NUMBER OF 150-Ω LOADS

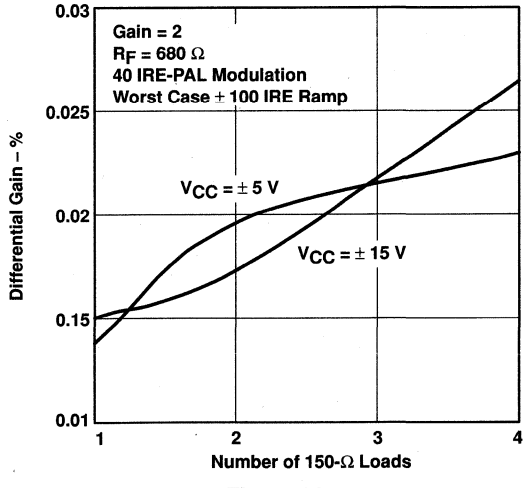


Figure 38

TYPICAL CHARACTERISTICS

1-V STEP RESPONSE

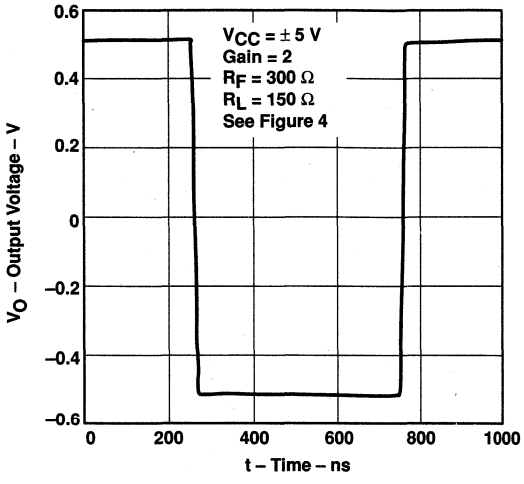


Figure 39

1-V STEP RESPONSE

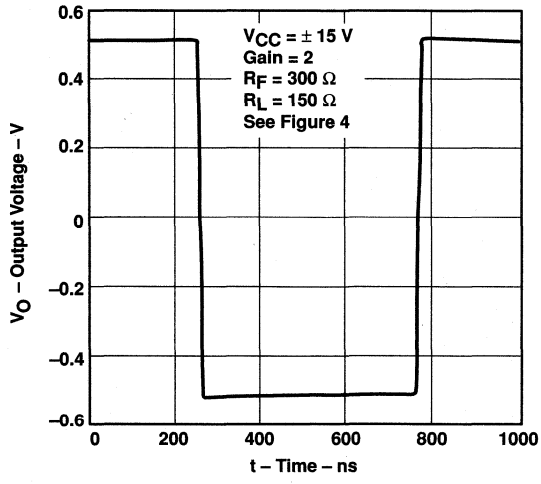


Figure 40

4-V STEP RESPONSE

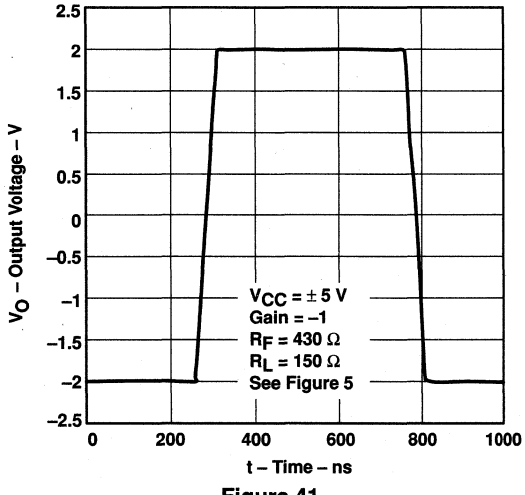


Figure 41

20-V STEP RESPONSE

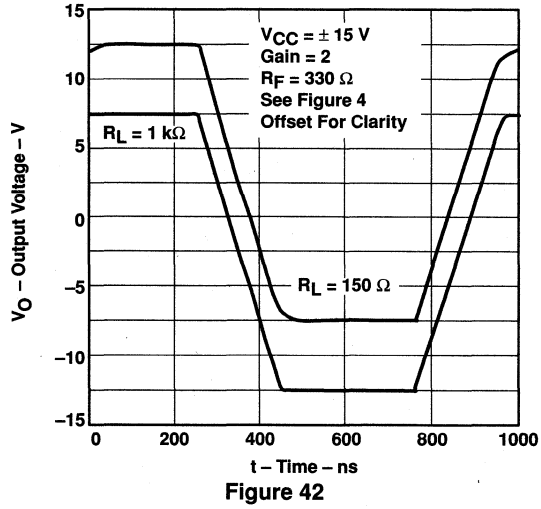


Figure 42

APPLICATION INFORMATION

theory of operation

The THS403x is a high-speed operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This results in an exceptionally high-performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 43.

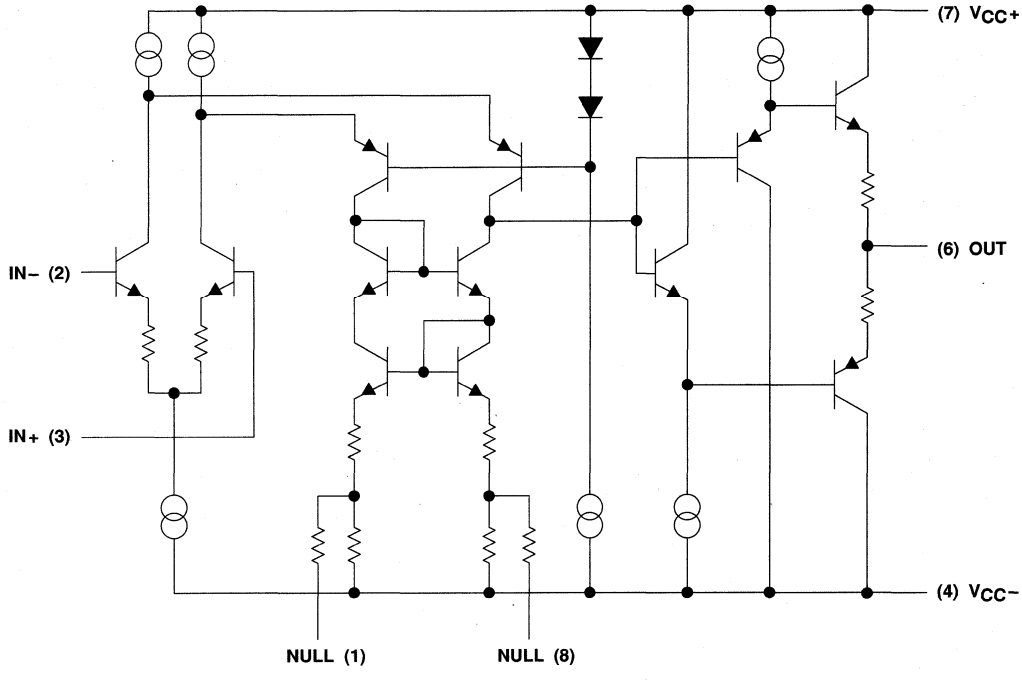


Figure 43. THS4031 Simplified Schematic

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true when amplifying small signals. The noise model for the THS403x, shown in Figure 44, includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{\text{Hz}}$)
- IN+ = Noninverting current noise (pA/$\sqrt{\text{Hz}}$)
- IN– = Inverting current noise (pA/$\sqrt{\text{Hz}}$)
- e_{Rx} = Thermal voltage noise associated with each resistor ($e_{Rx} = 4\ kTR_x$)

APPLICATION INFORMATION

noise calculations and noise figure (continued)

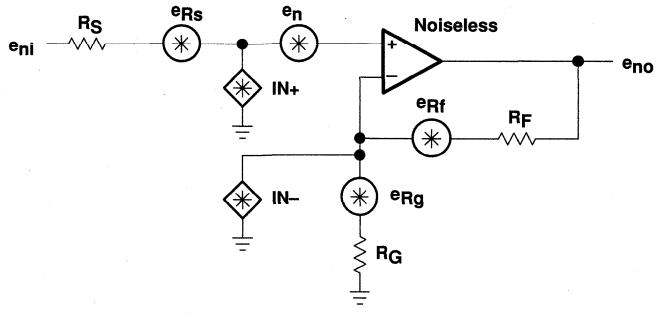


Figure 44. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN + \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\ kTR_s + 4\ kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\ A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)}$$

As the previous equations show, to keep noise at a minimum, small-value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This advantage can greatly simplify the formula and make noise calculations much easier to calculate.

For more information on noise analysis, please refer to the *Noise Analysis* section in *Operational Amplifier Circuits Applications Report* (literature number SLVA043).

APPLICATION INFORMATION

noise calculations and noise figure (continued)

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^2}{\left(e_{Rs}\right)^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\ kTR_S}\right]$$

Figure 45 shows the noise figure graph for the THS403x.

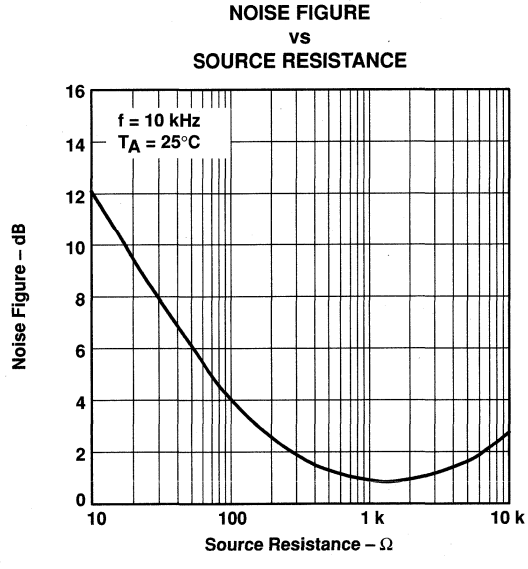


Figure 45. Noise Figure vs Source Resistance

APPLICATION INFORMATION

optimizing frequency response

Internal frequency compensation of the THS403x was selected to provide very wide bandwidth performance and still maintain a very low noise floor. In order to meet these performance requirements, the THS403x must have a minimum gain of 2 (–1). Because everything is referred to the noninverting terminal of an operational amplifier, the noise gain in a G = –1 configuration is the same as a G = 2 configuration.

One of the keys to maintaining a smooth frequency response, and hence, a stable pulse response, is to pay particular attention to the inverting terminal. Any stray capacitance at this node causes peaking in the frequency response (see Figure 46 and Figure 47). Two things can be done to help minimize this effect. The first is to simply remove any ground planes under the inverting terminal of the amplifier, including the trace that connects to this terminal. Additionally, the length of this trace should be minimized. The capacitance at this node causes a lag in the voltage being fed back due to the charging and discharging of the stray capacitance. If this lag becomes too long, the amplifier will not be able to correctly keep the noninverting terminal voltage at the same potential as the inverting terminal's voltage. Peaking and possible oscillations will then occur if this happens.

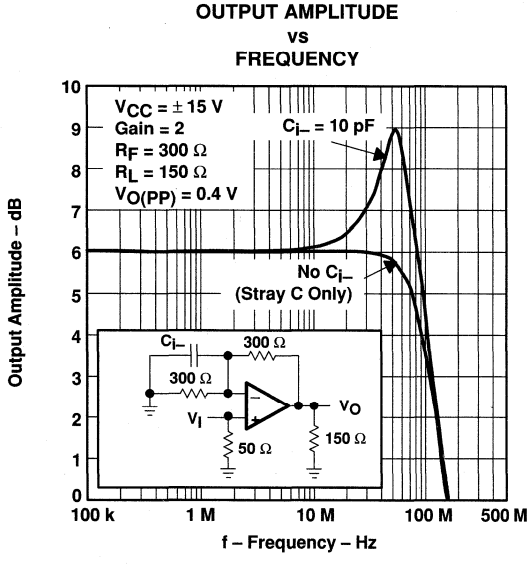


Figure 46

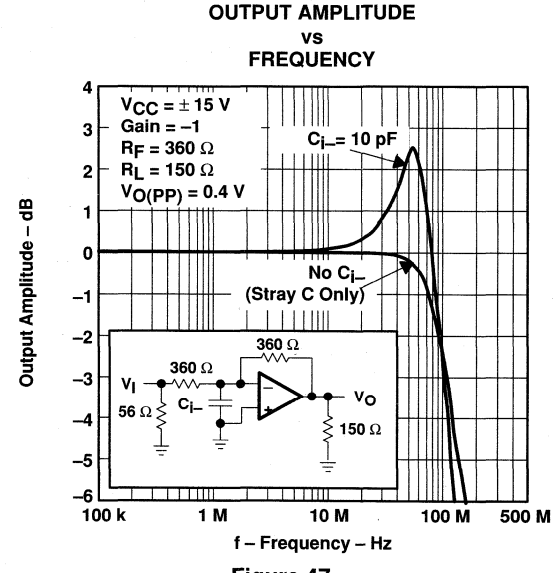


Figure 47

The second precaution to help maintain a smooth frequency response is to keep the feedback resistor (R_f) and the gain resistor (R_g) values fairly low. These two resistors are effectively in parallel when looking at the ac small-signal response. This is why in Figure 30, a feedback resistor of 3.9 kΩ with a gain resistor of 1 kΩ only shows a small peaking in the frequency response. The parallel resistance is only 800 Ω. This value, in conjunction with a very small stray capacitance test PCB, forms a zero on the edge of the amplifier's natural frequency response. To eliminate this peaking, all that needs to be done is to reduce the feedback and gain resistances. One other way to compensate for this stray capacitance is to add a small capacitor in parallel with the feedback resistor. This helps to neutralize the effects of the stray capacitance. To keep this peaking out of the operating range, the stray capacitance and resistor value's time constant must be kept low. But, as can be seen in Figures 26 – 29, a value too low starts to reduce the bandwidth of the amplifier. Table 1 shows some recommended feedback resistors to be used with the THS403x.

APPLICATION INFORMATION

optimizing frequency response (continued)

Table 1. Recommended Feedback Resistors

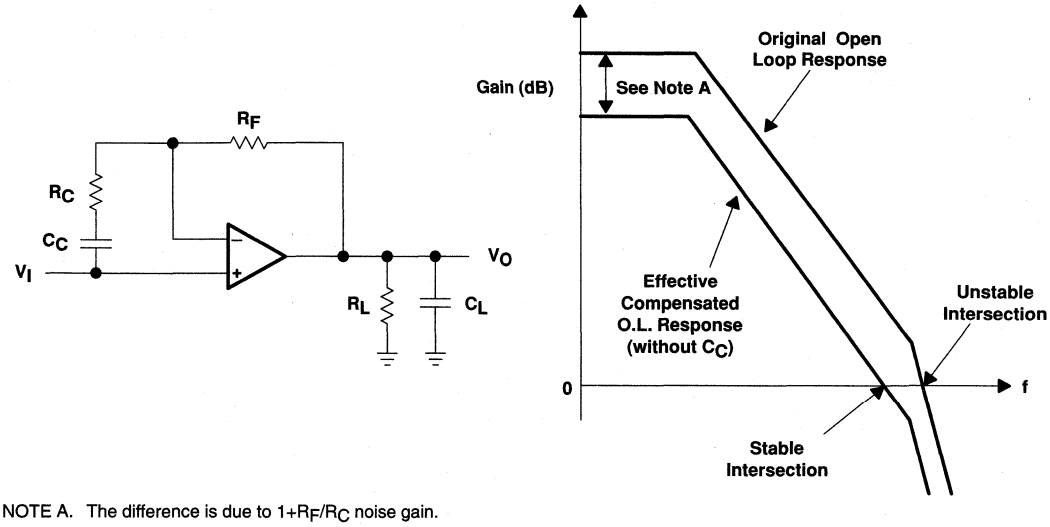
GAIN	R_f for V_{CC} = ±15 V and ± 5 V
2	300 Ω
–1	360 Ω
5	3.3 kΩ (low stray-c PCB only)

unity-gain concerns

THS403x was designed for extremely low noise with a minimum gain of 2 (–1). If the amplifier were to be configured for unity gain, the output would tend to oscillate because the open-loop intersection on a Bode diagram is at a –40 dB/decade slope instead of the –20 dB/decade slope required for stable operation. But, it is sometimes desirable to have a low-noise unity gain buffer. There is a way to accomplish this feat with the THS403x with some added complexity (see Figure 48). The lag compensation circuit shown in Figure 48 increases the noise gain of the amplifier without increasing the signal gain. Another way to look at this is that the open-loop gain is effectively reduced by the 1 + R_F/R_C gain. This reduction causes the –40 dB/decade pole to be shifted down into an open-loop gain of less than 1. The drawbacks of this circuit are the decreased frequency response, the increased noise, and the increased output offset voltage (V_{OO}). One way to eliminate the V_{OO} increase is to add a capacitor (C_C) in series with R_C, with the added requirement that the time constant of C_C and R_C be set low enough for the Bode plot intersection to be at a –20 dB/decade slope. Typically, a 1 + R_F/R_C gain of 2 to 3 yields a smooth frequency response for the THS403x. If C_C is used, it is desirable to have the $1/(2\pi R_C C_C)$ frequency 5 to 10 times lower than the amplifier's natural bandwidth. One additional advantage this circuit provides is that it makes driving capacitive loads much easier. A capacitive load causes the –40 dB/decade intersection (because of the phase lag), to be above unity gain, the same as described previously. In general, this R_C and C_C modification can be used in both an inverting and noninverting configuration with the same results.

APPLICATION INFORMATION

unity-gain concerns (continued)



NOTE A. The difference is due to $1+R_F/R_C$ noise gain.

Figure 48. Unity Gain Compensation

driving a capacitive load

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS403x has been internally compensated to maximize its bandwidth and slew-rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the phase margin of the device leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 49. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

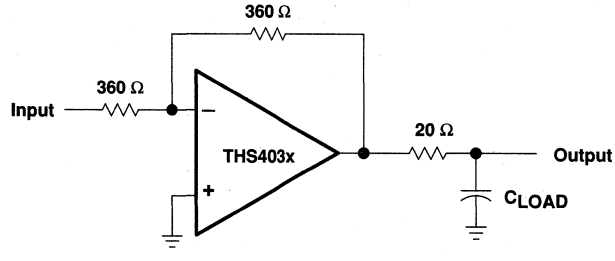


Figure 49. Driving a Capacitive Load

APPLICATION INFORMATION

offset nulling

The THS403x has very low input offset voltage for a high speed amplifier. However, if additional correction is required, the designer can make use of an offset nulling function provided on the THS4031. By placing a potentiometer between terminals 1 and 8 of the device and tying the wiper to the negative supply, the input offset can be adjusted. This is shown in Figure 50.

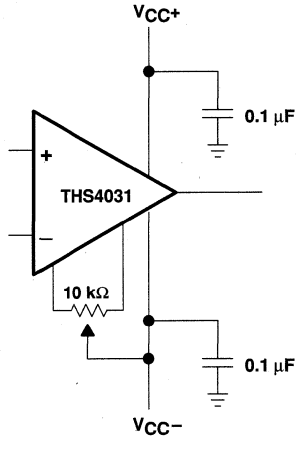
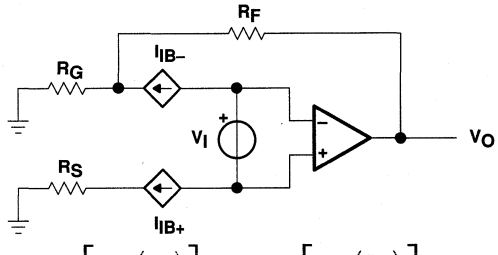


Figure 50. Offset Nulling Schematic

offset voltage

The output offset voltage (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



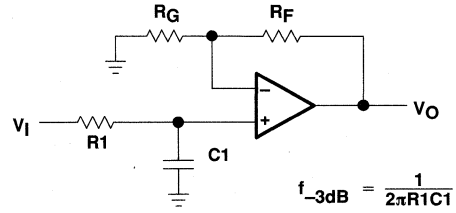
$$V_{OO} = V_{IO}\left[1 + \left(\frac{R_F}{R_G}\right)\right] \pm I_{IB+}\, R_S\left[1 + \left(\frac{R_F}{R_G}\right)\right] \pm I_{IB-}\, R_F$$

Figure 51. Output Offset Voltage Model

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifer (see Figure 52).



$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 52. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple-pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Otherwise, phase shift of the amplifier can occur.

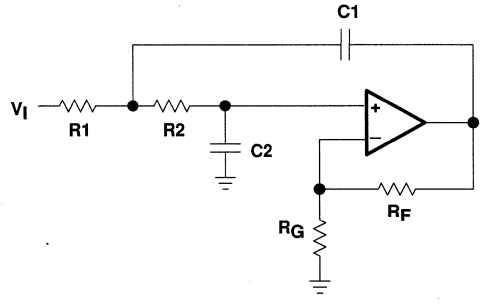


Figure 53. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

circuit-layout considerations

In order to achieve the levels of high-frequency performance of the THS403x, it is essential that proper printed-circuit board high-frequency design techniques be followed. A general set of guidelines is given below. In addition, a THS403x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power-supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inch between the device power terminals and the ceramic capacitors.
- Sockets – Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high-frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high-frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

general PowerPAD design considerations

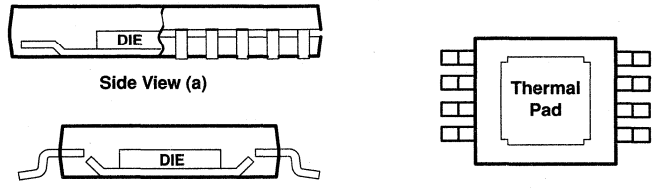
The THS403x is available in a thermally enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 54(a) and Figure 54(b)]. This arrangement results in the leadframe being exposed as a thermal pad on the underside of the package [see Figure 54(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the heretofore awkward mechanical methods of heatsinking.

APPLICATION INFORMATION

general PowerPAD design considerations (continued)



NOTE B. The thermal pad is electrically isolated from all terminals in the package.

Figure 54. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach.

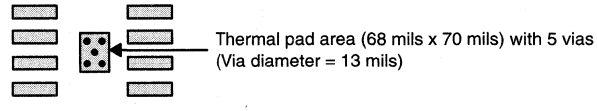


Figure 55. PowerPAD PCB Etch and Via Pattern

1. Prepare the PCB with a top-side etch pattern as shown in Figure 55. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS403xDGN IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, *do not* use the typical web or spoke via connection methodology. Web connections have a high thermal-resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS403xDGN package should connect to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area, which prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and to all the IC terminals.
8. With these preparatory steps in place, the THS403xDGN IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

APPLICATION INFORMATION

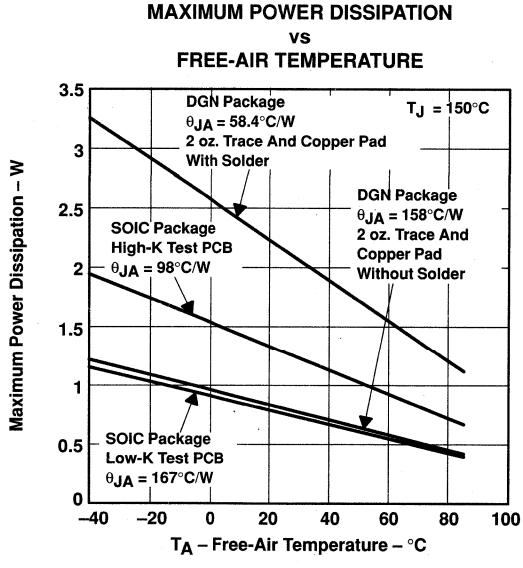
general PowerPAD design considerations (continued)

The actual thermal performance achieved with the THS403xDGN in its PowerPAD package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA}, is about 58.4°C/W. For comparison, the non-PowerPAD version of the THS403x IC (SOIC) is shown. For a given θ_{JA}, the maximum power dissipation is shown in Figure 56 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS403x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A. Results are with no air flow and PCB size = 3″× 3″

Figure 56. Maximum Power Dissipation vs Free-Air Temperature

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments technical brief, *PowerPAD Thermally Enhanced Package*. This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

The next thing to be considered is package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multiamplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 57 to Figure 60 shows this effect, along with the quiescent heat, with an ambient air temperature of 50°C. When using $V_{CC} = \pm 5$ V, heat is generally not a problem, even with SOIC packages. But, when using $V_{CC} = \pm 15$ V, the SOIC package is severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual amplifier package (THS4032), the sum of the RMS output currents and voltages should be used to choose the proper package.

THS4031
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

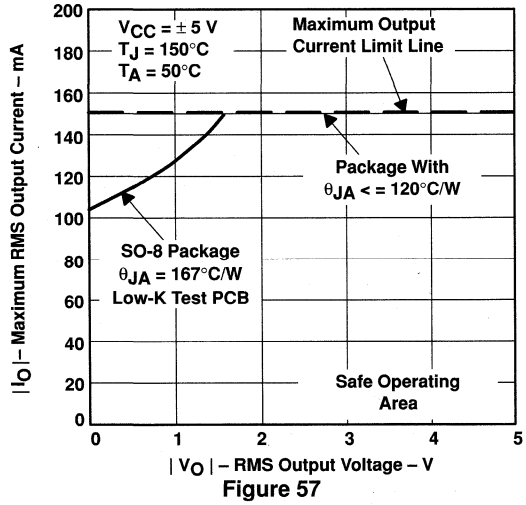


Figure 57

THS4031
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

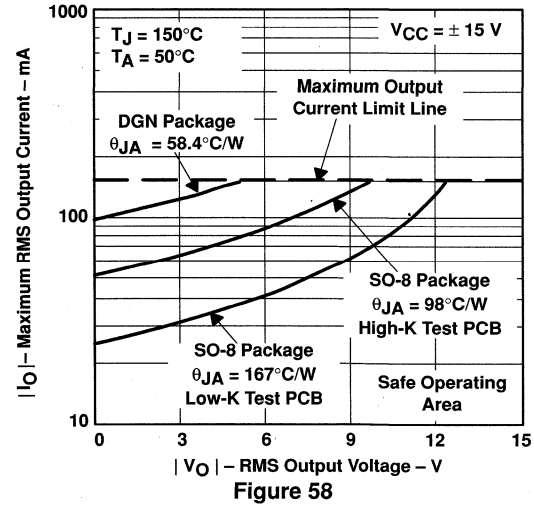


Figure 58

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

THS4032
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

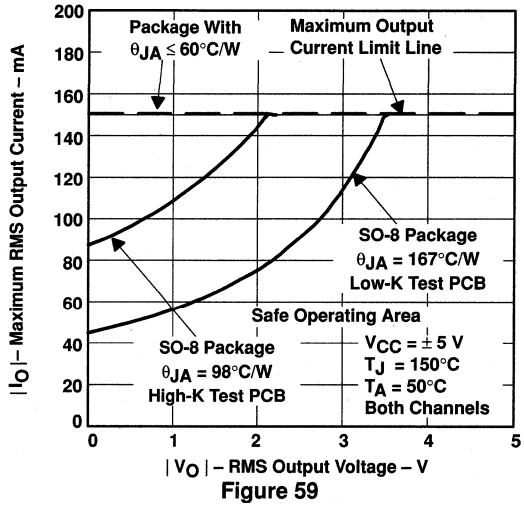


Figure 59

THS4032
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

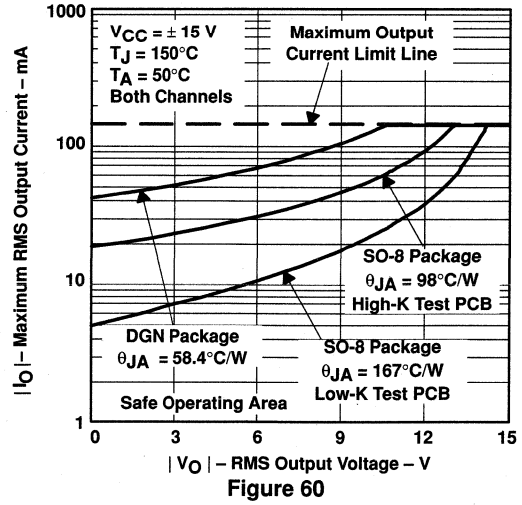


Figure 60

APPLICATION INFORMATION

evaluation board

An evaluation board is available for the THS4031 (literature number SLOP203) and THS4032 (Literature Number SLOP135). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 61. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. For more information, please refer to the *THS4031 EVM User's Guide* (literature number SLOU038) or the *THS4032 EVM User's Guide* (literature number SLOU039). To order the evaluation board, contact your local TI sales office or distributor.

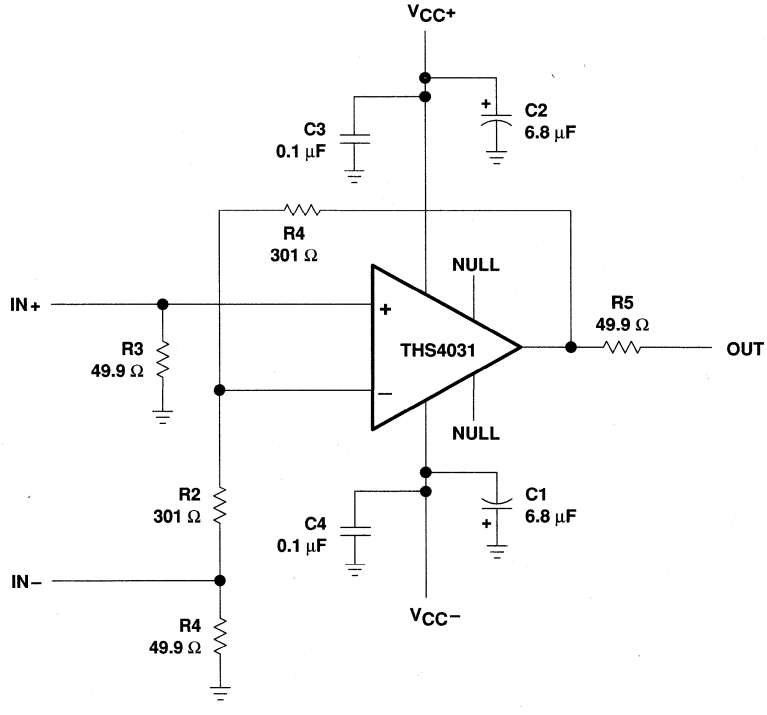
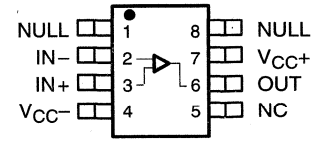


Figure 61. THS4031 Evaluation Board

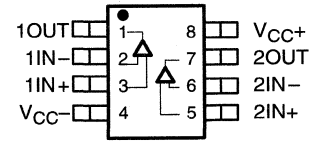
- **C-Stable Amplifiers Drive Any Capacitive Load**
- **High Speed**
  - **165 MHz Bandwidth (–3 dB); C_L = 0 pF**
  - **100 MHz Bandwidth (–3 dB); C_L = 100 pF**
  - **35 MHz Bandwidth (–3 dB); C_L = 1000 pF**
  - **400 V/μs Slew Rate**
- **Unity Gain Stable**
- **High Output Drive, I_O = 100 mA (typ)**
- **Very Low Distortion**
  - **THD = –75 dBc (f = 1 MHz, R_L = 150 Ω)**
  - **THD = –89 dBc (f = 1 MHz, R_L = 1 kΩ)**
- **Wide Range of Power Supplies**
  - **V_{CC} = ±5 V to ±15 V**
- **Available in Standard SOIC or MSOP PowerPAD™ Package**
- **Evaluation Module Available**

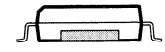
THS4041
D AND DGN PACKAGE
(TOP VIEW)



NC – No internal connection

THS4042
D AND DGN PACKAGE
(TOP VIEW)



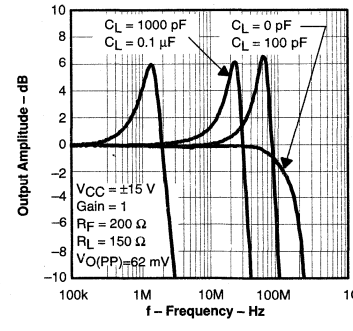


Cross Section View Showing
PowerPAD Option (DGN)

description

The THS4041 and THS4042 are single/dual, high-speed voltage feedback amplifiers capable of driving any capacitive load. This makes them ideal for a wide range of applications including driving video lines or buffering ADCs. The devices feature high 165-MHz bandwidth and 400-V/μsec slew rate. The THS4041/2 are stable at all gains for both inverting and noninverting configurations. For video applications, the THS4041/2 offer excellent video performance with 0.01% differential gain error and 0.01° differential phase error. These amplifiers can drive up to 100 mA into a 20-Ω load and operate off power supplies ranging from ±5V to ±15V.

OUTPUT AMPLITUDE
vs
FREQUENCY



RELATED DEVICES

RELATED DEVICES	
DEVICE	**DESCRIPTION**
THS4011/2	290-MHz Low Distortion High-Speed Amplifier
THS4031/2	100-MHz Low Noise High-Speed Amplifier
THS4081/2	175-MHz Low Power High-Speed Amplifiers

CAUTION: The THS4041 and THS4042 provide ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

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AVAILABLE OPTIONS

T_A	NUMBER OF CHANNELS	PACKAGED DEVICES		MSOP SYMBOL	EVALUATION MODULE
		PLASTIC SMALL OUTLINE† (D)	PLASTIC MSOP† (DGN)		
0°C to 70°C	1	THS4041CD	THS4041CDGN	ACO	THS4041EVM
	2	THS4042CD	THS4042CDGN	ACC	THS4042EVM
–40°C to 85°C	1	THS4041D	THS4041IDGN	ACP	—
	2	THS4042ID	THS4042IDGN	ACD	—

† The D and DGN packages are available taped and reeled. Add an R suffix to the device type (i.e., THS4041CDGNR).

functional block diagram

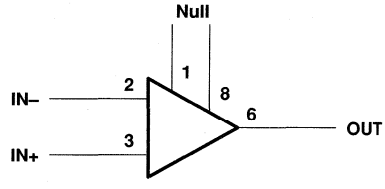


Figure 2. THS4041 – Single Channel

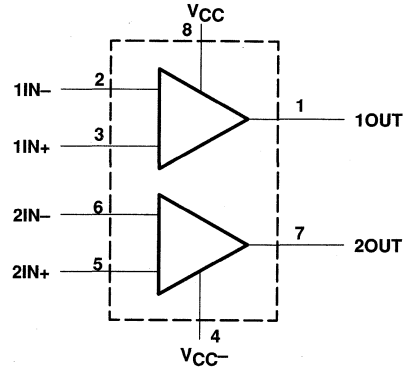


Figure 1. THS4042 – Dual Channel

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} ..... ±16.5 V
Input voltage, V_I ..... $\pm V_{CC}$
Output current, I_O ..... 150 mA
Differential input voltage, V_{IO} ..... ±4 V
Continuous total power dissipation ..... See Dissipation Rating Table
Maximum junction temperature, T_J ..... 150°C
Operating free-air temperature, T_A: C-suffix ..... 0°C to 70°C
I-suffix ..... –40°C to 85°C
Storage temperature, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING
D	167†	38.3	740 mW
DGN‡	58.4	4.7	2.14 W

† This data was taken using the JEDEC standard Low-K test PCB. For the JEDEC proposed High-K test PCB, the θ_{JA} is 95°C/W with a power rating at T_A = 25°C of 1.32 W.
‡ This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3 in. × 3 in. PC. For further information, refer to *Application Information* section of this data sheet.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} and V_{CC-}	Dual supply	±4.5		±16	V
	Single supply	9		32	
Operating free-air temperature, T_A	C-suffix	0		70	°C
	I-suffix	–40		85	

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
BW	Dynamic performance small-signal bandwidth (–3 dB)	V_{CC} = ±15 V	R_f = 200 Ω	Gain = 1		165		MHz
		V_{CC} = ±5 V	R_f = 200 Ω			150		
		V_{CC} = ±15 V	R_f = 1.3 kΩ	Gain = 2		60		MHz
		V_{CC} = ±5 V	R_f = 1.3 kΩ			60		
	Bandwidth for 0.1 dB flatness	V_{CC} = ±15 V	R_f = 200 Ω	Gain = 1		45		MHz
		V_{CC} = ±5 V	R_f = 200 Ω			45		
	Full power bandwidth§	$V_{O(pp)}$ = 20 V,	V_{CC} = ±15 V			6.3		MHz
		$V_{O(pp)}$ = 5 V,	V_{CC} = ±5 V			20		
SR	Slew rate‡	V_{CC} = ±15 V,	20-V step,	Gain = 5		400		V/μs
		V_{CC} = ±5 V,	5-V step,	Gain = –1		325		
t_s	Settling time to 0.1%	V_{CC} = ±15 V,	5-V step	Gain = –1		120		ns
		V_{CC} = ±5 V,	2-V step			120		
	Settling time to 0.01%	V_{CC} = ±15 V,	5-V step	Gain = –1		250		ns
		V_{CC} = ±5 V,	2-V step			280		

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix
‡ Slew rate is measured from an output level range of 25% to 75%.
§ Full power bandwidth = slew rate / 2 π $V_{O(Peak)}$.

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

noise/distortion performance

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	$V_{O(pp)}$ = 2 V, f = 1 MHz, Gain = 2	V_{CC} = ±15 V	R_L = 150 Ω		–75		dBc
				R_L = 1 kΩ		–89		
			V_{CC} = ±5 V	R_L = 150 Ω		–75		
				R_L = 1 kΩ		–86		
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz			14		nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz			0.9		pA/√Hz

	Differential gain error	Gain = 2, 40 IRE modulation,	NTSC, ±100 IRE ramp	V_{CC} = ±15 V	0.01%	
				V_{CC} = ±5 V	0.01%	
	Differential phase error	Gain = 2, 40 IRE modulation,	NTSC, ±100 IRE ramp	V_{CC} = ±15 V	0.01°	
				V_{CC} = ±5 V	0.02°	
	Channel-to-channel crosstalk (THS4042 only)	V_{CC} = ±5 V or ±15 V,	f = 1 MHz	Gain = 2	–64	dB

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

dc performance

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
	Open loop gain	V_{CC} = ±15 V, R_L = 1 kΩ	V_O = ±10 V,	T_A = 25°C	74	80		dB
				T_A = full range	69			
		V_{CC} = ±5 V, R_L = 250 Ω	V_O = ±2.5 V,	T_A = 25°C	69	76		
				T_A = full range	66			
V_{OS}	Input offset voltage	V_{CC} = ±5 V or ±15 V		T_A = 25°C		2.5	10	mV
				T_A = full range			13	
	Offset voltage drift	V_{CC} = ±5 V or ±15 V		T_A = full range		10		µV/°C
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V		T_A = 25°C		2.5	6	µA
				T_A = full range			8	
I_{OS}	Input offset current	V_{CC} = ±5 V or ±15 V		T_A = 25°C		35	250	nA
				T_A = full range			400	
	Offset current drift	T_A = full range				0.3		nA/°C

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

input characteristics

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V			±13.8	±14.3		V
		V_{CC} = ±5 V			±3.8	±4.3		
CMRR	Common mode rejection ratio	V_{CC} = ±15 V,	V_{ICR} = ±12 V	T_A = full range	70	90		dB
		V_{CC} = ±5 V,	V_{ICR} = ±2.5 V		80	100		
r_i	Input resistance					1		MΩ
C_i	Input capacitance					1.5		pF

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

output characteristics

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 250 Ω	±11.5	±13		V
		V_{CC} = ±5 V	R_L = 150 Ω	±3.2	±3.5		
		V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.6		V
		V_{CC} = ±5 V		±3.5	±3.8		
I_O	Output current‡	V_{CC} = ±15 V	R_L = 20 Ω	80	100		mA
		V_{CC} = ±5 V		50	65		
I_{SC}	Short-circuit current‡	V_{CC} = ±15 V			150		mA
R_O	Output resistance	Open loop			13		Ω

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

‡ Observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the absolute maximum ratings section of this data sheet for more information.

power supply

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (per amplifier)	V_{CC} = ±15 V	T_A = 25°C		8	9.5	mA
			T_A = full range			11	
		V_{CC} = ±5 V	T_A = 25°C		7	8.5	
			T_A = full range			10	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	75	84		dB
			T_A = full range	70			

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

TYPICAL CHARACTERISTICS

OPEN LOOP GAIN AND PHASE RESPONSE vs FREQUENCY

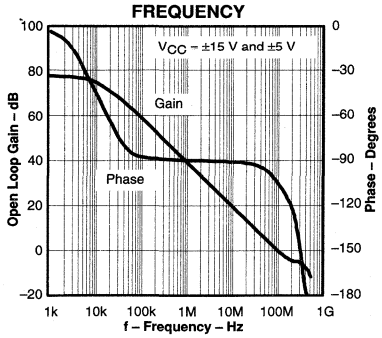


Figure 3

OUTPUT AMPLITUDE vs FREQUENCY

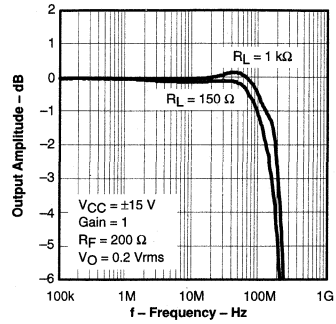


Figure 4

OUTPUT AMPLITUDE vs FREQUENCY

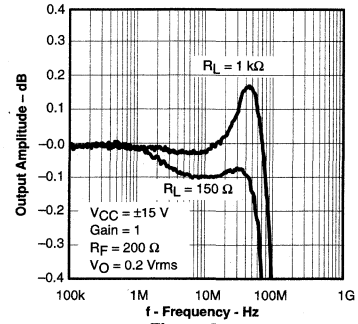


Figure 5

OUTPUT AMPLITUDE vs FREQUENCY

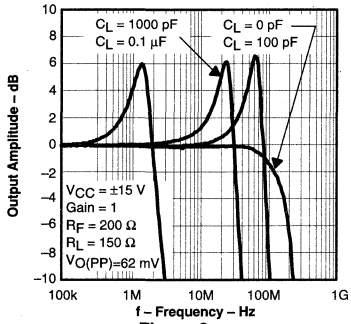


Figure 6

OUTPUT AMPLITUDE vs FREQUENCY

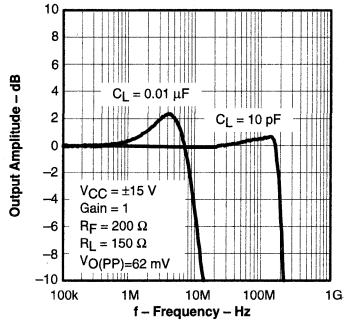


Figure 7

OUTPUT AMPLITUDE vs FREQUENCY

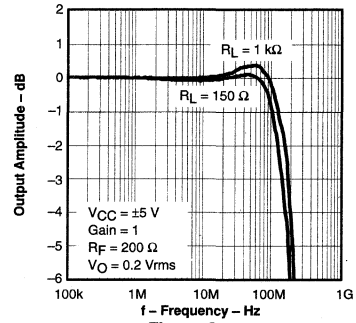


Figure 8

OUTPUT AMPLITUDE vs FREQUENCY

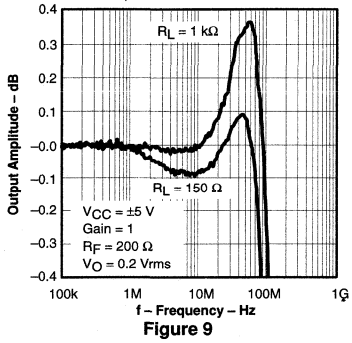


Figure 9

OUTPUT AMPLITUDE vs FREQUENCY

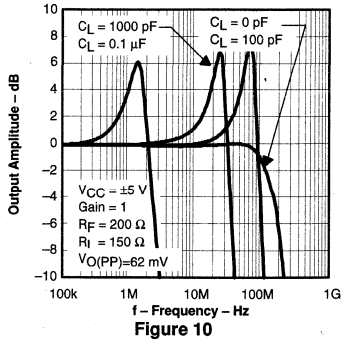


Figure 10

OUTPUT AMPLITUDE vs FREQUENCY

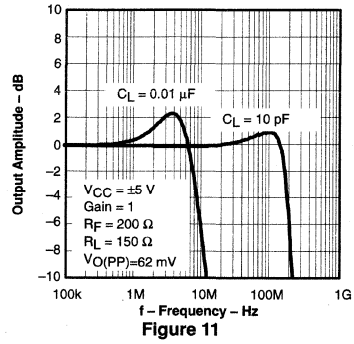


Figure 11

TYPICAL CHARACTERISTICS

OUTPUT AMPLITUDE vs FREQUENCY

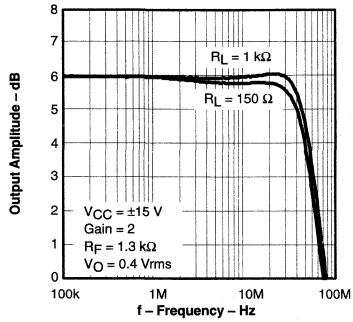


Figure 12

OUTPUT AMPLITUDE vs FREQUENCY

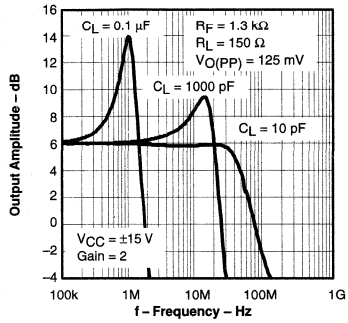


Figure 13

OUTPUT AMPLITUDE vs FREQUENCY

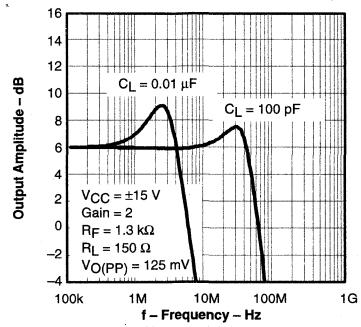


Figure 14

OUTPUT AMPLITUDE vs FREQUENCY

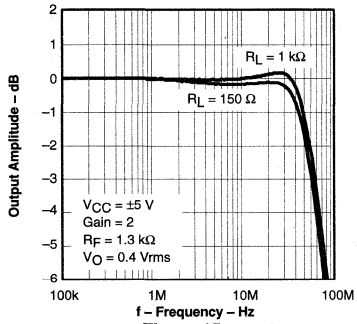


Figure 15

OUTPUT AMPLITUDE vs FREQUENCY

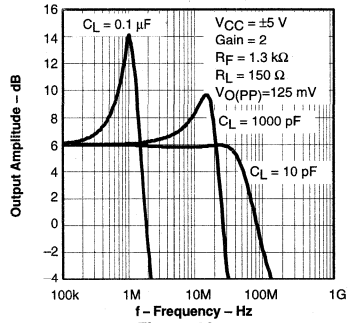


Figure 16

OUTPUT AMPLITUDE vs FREQUENCY

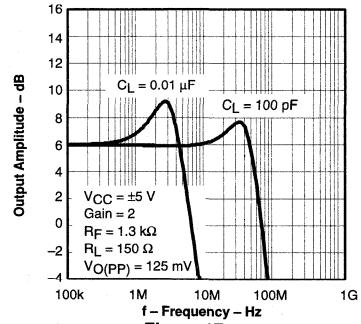


Figure 17

OUTPUT AMPLITUDE vs FREQUENCY

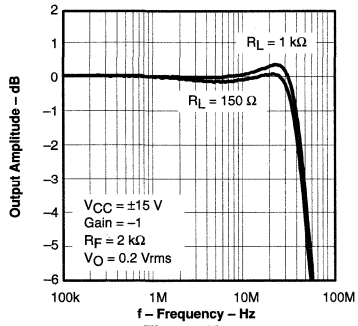


Figure 18

OUTPUT AMPLITUDE vs FREQUENCY

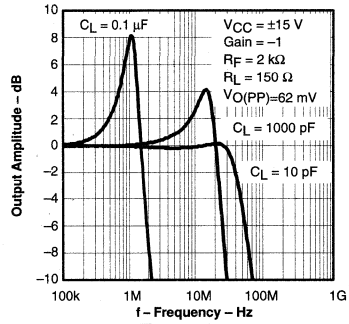


Figure 19

OUTPUT AMPLITUDE vs FREQUENCY

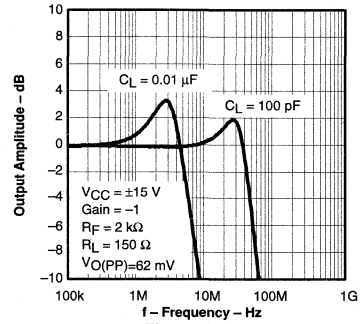


Figure 20

TYPICAL CHARACTERISTICS

OUTPUT AMPLITUDE vs FREQUENCY

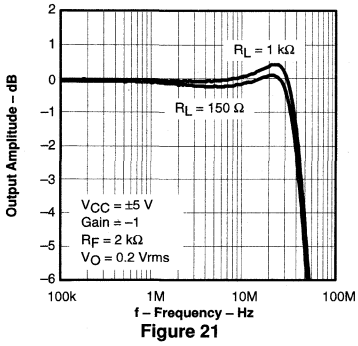


Figure 21

OUTPUT AMPLITUDE vs FREQUENCY

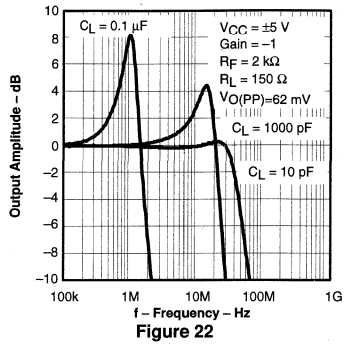


Figure 22

OUTPUT AMPLITUDE vs FREQUENCY

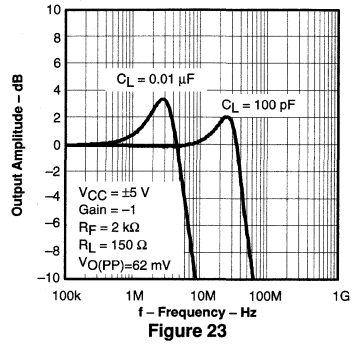


Figure 23

OUTPUT OVERSHOOT vs CAPACITIVE LOAD

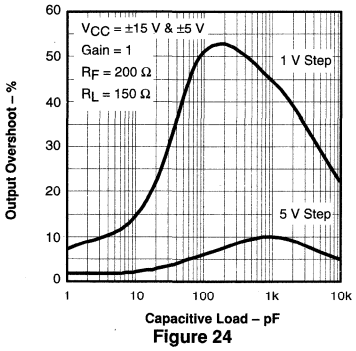


Figure 24

OUTPUT OVERSHOOT vs CAPACITIVE LOAD

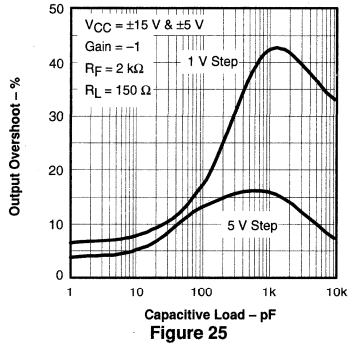


Figure 25

TOTAL HARMONIC DISTORTION vs FREQUENCY

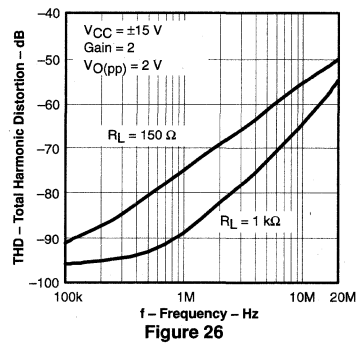


Figure 26

DISTORTION vs FREQUENCY

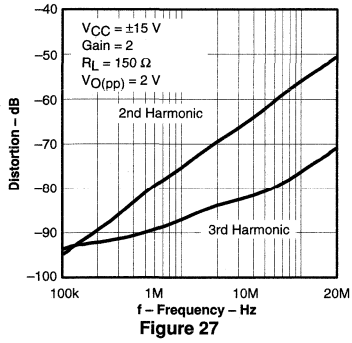


Figure 27

DISTORTION vs FREQUENCY

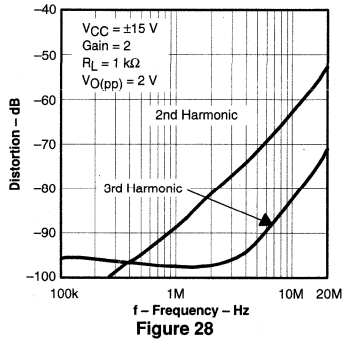


Figure 28

DISTORTION vs FREQUENCY

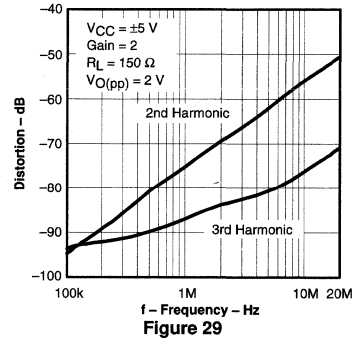


Figure 29

TYPICAL CHARACTERISTICS

DISTORTION vs FREQUENCY

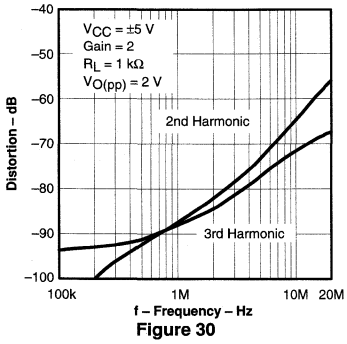


Figure 30

DISTORTION vs OUTPUT VOLTAGE

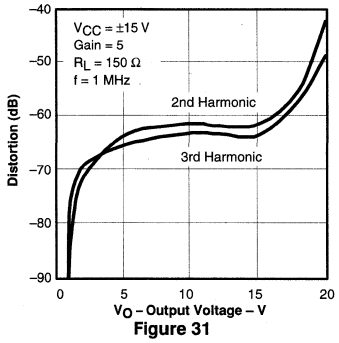


Figure 31

DISTORTION vs OUTPUT VOLTAGE

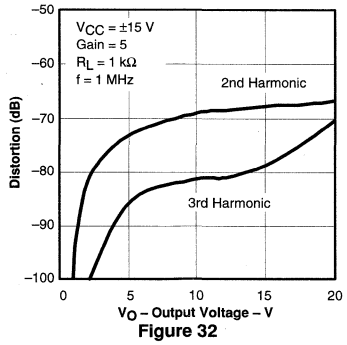


Figure 32

DIFFERENTIAL GAIN vs NUMBER OF 150-Ω LOADS

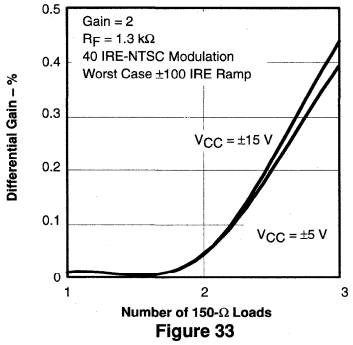


Figure 33

DIFFERENTIAL PHASE vs NUMBER OF 150-Ω LOADS

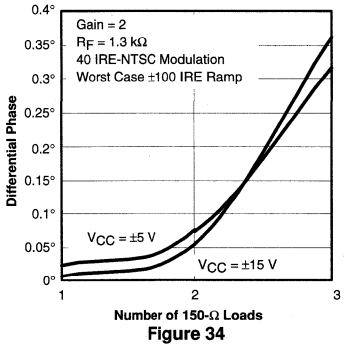


Figure 34

DIFFERENTIAL GAIN vs NUMBER OF 150-Ω LOADS

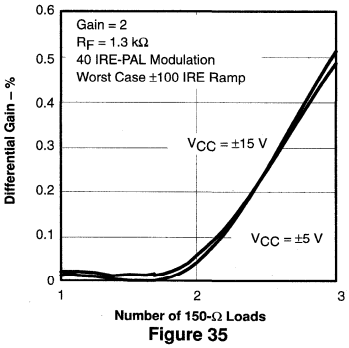


Figure 35

DIFFERENTIAL PHASE vs NUMBER OF 150-Ω LOADS

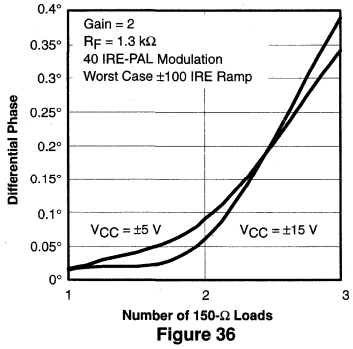


Figure 36

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

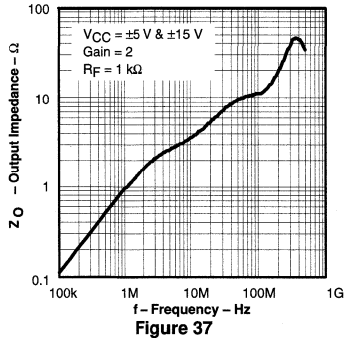


Figure 37

PSRR vs FREQUENCY

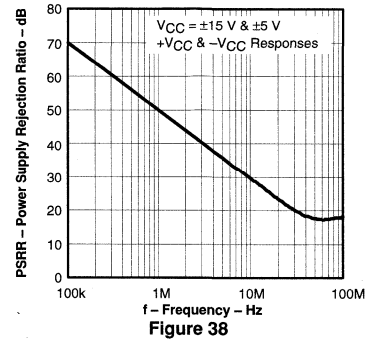


Figure 38

TYPICAL CHARACTERISTICS

CMRR vs FREQUENCY

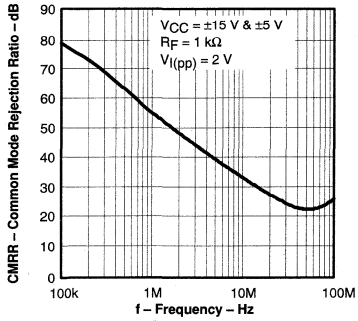


Figure 39

CROSSTALK vs FREQUENCY

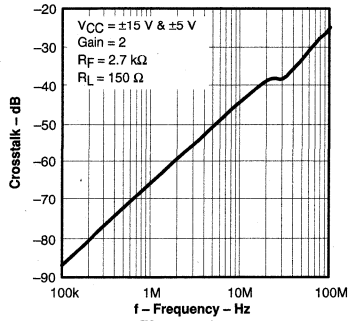


Figure 40

VOLTAGE & CURRENT NOISE vs FREQUENCY

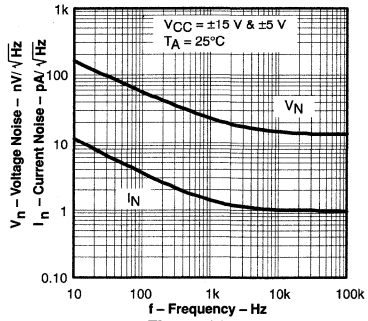


Figure 41

SLEW RATE vs FREE-AIR TEMPERATURE

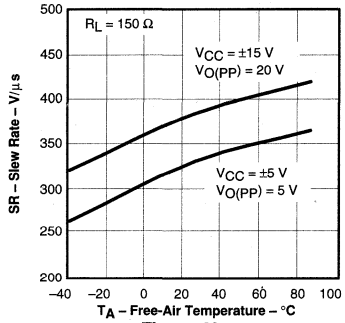


Figure 42

SETTING TIME vs OUTPUT STEP

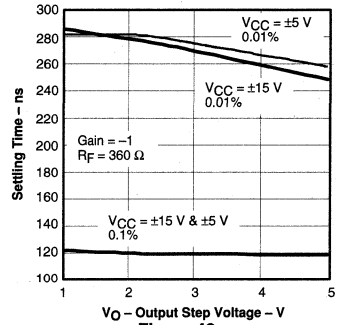


Figure 43

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

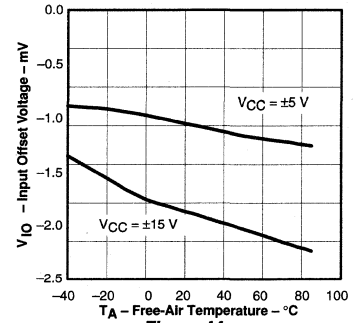


Figure 44

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

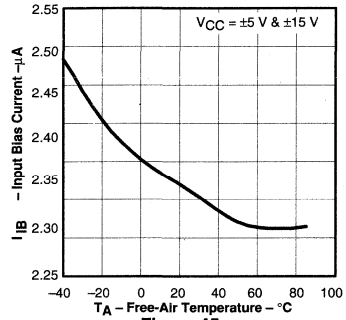


Figure 45

COMMON-MODE INPUT VOLTAGE vs SUPPLY VOLTAGE

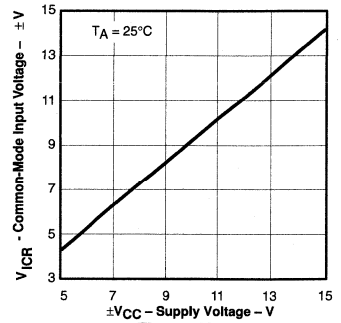


Figure 46

OUTPUT VOLTAGE vs SUPPLY VOLTAGE

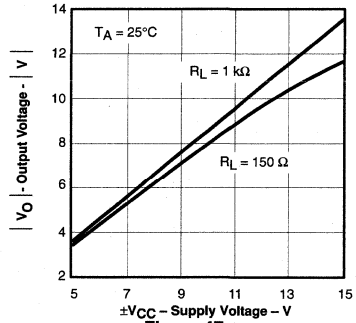


Figure 47

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

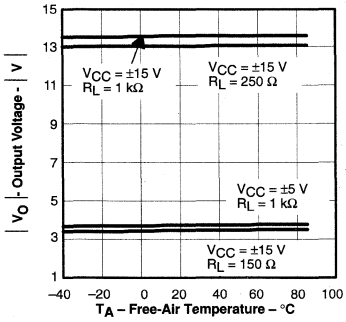


Figure 48

SUPPLY CURRENT vs SUPPLY VOLTAGE

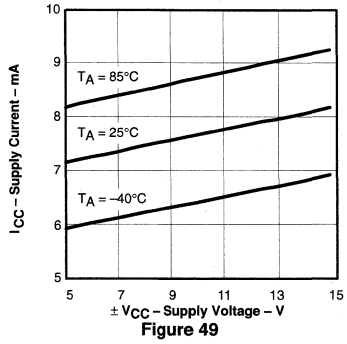


Figure 49

1-V FALLING EDGE RESPONSE

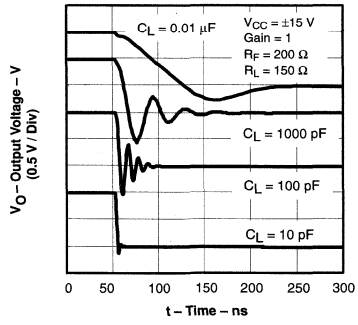


Figure 50

1-V FALLING EDGE RESPONSE

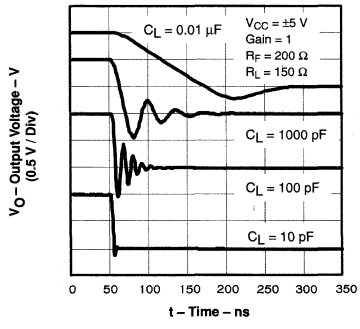


Figure 51

5-V FALLING EDGE RESPONSE

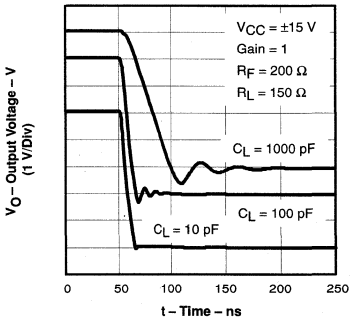


Figure 52

5-V FALLING EDGE RESPONSE

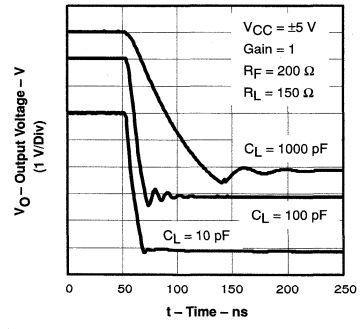


Figure 53

5-V AND 1-V STEP RESPONSE

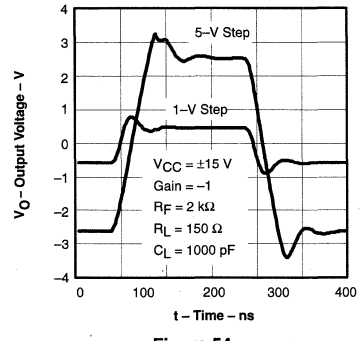


Figure 54

5-V AND 1-V STEP RESPONSE

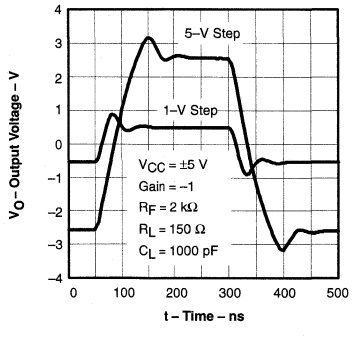


Figure 55

CAPACITIVE LOAD RESPONSE

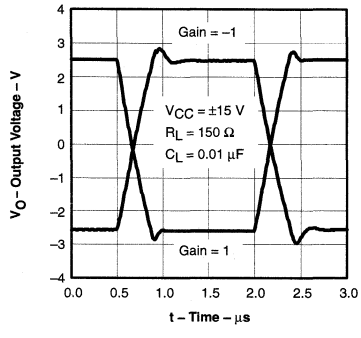


Figure 56

TYPICAL CHARACTERISTICS

CAPACITIVE LOAD RESPONSE

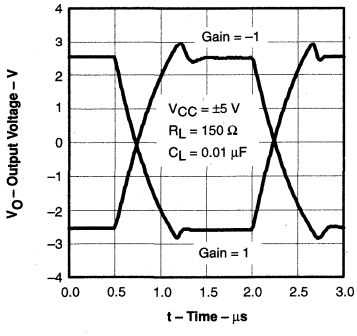


Figure 57

1-VOLT STEP RESPONSE

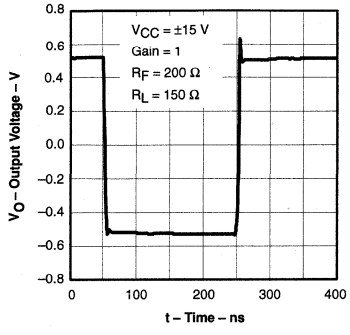


Figure 58

1-VOLT STEP RESPONSE

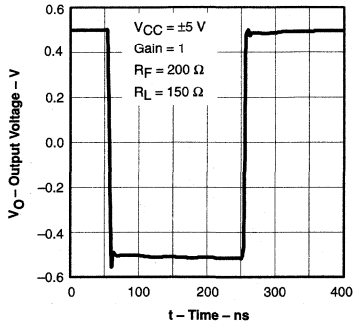


Figure 59

20-VOLT STEP RESPONSE

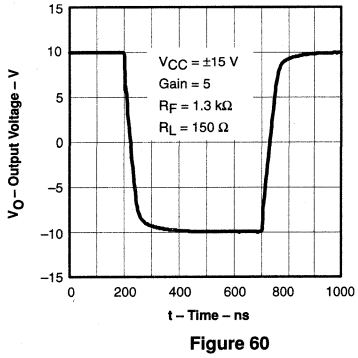


Figure 60

5-V STEP RESPONSE

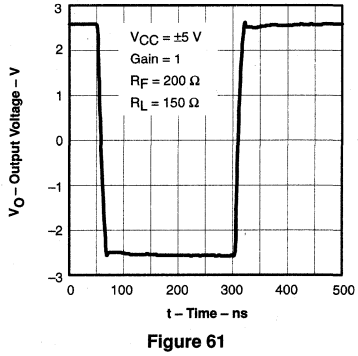


Figure 61

APPLICATION INFORMATION

theory of operation

The THS404x is a high-speed, operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This results in an exceptionally high performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 62.

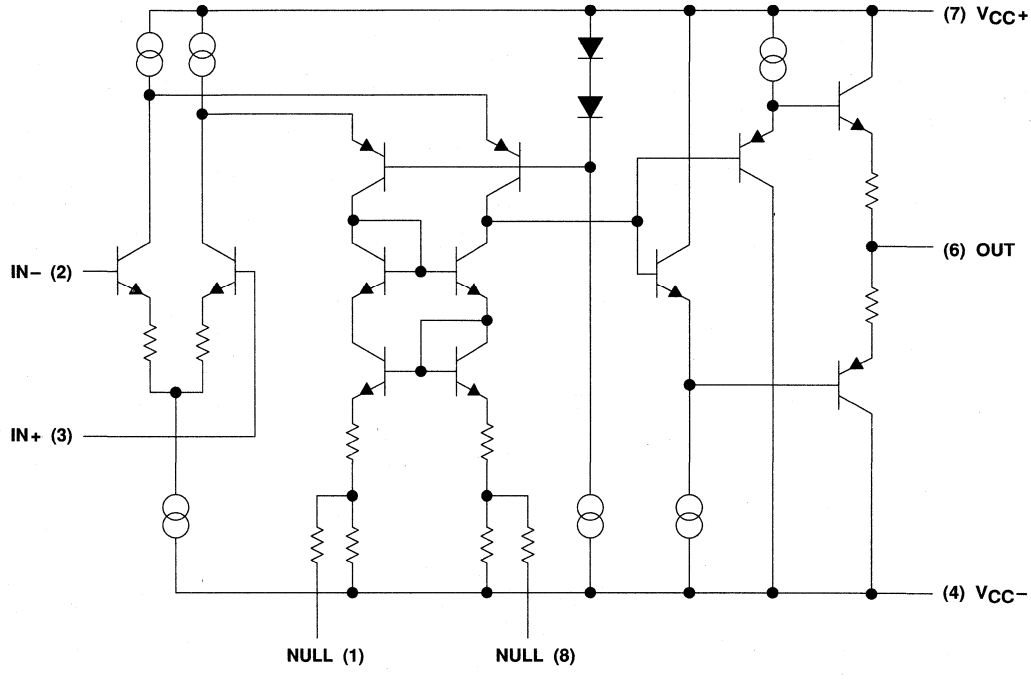


Figure 62. THS4041 Simplified Schematic

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true when amplifying small signals, where signal-to-noise ration (SNR) is very important. The noise model for the THS404x is shown in Figure 63. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{\text{Hz}}$)
- IN+ = Noninverting current noise (pA/$\sqrt{\text{Hz}}$)
- IN– = Inverting current noise (pA/$\sqrt{\text{Hz}}$)
- e_{Rx} = Thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR_x)

APPLICATION INFORMATION

noise calculations and noise figure (continued)

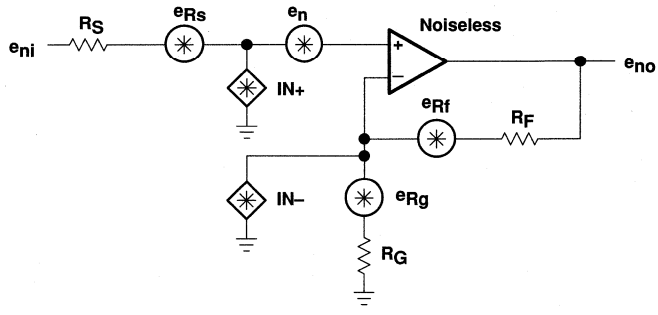


Figure 63. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN + \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\ kTR_s + 4\ kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\ A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (noninverting case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

For more information on noise analysis, please refer to the *Noise Analysis* section in *Operational Amplifier Circuits Applications Report* (literature number SLVA043).

APPLICATION INFORMATION

noise calculations and noise figure (continued)

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^2}{\left(e_{Rs}\right)^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\ kTR_S}\right]$$

Figure 64 shows the noise figure graph for the THS404x.

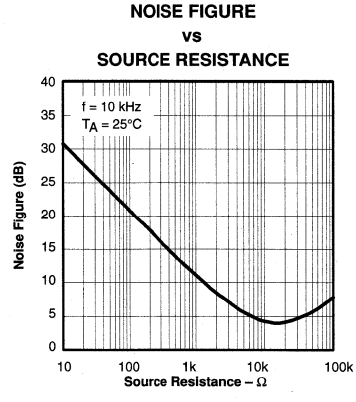


Figure 64. Noise Figure vs Source Resistance

APPLICATION INFORMATION

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS404x has been internally compensated to maximize its bandwidth and slew rate performance. Typically when the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin, leading to high frequency ringing or oscillations. However, the THS404x has added internal circuitry that senses a capacitive load and adds extra compensation to the internal dominant pole. As the capacitive load increases, the amplifier remains stable. But, it is not uncommon to see a small amount of peaking in the frequency response. There are typically two ways to compensate for this. The first is to simply increase the gain of the amplifier. This helps by increasing the phase margin to keep peaking minimized. The second is to place an isolation resistor in series with the output of the amplifier, as shown in Figure 65. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end. For more information about driving capacitive loads, refer to the *Output Resistance and Capacitance* section of the *Parasitic Capacitance in Op Amp Circuits Application Report* (literature number: SLOA013).

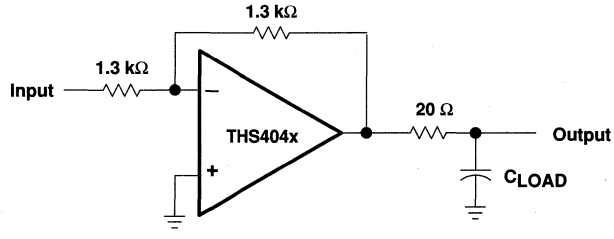


Figure 65. Driving a Capacitive Load for Extra Stability

offset nulling

The THS404x has very low input offset voltage for a high-speed amplifier. However, if additional correction is required, an offset nulling function has been provided on the THS4041. The input offset can be adjusted by placing a potentiometer between terminals 1 and 8 of the device and tying the wiper to the negative supply. This is shown in Figure 66.

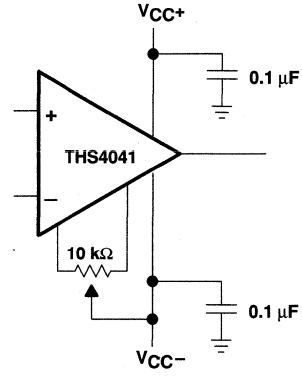
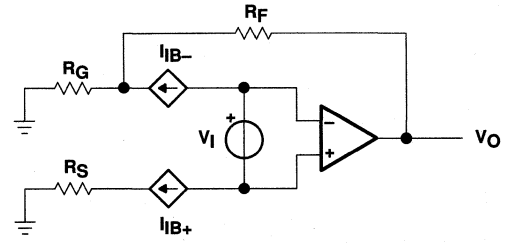


Figure 66. Offset Nulling Schematic

APPLICATION INFORMATION

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

Figure 67. Output Offset Voltage Model

optimizing unity gain response

Internal frequency compensation of the THS404x was selected to provide very wideband performance yet still maintain stability when operated in a noninverting unity gain configuration. When amplifiers are compensated in this manner there is usually peaking in the closed loop response and some ringing in the step response for very fast input edges, depending upon the application. This is because a minimum phase margin is maintained for the G=+1 configuration. For optimum settling time and minimum ringing, a feedback resistor of 200 Ω should be used as shown in Figure 68. Additional capacitance can also be used in parallel with the feedback resistance if even finer optimization is required.

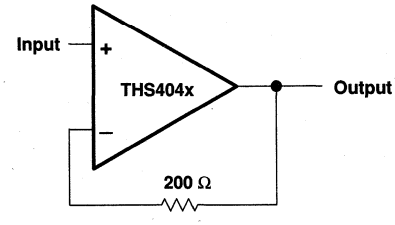


Figure 68. Noninverting, Unity Gain Schematic

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high frequency performance of the THS404x, follow proper printed-circuit board high frequency design techniques. A general set of guidelines is given below. In addition, a THS404x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

general PowerPAD design considerations

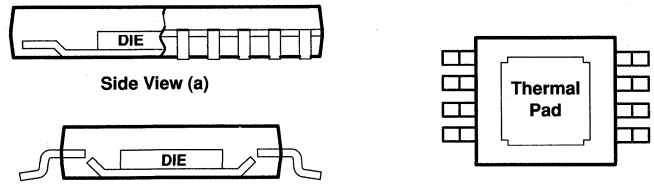
The THS404x is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 69(a) and Figure 69(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 69(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the, heretofore, awkward mechanical methods of heatsinking.

APPLICATION INFORMATION

general PowerPAD design considerations (continued)



NOTE A. The thermal pad is electrically isolated from all terminals in the package.

Figure 69. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach.

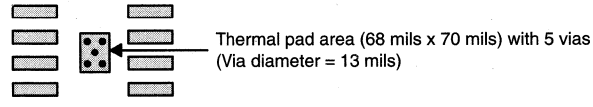


Figure 70. PowerPAD PCB Etch and Via Pattern

1. Prepare the PCB with a top side etch pattern as shown in Figure 70. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS404xDGN IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS404xDGN package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the THS404xDGN IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

APPLICATION INFORMATION

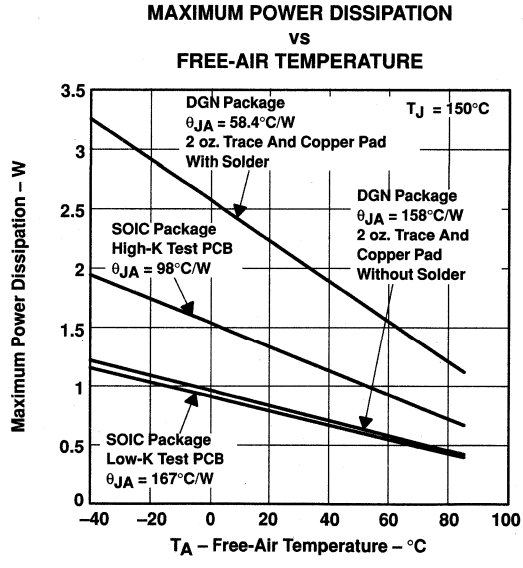
general PowerPAD design considerations (continued)

The actual thermal performance achieved with the THS404xDGN in its PowerPAD package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA}, is about 58.4°C/W. For comparison, the non-PowerPAD version of the THS404x IC (SOIC) is shown. For a given θ_{JA}, the maximum power dissipation is shown in Figure 71 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX}-T_A}{\theta_{JA}}\right)$$

Where:

P_D = Maximum power dissipation of THS404x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case (°C/W)
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A. Results are with no air flow and PCB size = 3"× 3"

Figure 71. Maximum Power Dissipation vs Free-Air Temperature

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially mutiamplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 72 to Figure 75 show this effect, along with the quiescent heat, with an ambient air temperature of 50°C. Obviously, as the ambient temperature increases, the limit lines shown will drop accordingly. The area under each respective limit line is considered the safe operating area. Any condition above this line will exceed the amplifier's limits and failure may result. When using $V_{CC} = \pm 5$ V, there is generally not a heat problem, even with SOIC packages. But, when using $V_{CC} = \pm 15$ V, the SOIC package is severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual amplifier package (THS4042), the sum of the RMS output currents and voltages should be used to choose the proper package. The graphs shown assume that both amplifier's outputs are identical.

THS4041
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

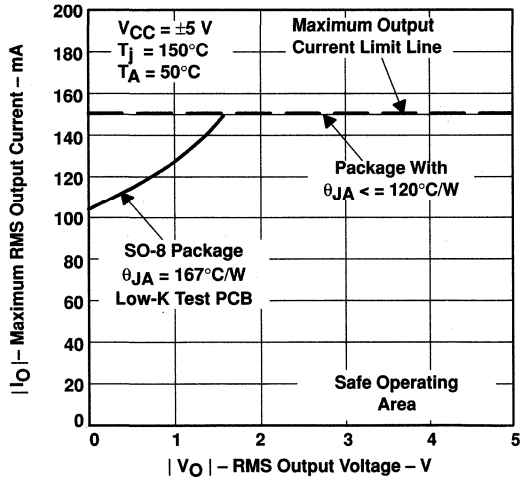


Figure 72

THS4041
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

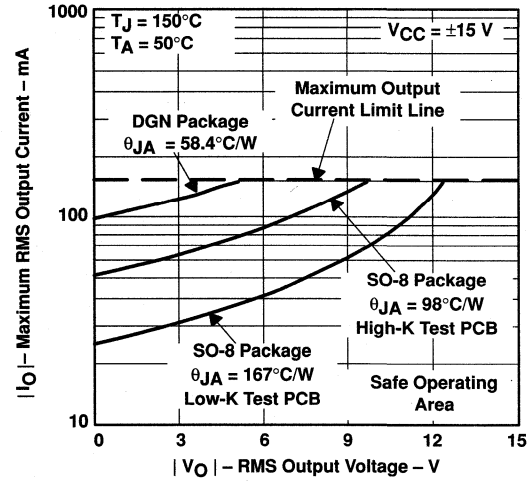


Figure 73

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

THS4042
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

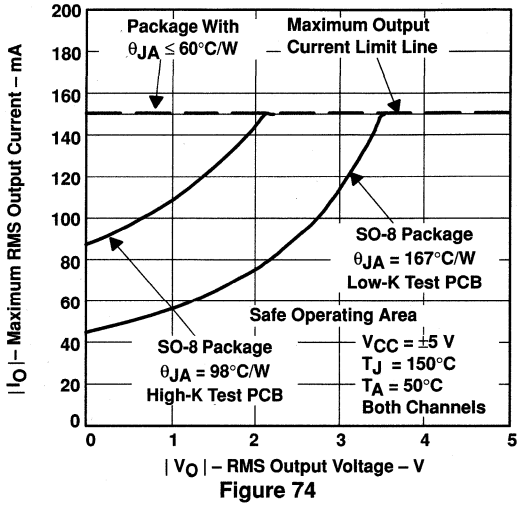


Figure 74

THS4042
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

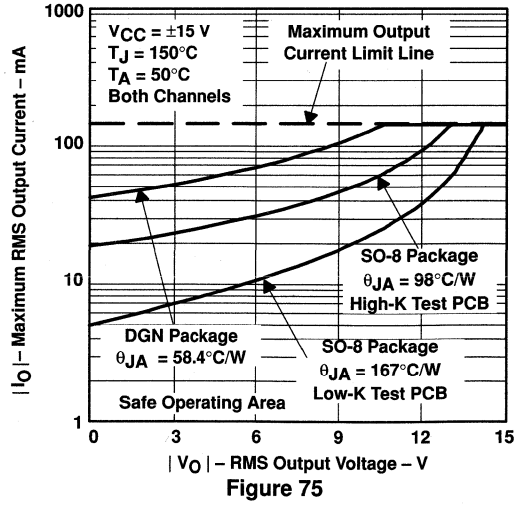


Figure 75

APPLICATION INFORMATION

evaluation board

An evaluation board is available for the THS4041 (literature number SLOP219) and THS4042 (literature number SLOP233). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 76. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. For more information, please refer to the *THS4041 EVM User's Guide* or the *THS4042 EVM User's Guide*. To order the evaluation board, contact your local TI sales office or distributor.

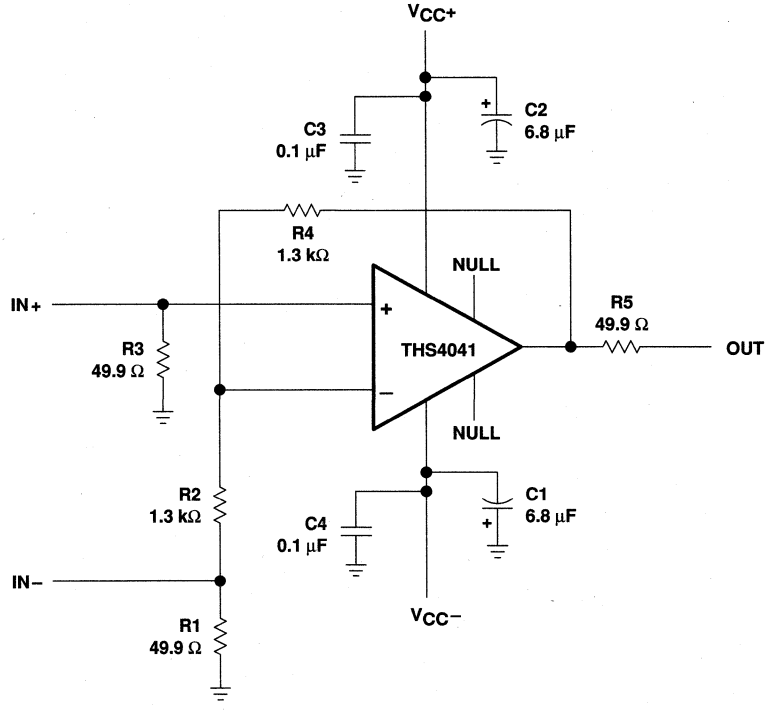
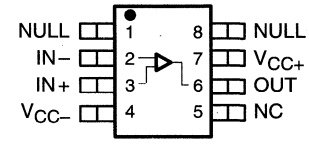


Figure 76. THS4041 Evaluation Board

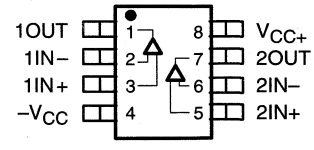
- **High Speed**
  - **70 MHz Bandwidth (G = 1, –3 dB)**
  - **240 V/μs Slew Rate**
  - **60-ns Settling Time (0.1%)**
- **High Output Drive, I_O = 100 mA (typ)**
- **Excellent Video Performance**
  - **0.1 dB Bandwidth of 30 MHz (G = 1)**
  - **0.01% Differential Gain**
  - **0.01° Differential Phase**
- **Very Low Distortion**
  - **THD = –82 dBc (f = 1 MHz, R_L = 150 Ω)**
  - **THD = –89 dBc (f = 1 MHz, R_L = 1 kΩ)**
- **Wide Range of Power Supplies**
  - **V_{CC} = ±5 V to ±15 V**
- **Available in Standard SOIC or MSOP PowerPAD™ Package**
- **Evaluation Module Available**

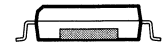
THS4051
D AND DGN PACKAGE
(TOP VIEW)



NC – No internal connection

THS4052
D AND DGN† PACKAGE
(TOP VIEW)





Cross Section View Showing
PowerPAD Option (DGN)

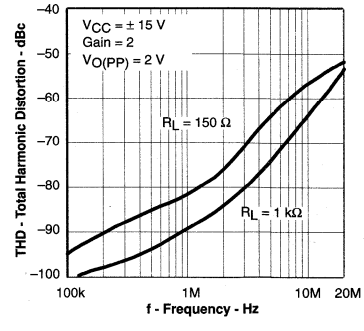
† This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

description

The THS4051 and THS4052 are general-purpose, single/dual, high-speed voltage feedback amplifiers ideal for a wide range of applications including video, communication, and imaging. The devices offer very good ac performance with 70-MHz bandwidth, 240-V/μs slew rate, and 60-ns settling time (0.1%). The THS4051/2 are stable at all gains for both inverting and noninverting configurations. These amplifiers have a high output drive capability of 100 mA and draw only 8.5-mA supply current per channel. Excellent professional video results can be obtained with the low differential gain/phase errors of 0.01%/0.01° and wide 0.1 db flatness to 30 MHz. For applications requiring low distortion, the THS4051/2 is ideally suited with total harmonic distortion of –82 dBc at 1 MHz.

RELATED DEVICES	
DEVICE	**DESCRIPTION**
THS4011/2	290-MHz Low Distortion High-Speed Amplifiers
THS4031/2	100-MHz Low Noise High-Speed Amplifiers
THS4081/2	175-MHz Low Power High-Speed Amplifiers

TOTAL HARMONIC DISTORTION
vs
FREQUENCY



CAUTION: The THS4051 and THS4052 provide ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

PowerPAD is a trademark of Texas Instruments Incorporated.

AVAILABLE OPTIONS

T_A	NUMBER OF CHANNELS	PACKAGED DEVICES		MSOP SYMBOL	EVALUATION MODULE
		PLASTIC SMALL OUTLINE† (D)	PLASTIC MSOP† (DGN)		
0°C to 70°C	1	THS4051CD	THS4051CDGN	ACQ	THS4051EVM
	2	THS4052CD	THS4052CDGN‡	ACE	THS4052EVM
–40°C to 85°C	1	THS4051ID	THS4051IDGN	ACR	—
	2	THS4052ID	THS4052IDGN‡	ACF	—

† The D and DGN packages are available taped and reeled. Add an R suffix to the device type (i.e., THS4051CDGN).
‡ This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

functional block diagram

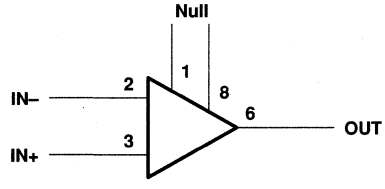


Figure 1. THS4051 – Single Channel

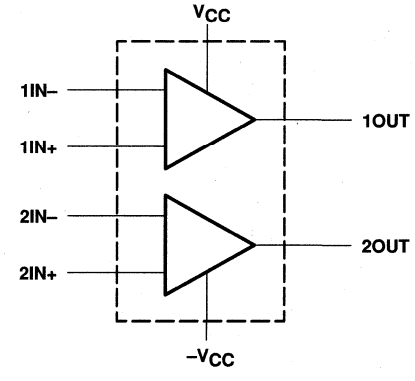


Figure 2. THS4052 – Dual Channel

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} ..... ±16.5 V
Input voltage, V_I ..... $\pm V_{CC}$
Output current, I_O ..... 150 mA
Differential input voltage, V_{IO} ..... ±4 V
Continuous total power dissipation ..... See Dissipation Rating Table
Maximum junction temperature, T_J ..... 150°C
Operating free-air temperature, T_A: C-suffix ..... 0°C to 70°C
I-suffix ..... –40°C to 85°C
Storage temperature, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING
D	167†	38.3	740 mW
DGN‡	58.4	4.7	2.14 W

† This data was taken using the JEDEC standard Low-K test PCB. For the JEDEC Proposed High-K test PCB, the θ_{JA} is 95°C/W with a power rating at T_A = 25°C of 1.32 W.
‡ This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3 in. × 3 in. PC. For further information, refer to *Application Information* section of this data sheet.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} and V_{CC-}	Dual supply	±4.5		±16	V
	Single supply	9		32	
Operating free-air temperature, T_A	C-suffix	0		70	°C
	I-suffix	–40		85	

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
BW	Dynamic performance small-signal bandwidth (–3 dB)	V_{CC} = ±15 V	Gain = 1		70		MHz
		V_{CC} = ±5 V			70		
		V_{CC} = ±15 V	Gain = 2		38		MHz
		V_{CC} = ±5 V			38		
	Bandwidth for 0.1 dB flatness	V_{CC} = ±15 V	Gain = 1		30		MHz
		V_{CC} = ±5 V			30		
	Full power bandwidth§	$V_{O(pp)}$ = 20 V, V_{CC} = ±15 V			3.8		MHz
		$V_{O(pp)}$ = 5 V, V_{CC} = ±5 V			12.7		
SR	Slew rate‡	V_{CC} = ±15 V, 20-V step,	Gain = 5		240		V/μs
		V_{CC} = ±5 V, 5-V step	Gain = –1		200		
t_s	Settling time to 0.1%	V_{CC} = ±15 V, 5-V step	Gain = –1		60		ns
		V_{CC} = ±5 V, 2-V step			60		
	Settling time to 0.01%	V_{CC} = ±15 V, 5-V step	Gain = –1		130		ns
		V_{CC} = ±5 V, 2-V step			140		

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix
‡ Slew rate is measured from an output level range of 25% to 75%.
§ Full power bandwidth = slew rate/2 $\pi V_{O(Peak)}$.

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

noise/distortion performance

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	$V_{O(pp)}$ = 2 V, f = 1 MHz, Gain = 2	V_{CC} = ±15 V	R_L = 150 Ω		–82		dBc
				R_L = 1 kΩ		–89		
			V_{CC} = ±5 V	R_L = 150 Ω		–78		
				R_L = 1 kΩ		–87		
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz			14		nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz			0.9		pA/√Hz

	Differential gain error	Gain = 2, 40 IRE modulation,	NTSC, ±100 IRE ramp	V_{CC} = ±15 V	0.01%	
				V_{CC} = ±5 V	0.01%	
	Differential phase error	Gain = 2, 40 IRE modulation,	NTSC, ±100 IRE ramp	V_{CC} = ±15 V	0.01°	
				V_{CC} = ±5 V	0.03°	
	Channel-to-channel crosstalk (THS4052 only)	V_{CC} = ±5 V or ±15 V,	f = 1 MHz		–57	dB

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix.

dc performance

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
	Open loop gain	V_{CC} = ±15 V, R_L = 1 kΩ	V_O = ±10 V	T_A = 25°C	5	9		V/mV
				T_A = full range	3			
		V_{CC} = ±5 V, R_L = 250 Ω	V_O = ±2.5 V	T_A = 25°C	2.5	6		V/mV
				T_A = full range	2			
V_{OS}	Input offset voltage	V_{CC} = ±5 V or ±15 V		T_A = 25°C		2.5	10	mV
				T_A = full range			12	
	Offset voltage drift	V_{CC} = ±5 V or ±15 V		T_A = full range		15		µV/°C
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V		T_A = 25°C		2.5	6	µA
				T_A = full range			8	
I_{OS}	Input offset current	V_{CC} = ±5 V or ±15 V		T_A = 25°C		35	250	nA
				T_A = full range			400	
	Offset current drift	T_A = full range				0.3		nA/°C

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

input characteristics

PARAMETER		TEST CONDITIONS†			MIN	TYP	MAX	UNIT
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V			±13.8	±14.3		V
		V_{CC} = ±5 V			±3.8	±4.3		
CMRR	Common mode rejection ratio	V_{CC} = ±15 V,	V_{ICR} = ±12 V	T_A = full range	70	100		dB
		V_{CC} = ±5 V,	V_{ICR} = ±2.5 V		70	100		
r_i	Input resistance					1		MΩ
C_i	Input capacitance					1.5		pF

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

output characteristics

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 250 Ω	±11.5	±13		V
		V_{CC} = ±5 V	R_L = 150 Ω	±3.2	±3.5		
		V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.6		V
		V_{CC} = ±5 V		±3.5	±3.8		
I_O	Output current‡	V_{CC} = ±15 V	R_L = 20 Ω	80	100		mA
		V_{CC} = ±5 V		50	75		
I_{SC}	Short-circuit current‡	V_{CC} = ±15 V			150		mA
R_O	Output resistance	Open loop			13		Ω

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

‡ Observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the absolute maximum ratings section of this data sheet for more information.

power supply

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (per amplifier)	V_{CC} = ±15 V	T_A = 25°C		8.5	10.5	mA
			T_A = full range			11.5	
		V_{CC} = ±5 V	T_A = 25°C		7.5	9.5	
			T_A = full range			10.5	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	70	84		dB
			T_A = full range	68			

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

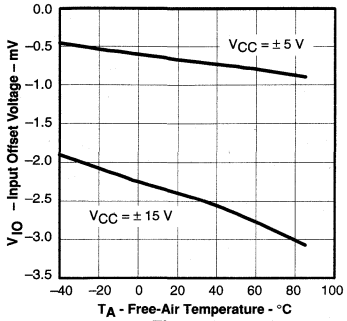


Figure 3

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

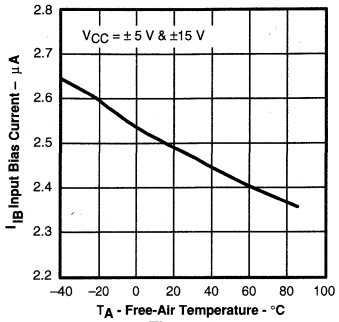


Figure 4

OUTPUT VOLTAGE vs SUPPLY VOLTAGE

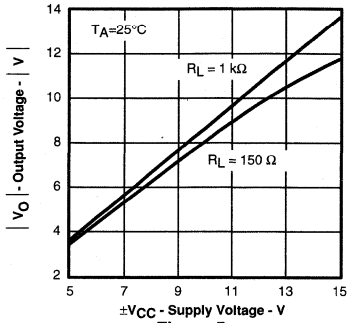


Figure 5

COMMON-MODE INPUT VOLTAGE vs SUPPLY VOLTAGE

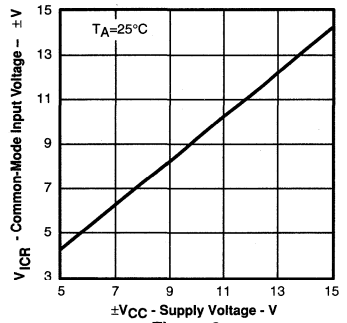


Figure 6

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

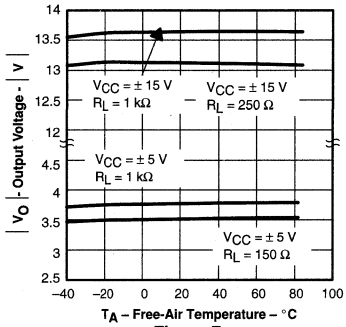


Figure 7

SUPPLY CURRENT vs SUPPLY VOLTAGE

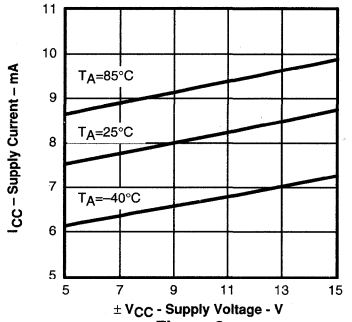


Figure 8

VOLTAGE & CURRENT NOISE vs FREQUENCY

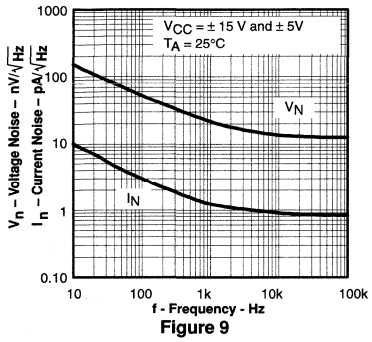


Figure 9

POWER SUPPLY REJECTION RATIO vs FREQUENCY

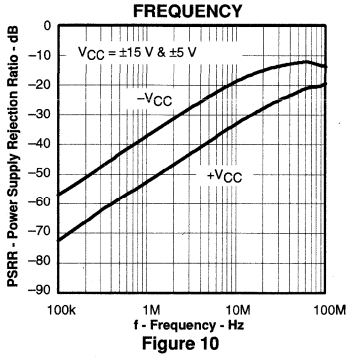


Figure 10

CMRR vs FREQUENCY

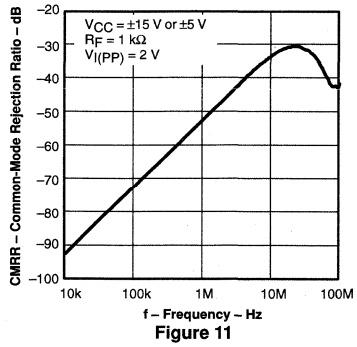


Figure 11

TYPICAL CHARACTERISTICS

CROSSTALK vs FREQUENCY

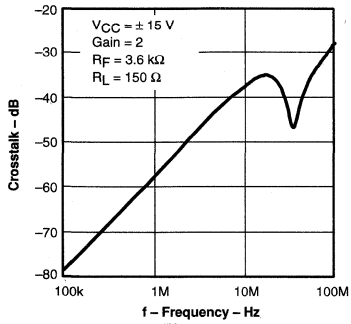


Figure 12

OPEN LOOP GAIN AND PHASE RESPONSE vs FREQUENCY

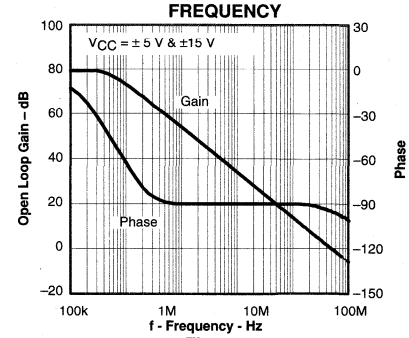


Figure 13

TOTAL HARMONIC DISTORTION vs FREQUENCY

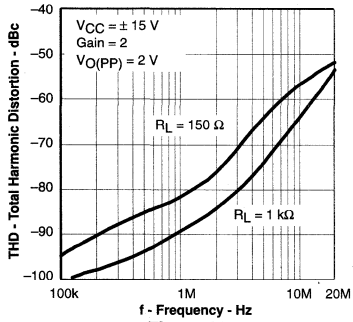


Figure 14

DISTORTION vs OUTPUT VOLTAGE

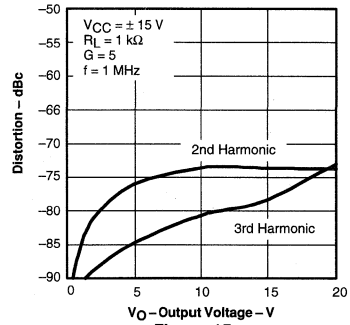


Figure 15

DISTORTION vs OUTPUT VOLTAGE

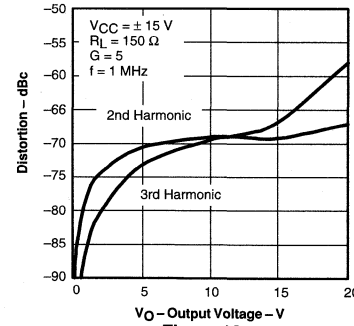


Figure 16

DISTORTION vs FREQUENCY

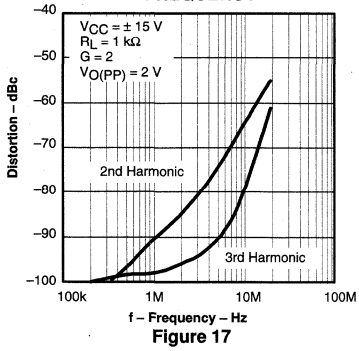


Figure 17

DISTORTION vs FREQUENCY

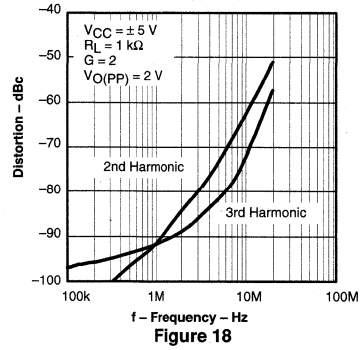


Figure 18

DISTORTION vs FREQUENCY

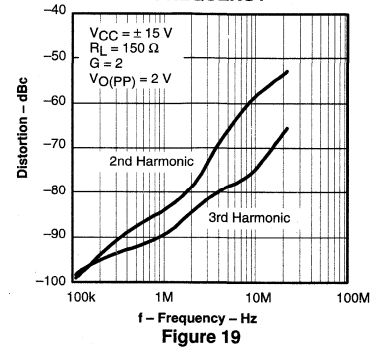


Figure 19

TYPICAL CHARACTERISTICS

DISTORTION vs FREQUENCY

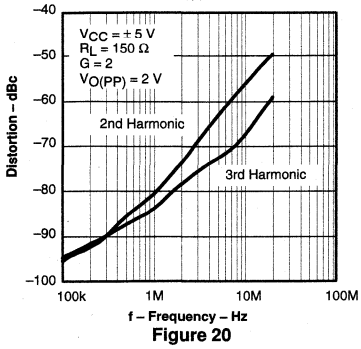


Figure 20

OUTPUT AMPLITUDE vs FREQUENCY

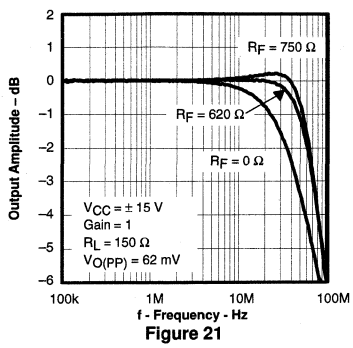


Figure 21

OUTPUT AMPLITUDE vs FREQUENCY

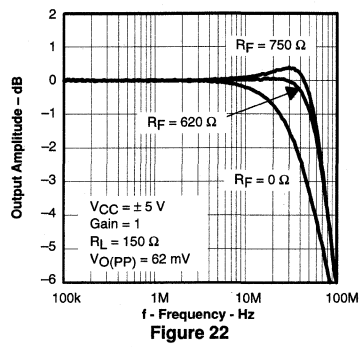


Figure 22

OUTPUT AMPLITUDE vs FREQUENCY

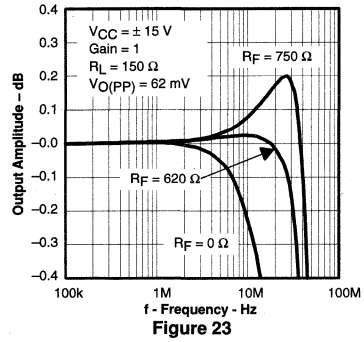


Figure 23

OUTPUT AMPLITUDE vs FREQUENCY

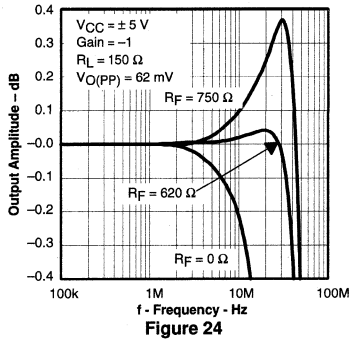


Figure 24

OUTPUT AMPLITUDE vs FREQUENCY

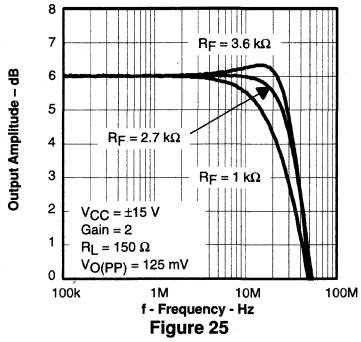


Figure 25

OUTPUT AMPLITUDE vs FREQUENCY

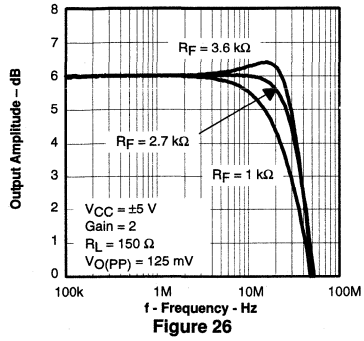


Figure 26

OUTPUT AMPLITUDE vs FREQUENCY

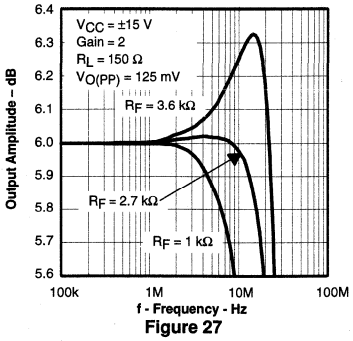


Figure 27

OUTPUT AMPLITUDE vs FREQUENCY

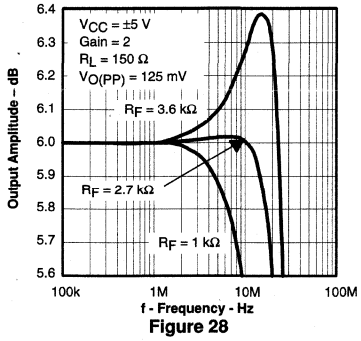


Figure 28

TYPICAL CHARACTERISTICS

OUTPUT AMPLITUDE vs FREQUENCY

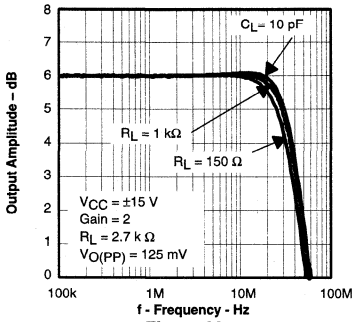


Figure 29

OUTPUT AMPLITUDE vs FREQUENCY

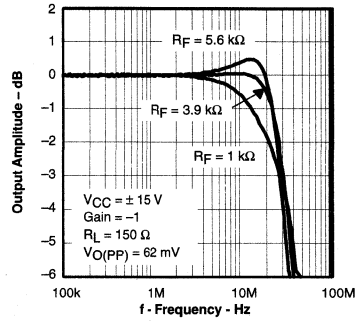


Figure 30

OUTPUT AMPLITUDE vs FREQUENCY

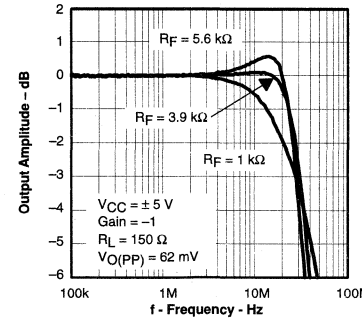


Figure 31

OUTPUT AMPLITUDE vs FREQUENCY

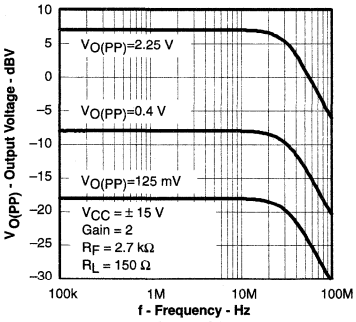


Figure 32

SETTING TIME vs OUTPUT STEP

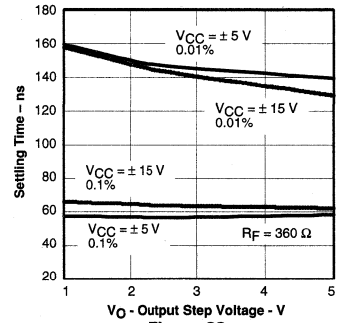


Figure 33

DIFFERENTIAL GAIN vs NUMBER OF 150-Ω LOADS

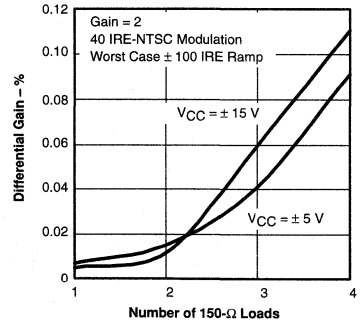


Figure 34

DIFFERENTIAL GAIN vs NUMBER OF 150-Ω LOADS

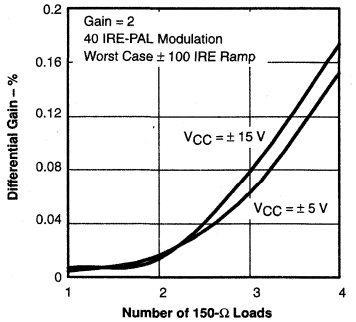


Figure 35

DIFFERENTIAL PHASE vs NUMBER OF 150-Ω LOADS

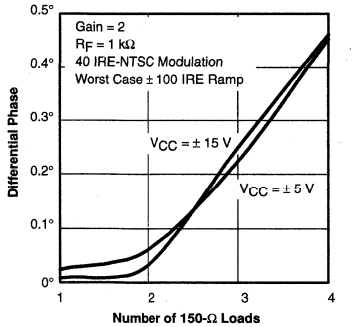


Figure 36

DIFFERENTIAL PHASE vs NUMBER OF 150-Ω LOADS

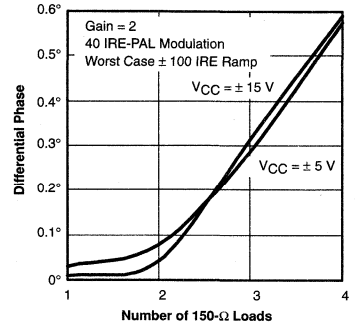


Figure 37

TYPICAL CHARACTERISTICS

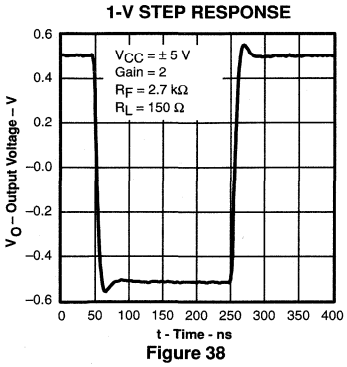


Figure 38

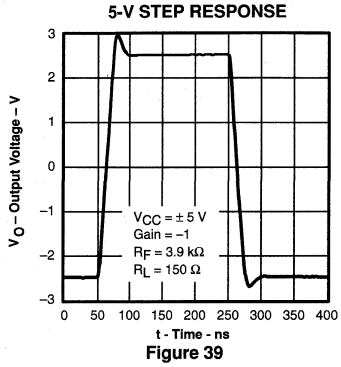


Figure 39

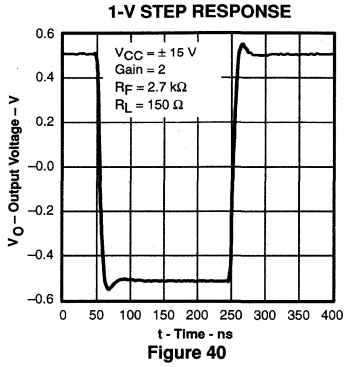


Figure 40

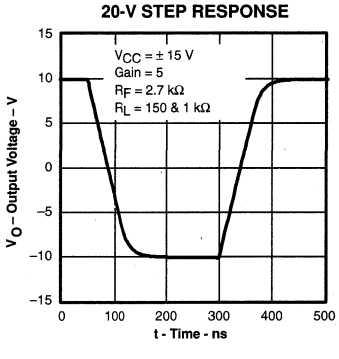


Figure 41

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

APPLICATION INFORMATION

theory of operation

The THS405x is a high-speed, operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This results in an exceptionally high performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 42.

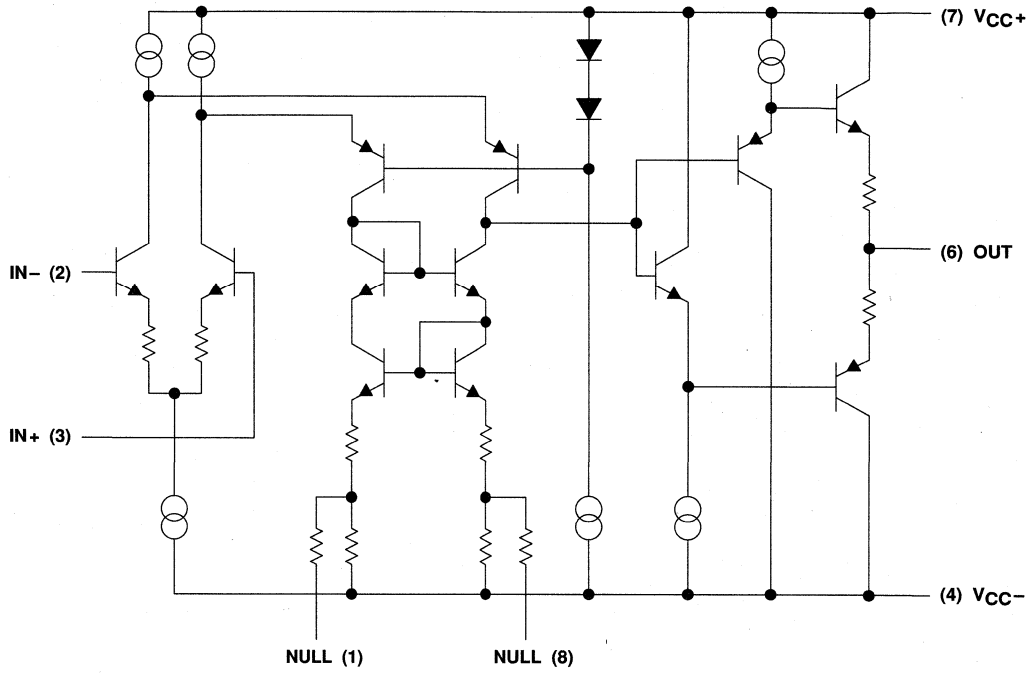


Figure 42. THS4051 Simplified Schematic

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true when amplifying small signals, where signal-to-noise ration (SNR) is very important. The noise model for the THS405x is shown in Figure 43. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise ($nV/\sqrt{Hz}$)
- IN+ = Noninverting current noise ($pA/\sqrt{Hz}$)
- IN– = Inverting current noise ($pA/\sqrt{Hz}$)
- e_{Rx} = Thermal voltage noise associated with each resistor ($e_{Rx} = 4\ kTR_x$)

APPLICATION INFORMATION

noise calculations and noise figure (continued)

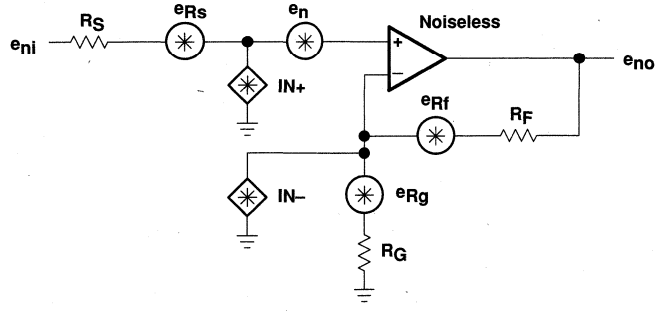


Figure 43. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN + \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\ kTR_s + 4\ kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\ A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (noninverting case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

For more information on noise analysis, please refer to the *Noise Analysis* section in *Operational Amplifier Circuits Applications Report* (literature number SLVA043).

APPLICATION INFORMATION

noise calculations and noise figure (continued)

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^2}{\left(e_{Rs}\right)^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\ kTR_S}\right]$$

Figure 44 shows the noise figure graph for the THS405x.

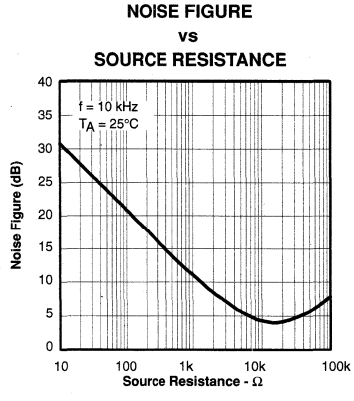


Figure 44. Noise Figure vs Source Resistance

APPLICATION INFORMATION

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS405x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 45. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

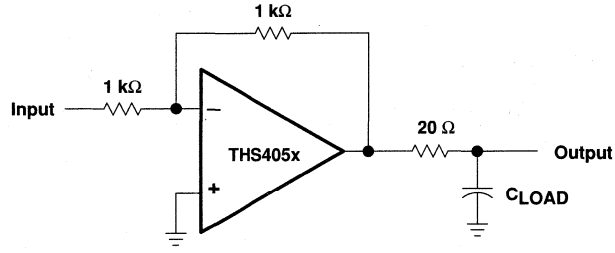


Figure 45. Driving a Capacitive Load

offset nulling

The THS405x has very low input offset voltage for a high-speed amplifier. However, if additional correction is required, an offset nulling function has been provided on the THS4051. The input offset can be adjusted by placing a potentiometer between terminals 1 and 8 of the device and tying the wiper to the negative supply. This is shown in Figure 46.

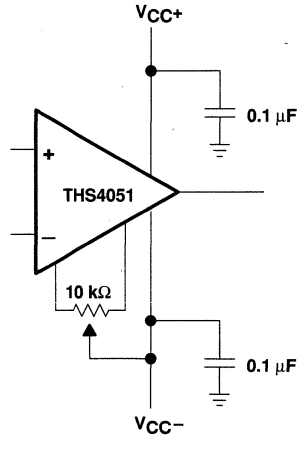
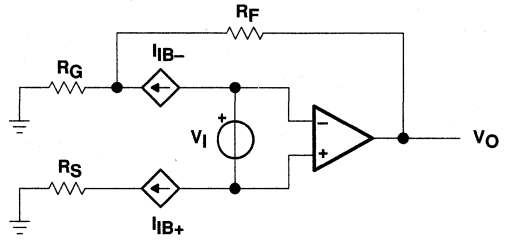


Figure 46. Offset Nulling Schematic

APPLICATION INFORMATION

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

Figure 47. Output Offset Voltage Model

optimizing unity gain response

Internal frequency compensation of the THS405x was selected to provide very wideband performance yet still maintain stability when operated in a noninverting unity gain configuration. When amplifiers are compensated in this manner there is usually peaking in the closed loop response and some ringing in the step response for very fast input edges, depending upon the application. This is because a minimum phase margin is maintained for the G=+1 configuration. For optimum settling time and minimum ringing, a feedback resistor of 620 Ω should be used as shown in Figure 48. Additional capacitance can also be used in parallel with the feedback resistance if even finer optimization is required.

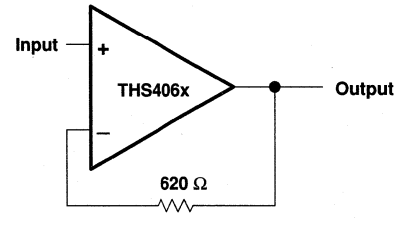


Figure 48. Noninverting, Unity Gain Schematic

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 49).

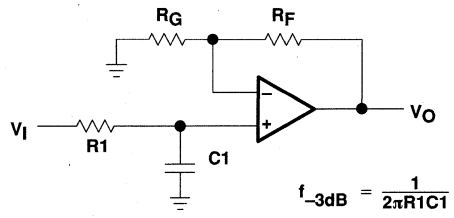


Figure 49. Single-Pole Low-Pass Filter

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

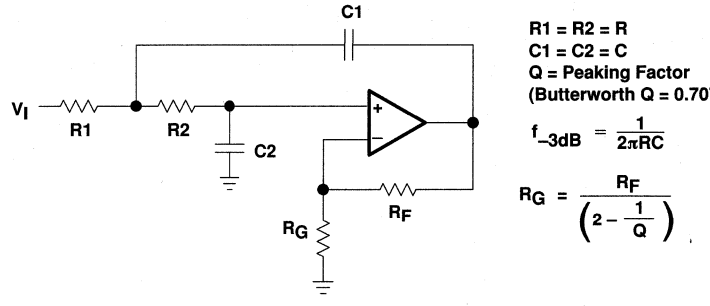


Figure 50. 2-Pole Low-Pass Sallen-Key Filter

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high frequency performance of the THS405x, follow proper printed-circuit board high frequency design techniques. A general set of guidelines is given below. In addition, a THS405x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

general PowerPAD design considerations

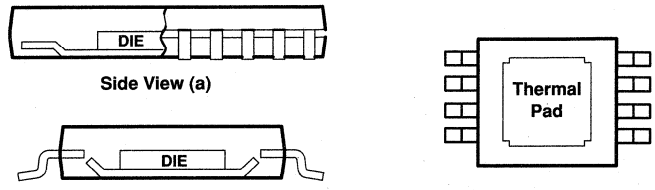
The THS405x is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 51(a) and Figure 51(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 51(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the, heretofore, awkward mechanical methods of heatsinking.

APPLICATION INFORMATION

general PowerPAD design considerations (continued)



NOTE A. The thermal pad is electrically isolated from all terminals in the package.

Figure 51. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach.

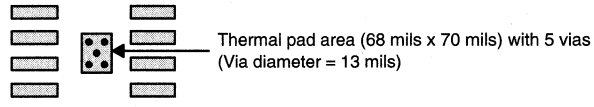


Figure 52. PowerPAD PCB Etch and Via Pattern

1. Prepare the PCB with a top side etch pattern as shown in Figure 52. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS405xDGN IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS405xDGN package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the THS405xDGN IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

APPLICATION INFORMATION

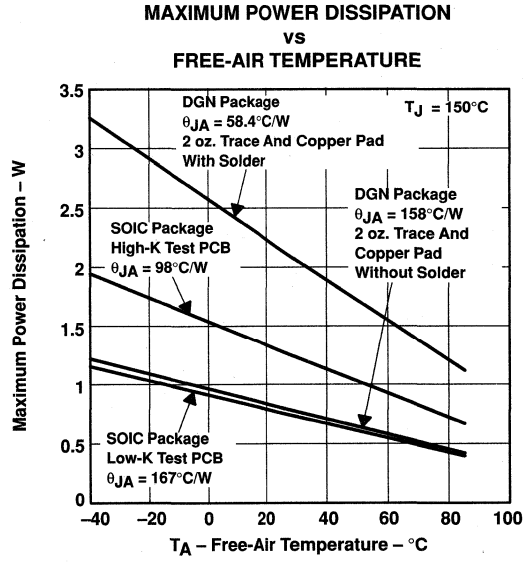
general PowerPAD design considerations (continued)

The actual thermal performance achieved with the THS405xDGN in its PowerPAD package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA}, is about 58.4°C/W. For comparison, the non-PowerPAD version of the THS405x IC (SOIC) is shown. For a given θ_{JA}, the maximum power dissipation is shown in Figure 53 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS405x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A. Results are with no air flow and PCB size = 3"× 3"

Figure 53. Maximum Power Dissipation vs Free-Air Temperature

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially devices with multiple amplifiers. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 54 to Figure 57 show this effect, along with the quiescent heat, with an ambient air temperature of 50°C. Obviously, as the ambient temperature increases, the limit lines shown will drop accordingly. The area under each respective limit line is considered the safe operating area. Any condition above this line will exceed the amplifier's limits and failure may result. When using V_{CC} = ±5 V, there is generally not a heat problem, even with SOIC packages. But, when using V_{CC} = ±15 V, the SOIC package is severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual amplifier package (THS4052), the sum of the RMS output currents and voltages should be used to choose the proper package. The graphs shown assume that both amplifier's outputs are identical.

THS4051
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

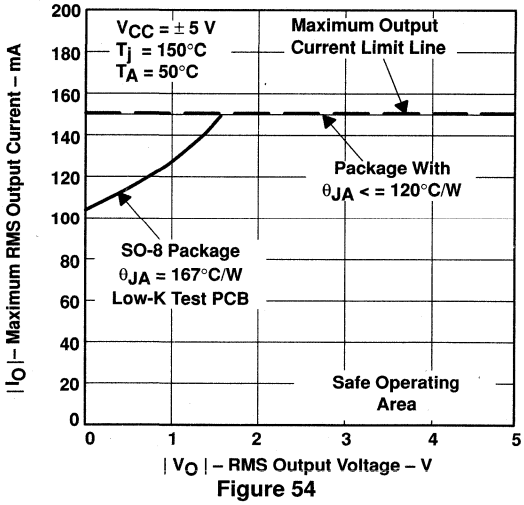


Figure 54

THS4051
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

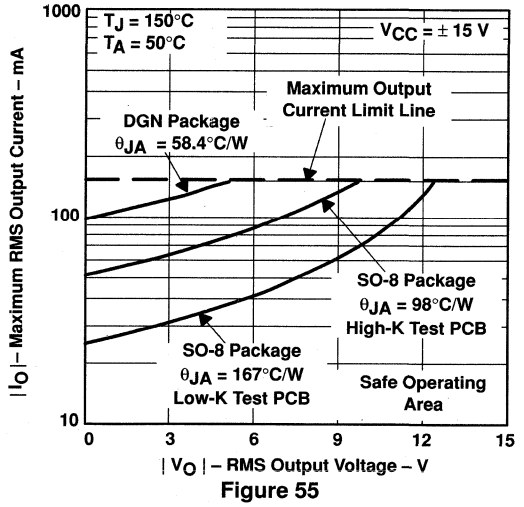


Figure 55

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

THS4052
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

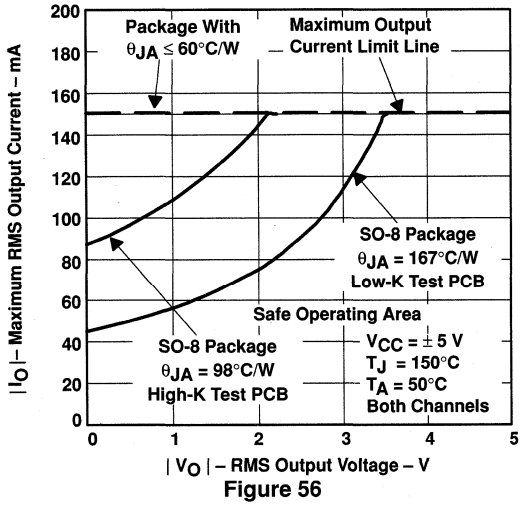


Figure 56

THS4052
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

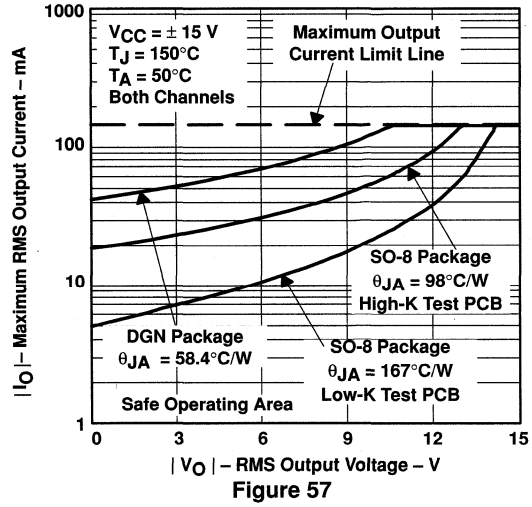


Figure 57

APPLICATION INFORMATION

evaluation board

An evaluation board is available for the THS4051 (literature number SLOP220) and THS4052 (literature number SLOP234). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 58. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. For more information, please refer to the *THS4051 EVM User's Guide* or the *THS4052 EVM User's Guide*. To order the evaluation board, contact your local TI sales office or distributor.

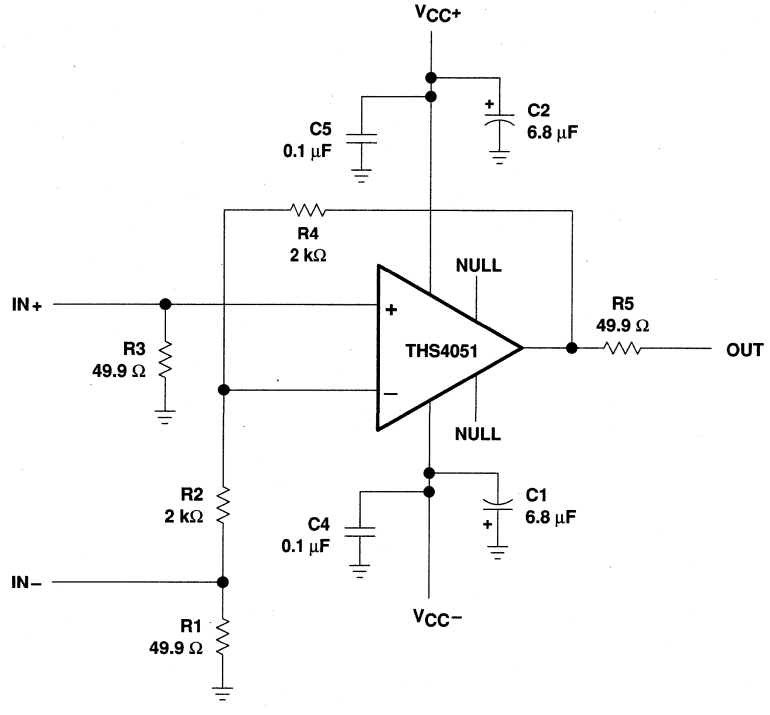
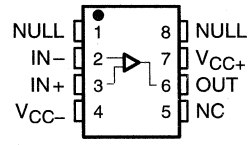


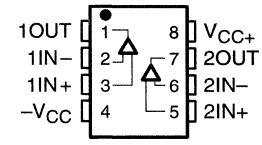
Figure 58. THS4051 Evaluation Board

- **High Speed**
  - **180 MHz Bandwidth (G = 1, –3 dB)**
  - **400 V/μs Slew Rate**
  - **40-ns Settling Time (0.1%)**
- **High Output Drive, I_O = 115 mA (typ)**
- **Excellent Video Performance**
  - **75 MHz 0.1 dB Bandwidth (G = 1)**
  - **0.02% Differential Gain**
  - **0.02° Differential Phase**
- **Very Low Distortion**
  - **THD = –72 dBc at f = 1 MHz**
- **Wide Range of Power Supplies**
  - **V_{CC} = ±5 V to ±15 V**
- **Available in Standard SOIC, MSOP PowerPAD™, JG, or FK Package**
- **Evaluation Module Available**

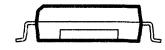
THS4061
JG, D AND DGN PACKAGE
(TOP VIEW)



THS4062
D AND DGN PACKAGE
(TOP VIEW)

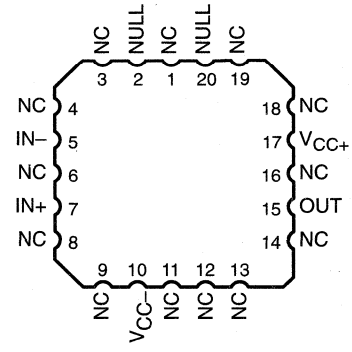


NC – No internal connection



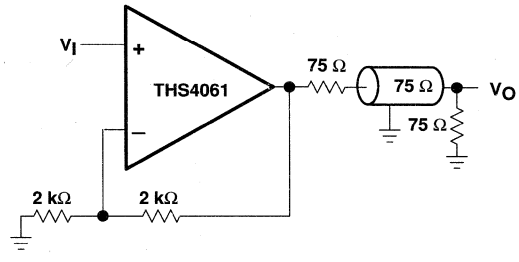
Cross-Section View Showing
PowerPAD Option (DGN)

THS4061
FK PACKAGE
(TOP VIEW)



description

The THS4061 and THS4062 are general-purpose, single/dual, high-speed voltage feedback amplifiers ideal for a wide range of applications including video, communication, and imaging. The devices offer very good ac performance with 180-MHz bandwidth, 400-V/μs slew rate, and 40-ns settling time (0.1%). The THS4061/2 are stable at all gains for both inverting and noninverting configurations. These amplifiers have a high output drive capability of 115 mA and draw only 7.8 mA supply current per channel. Excellent professional video results can be obtained with the low differential gain/phase errors of 0.02%/0.02° and wide 0.1 db flatness to 75 MHz. For applications requiring low distortion, the THS4061/2 is ideally suited with total harmonic distortion of –72 dBc at f = 1 MHz.



LINE DRIVER (G = 2)

CAUTION: The THS4061 and THS4062 provide ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality

PowerPAD is a trademark of Texas Insruments Incorporated.

RELATED DEVICES	
DEVICE	**DESCRIPTION**
THS4011/2	290-MHz Low Distortion High-Speed Amplifiers
THS4031/2	100-MHz Low Noise High Speed-Amplifiers
THS4061/2	180-MHz High-Speed Amplifiers

AVAILABLE OPTIONS

T_A	NUMBER OF CHANNELS	PACKAGED DEVICES				MSOP SYMBOL	EVALUATION MODULES
		PLASTIC SMALL OUTLINE† (D)	PLASTIC MSOP† (DGN)	CERAMIC DIP (JG)	CHIP CARRIER (FK)		
0°C to 70°C	1	THS4061CD	THS4061CDGN	—	—	TIABS	THS4061EVM
	2	THS4062CD	THS4062CDGN	—	—	TIABM	THS4062EVM
–40°C to 85°C	1	THS4061ID	THS4061IDGN	—	—	TIABT	—
	2	THS4062ID	THS4062IDGN	—	—	TIABN	—
–55°C to 125°C	1	—	—	THS4061MJG	THS4061MFK	—	—

† The D and DGN packages are available taped and reeled. Add an R suffix to the device type (i.e., THS4061CDGNR).

functional block diagram

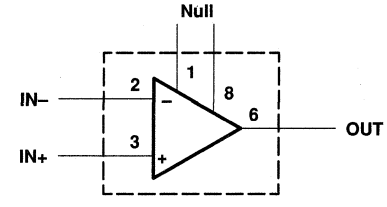


Figure 1. THS4061 – Single Channel

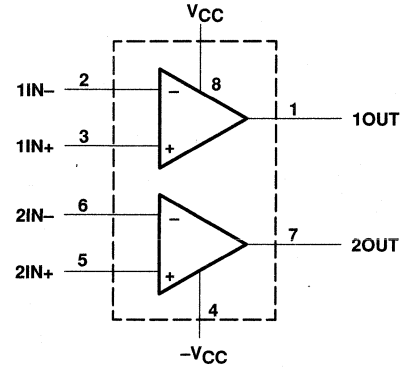


Figure 2. THS4062 – Dual Channel

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, $V_{CC}+$ to $V_{CC}-$ ..... 33 V
Input voltage, V_I ..... $\pm V_{CC}$
Output current, I_O ..... 150 mA
Differential input voltage, V_{IO} ..... ±4 V
Continuous total power dissipation ..... See Dissipation Rating Table
Maximum junction temperature, T_J ..... 150°C
Operating free-air temperature, T_A: C-suffix ..... 0°C to 70°C
I-suffix ..... –40°C to 85°C
M-suffix ..... –55°C to 125°C
Storage temperature, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds, D and DGN package ..... 300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds, JG package ..... 300°C
Case temperature for 60 seconds, FK package ..... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	740 mW	6 mW/°C	475 mW	385 mW	—
DGN‡	2.14 W	17.1 mW/°C	1.37 W	1.11 W	—
JG	1057 mW	8.4 mW/°C	627 mW	546 mW	210 mW
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW

‡ The DGN package incorporates a PowerPAD on the underside of the device. This acts as a heatsink and must be connected to a thermal dissipation plane for proper power dissipation. Failure to do so can result in exceeding the maximum specified junction temperature, which could permanently damage the device.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}+$ and $V_{CC}-$	Dual supply	±4.5		±16	V
	Single supply	9		32	
Operating free-air temperature, T_A	C-suffix	0		70	°C
	I-suffix	–40		85	
	M-suffix	–55		125	

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS†		THS4061C/I, THS4062C/I MIN	TYP	MAX	UNIT
BW	Dynamic performance small-signal bandwidth (–3 dB)	V_{CC} = ±5 V	Gain = 1		180		MHz
		V_{CC} = ±15 V	Gain = –1		50		MHz
		V_{CC} = ±5 V			50		
	Bandwidth for 0.1 dB flatness	V_{CC} = ±15 V	Gain = 1		75		MHz
		V_{CC} = ±5 V			20		
SR	Slew rate	V_{CC} = ±15 V	Gain = –1		400		V/µs
		V_{CC} = ±5 V			350		
t_s	Settling time to 0.1%	V_{CC} = ±15 V, 5-V step (0 V to 5 V)	Gain = –1		40		ns
		V_{CC} = ±5 V, V_O = –2.5 V to 2.5 V,			40		
	Settling time to 0.01%	V_{CC} = ±15 V, 5-V step (0 V to 5 V)	Gain = –1		140		ns
		V_{CC} = ±5 V, V_O = –2.5 V to 2.5 V,			150		

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

noise/distortion performance

PARAMETER		TEST CONDITIONS†		THS4061C/I, THS4062C/I MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	f = 1 MHz			–72		dBc
V_n	Input voltage noise	f = 10 kHz, V_{CC} = ±5 V or ±15 V			14.5		nV/√Hz
I_n	Input current noise	f = 10 kHz, V_{CC} = ±5 V or ±15 V			1.6		pA/√Hz
	Differential gain error	Gain = 2, NTSC, 40 IRE modulation	V_{CC} = ±15 V		0.02 %		
			V_{CC} = ±5 V		0.02 %		
	Differential phase error	Gain = 2, NTSC, 40 IRE modulation	V_{CC} = ±15 V		0.02°		
			V_{CC} = ±5 V		0.06°		
	Channel-to-channel crosstalk (THS4062 only)	V_{CC} = ±5 V or ±15 V, f = 1 MHz			65		dB

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

dc performance

PARAMETER		TEST CONDITIONS†		THS4061C/I, THS4062C/I MIN	TYP	MAX	UNIT
	Open loop gain	V_{CC} = ±15 V, V_O = ±10 V, R_L = 1 kΩ	T_A = 25°C	5	15		V/mV
			T_A = full range	4			
		V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 1 kΩ	T_A = 25°C	2.5	8		V/mV
			T_A = full range	2			
V_{OS}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = full range		2.5	8	mV
	Offset drift	V_{CC} = ±5 V or ±15 V			15		µV/°C
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V	T_A = full range		3	6	µA
I_{OS}	Input offset current	V_{CC} = ±5 V or ±15 V	T_A = full range		75	250	nA
	Offset current drift	T_A = full range			0.3		nA/°C

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

input characteristics

PARAMETER		TEST CONDITIONS†			THS4061C/I, THS4062C/I			UNIT
					MIN	TYP	MAX	
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V			±13.8	±14.1		V
		V_{CC} = ±5 V			±3.8	±4.3		
CMRR	Common mode rejection ratio	V_{CC} = ±15 V,	V_{ICR} = ±12 V	T_A = full range	70	110		dB
		V_{CC} = ±5 V,	V_{ICR} = ±2.5 V		70	95		
R_I	Input resistance					1		MΩ
C_i	Input capacitance					2		pF

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

output characteristics

PARAMETER		TEST CONDITIONS†		THS4061C/I, THS4062C/I			UNIT
				MIN	TYP	MAX	
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 250 Ω	±11.5	±12.5		V
		V_{CC} = ±5 V	R_L = 150 Ω	±3.2	±3.5		
		V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.5		V
		V_{CC} = ±5 V		±3.5	±3.7		
I_O	Output current	V_{CC} = ±15 V	R_L = 20 Ω	80	115		mA
		V_{CC} = ±5 V		50	75		
I_{SC}	Short-circuit current	V_{CC} = ±15 V			150		mA
R_O	Output resistance	Open loop			12		Ω

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

power supply

PARAMETER		TEST CONDITIONS†		THS4061C/I, THS4062C/I			UNIT
				MIN	TYP	MAX	
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Quiescent current (per amplifier)	V_{CC} = ±15 V	T_A = full range		7.8	10.5	mA
		V_{CC} = ±5 V			7.3	10	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	70	78		dB
			T_A = full range	68			

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS†		THS4061M MIN	THS4061M TYP	THS4061M MAX	UNIT
BW	Unity-gain bandwidth	Closed loop, R_L = 1 kΩ	V_{CC} = ±15 V	*140	180		MHz
	Dynamic performance small-signal bandwidth (–3 dB)	V_{CC} = ±15 V	Gain = 1		180		MHz
		V_{CC} = ±5 V			180		
		V_{CC} = ±15 V	Gain = –1		50		MHz
		V_{CC} = ±5 V			50		
	Bandwidth for 0.1 dB flatness	V_{CC} = ±15 V	Gain = 1		75		MHz
		V_{CC} = ±5 V			20		
SR	Slew rate	V_{CC} = ±15 V R_L = 1 kΩ		*400	500		V/μs
t_s	Settling time to 0.1%	V_{CC} = ±15 V, 5-V step (0 V to 5 V)	Gain = –1		40		ns
		V_{CC} = ±5 V, V_O = –2.5 V to 2.5 V,			40		
	Settling time to 0.01%	V_{CC} = ±15 V, 5-V step (0 V to 5 V)	Gain = –1		140		ns
		V_{CC} = ±5 V, V_O = –2.5 V to 2.5 V,			150		

† Full range = –55°C to 125°C for M suffix
*This parameter is not tested.

noise/distortion performance

PARAMETER		TEST CONDITIONS†		THS4061M MIN	THS4061M TYP	THS4061M MAX	UNIT
THD	Total harmonic distortion	f = 1 MHz			–72		dBc
V_n	Input voltage noise	f = 10 kHz, V_{CC} = ±5 V or ±15 V			14.5		nV/√Hz
I_n	Input current noise	f = 10 kHz, V_{CC} = ±5 V or ±15 V			1.6		pA/√Hz
	Differential gain error	Gain = 2, NTSC, 40 IRE Modulation	V_{CC} = ±15 V		0.02		%
			V_{CC} = ±5 V		0.02		
	Differential phase error	Gain = 2, NTSC, 40 IRE Modulation	V_{CC} = ±15 V		0.02°		
			V_{CC} = ±5 V		0.06°		

† Full range = –55°C to 125°C for M suffix

dc performance

PARAMETER		TEST CONDITIONS†		THS4061M MIN	THS4061M TYP	THS4061M MAX	UNIT
	Open loop gain	V_{CC} = ±15 V, V_O = ±10 V, R_L = 1 kΩ	T_A = full range	5	9		V/mV
		V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 1 kΩ		2.5	6		
V_{IO}	Input offset voltage	V_{CC} = ±5 V or ±15 V R_L = 1 kΩ	T_A = 25°C		2.5	8	mV
			T_A = full range			9	mV
	Offset drift	V_{CC} = ±5 V or ±15 V R_L = 1 kΩ	T_A = full range		15		μV/°C
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V R_L = 1 kΩ	T_A = full range		3	6	μA
I_{IO}	Input offset current	V_{CC} = ±5 V or ±15 V R_L = 1 kΩ	T_A = full range		75	250	nA
	Offset current drift	V_{CC} = ±5 V or ±15 V R_L = 1 kΩ	T_A = full range		0.3		nA/°C

† Full range = –55°C to 125°C for M suffix

electrical characteristics at T_A = full range, V_{CC} = ±15 V, R_L = 1 kΩ (unless otherwise noted) (continued)

input characteristics

PARAMETER		TEST CONDITIONS†		THS4061M			UNIT
				MIN	TYP	MAX	
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V		±13.8	±14.1		V
		V_{CC} = ±5 V		±3.8	±4.3		
CMRR	Common mode rejection ratio	V_{CC} = ±15 V,	V_{ICR} = ±12 V	70	86		dB
		V_{CC} = ±5 V,	V_{ICR} = ±2.5 V	80	90		
R_I	Input resistance				1		MΩ
C_i	Input capacitance				2		pF

† Full range = –55°C to 125°C for M suffix

output characteristics

PARAMETER		TEST CONDITIONS†		THS4061M			UNIT
				MIN	TYP	MAX	
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 250 Ω	±12	±13.1		V
		V_{CC} = ±5 V	R_L = 150 Ω	±3.2	±3.5		
		V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.5		V
		V_{CC} = ±5 V		±3.5	±3.7		
I_O	Output current	V_{CC} = ±15 V	R_L = 20 Ω	70	115		mA
		V_{CC} = ±5 V		50	75		
I_{SC}	Short-circuit current	V_{CC} = ±15 V	T_A = 25°C		150		mA
R_O	Output resistance	Open loop			12		Ω

† Full range = –55°C to 125°C for M suffix

power supply

PARAMETER		TEST CONDITIONS†		THS4061M			UNIT
				MIN	TYP	MAX	
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Quiescent current	V_{CC} = ±15 V	T_A = 25°C		7.8	9	mA
		V_{CC} = ±5 V			7.3	8.5	
		V_{CC} = ±15 V	T_A = full range			11	
		V_{CC} = ±5 V				10.5	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	76	80		dB
			T_A = full range	74	78		

† Full range = –55°C to 125°C for M suffix

TYPICAL CHARACTERISTICS

			FIGURE
I_{IB}	Input bias current	vs Free-air temperature	3
V_{IO}	Input offset voltage	vs Free-air temperature	4
	Open-loop gain	vs Frequency	5
	Phase	vs Frequency	5
	Differential gain	vs Number of loads	6, 8
	Differential phase	vs Number of loads	7, 9
	Closed-loop gain	vs Frequency	10, 11
	Output Amplitude	vs Frequency	12, 13
CMRR	Common-mode rejection ratio	vs Frequency	14
PSRR	Power-supply rejection ratio	vs Frequency	15
		vs Free-air temperature	16
$V_{O(PP)}$	Output voltage swing	vs Supply voltage	17
I_{CC}	Supply current	vs Free-air temperature	18
E_{nv}	Noise spectral density	vs Frequency	19
THD	Total harmonic distortion	vs Frequency	20, 21

TYPICAL CHARACTERISTICS

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

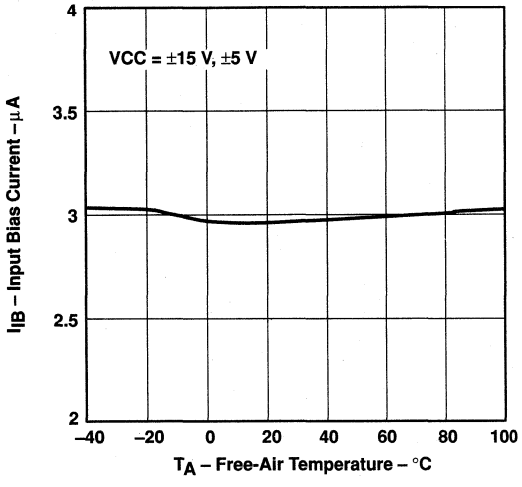


Figure 3

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

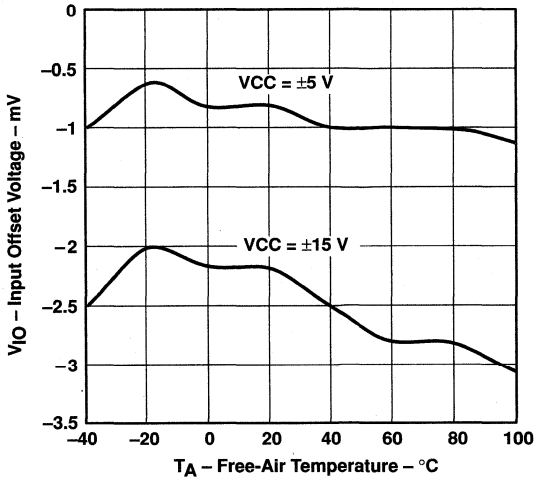


Figure 4

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

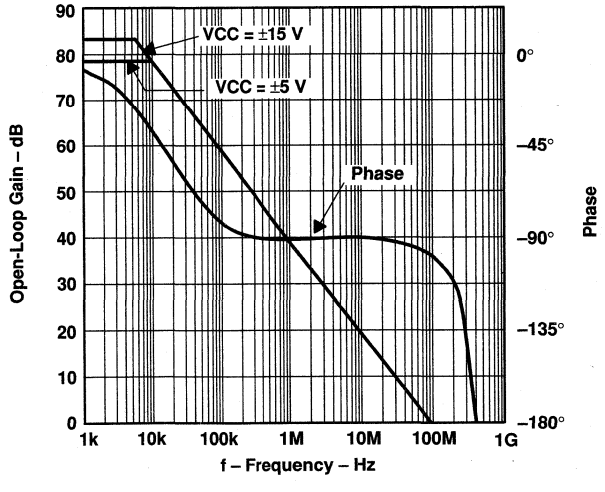


Figure 5

TYPICAL CHARACTERISTICS

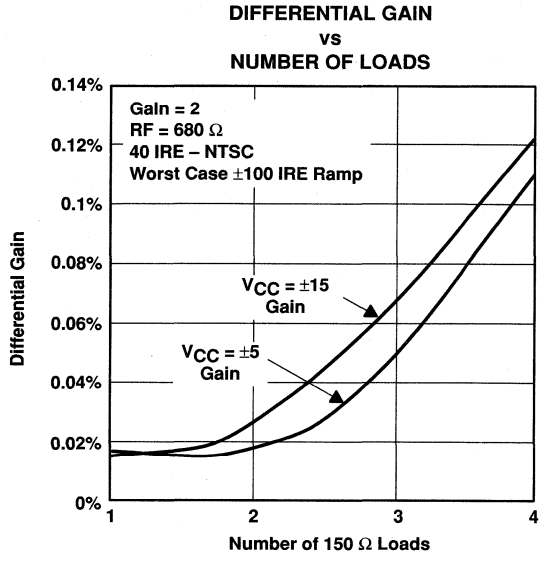


Figure 6

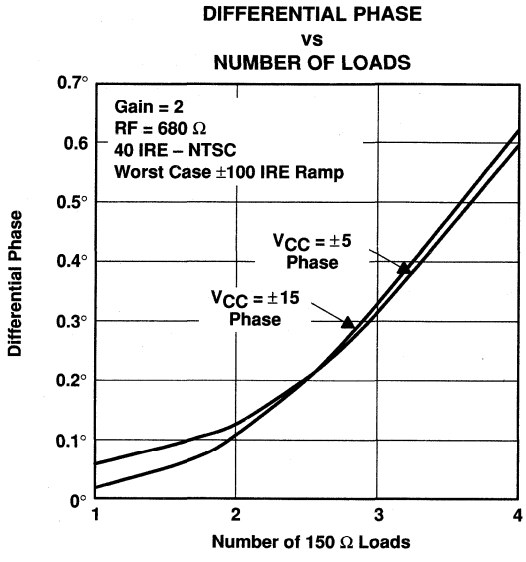


Figure 7

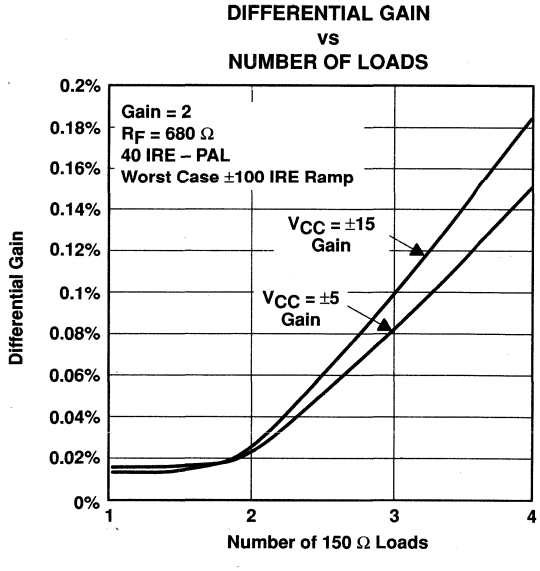


Figure 8

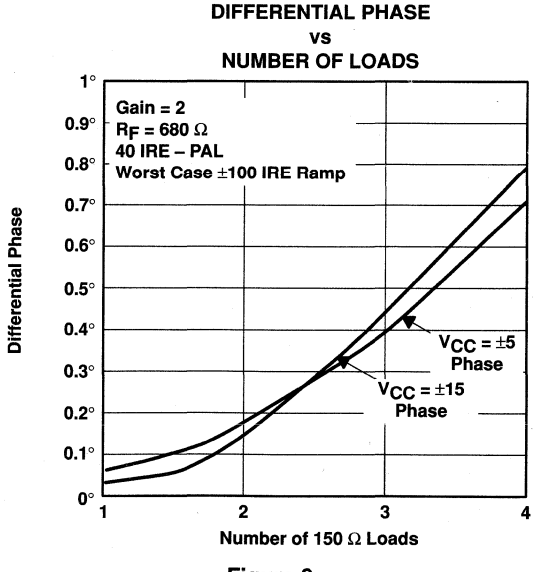


Figure 9

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN
vs
FREQUENCY

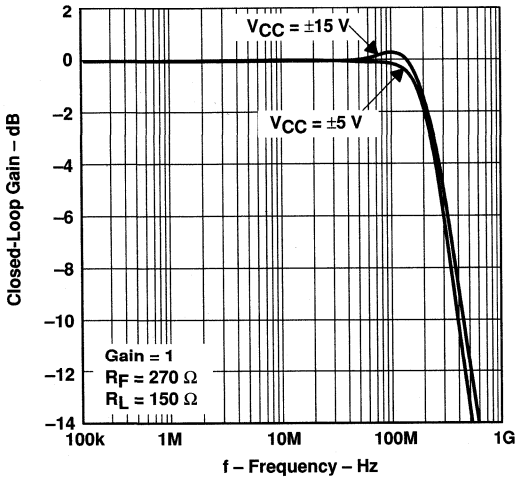


Figure 10

CLOSED-LOOP GAIN
vs
FREQUENCY

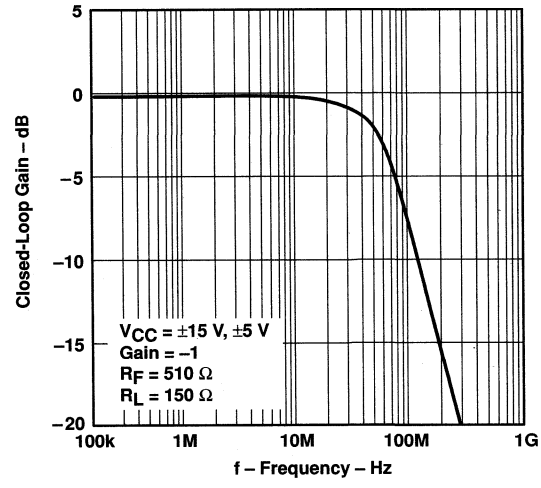


Figure 11

OUTPUT AMPLITUDE
vs
FREQUENCY

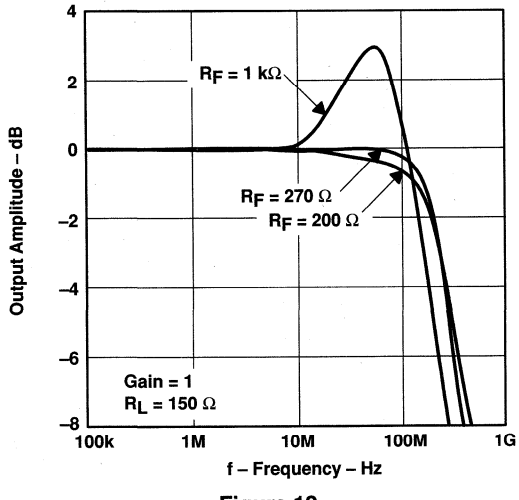


Figure 12

OUTPUT AMPLITUDE
vs
FREQUENCY

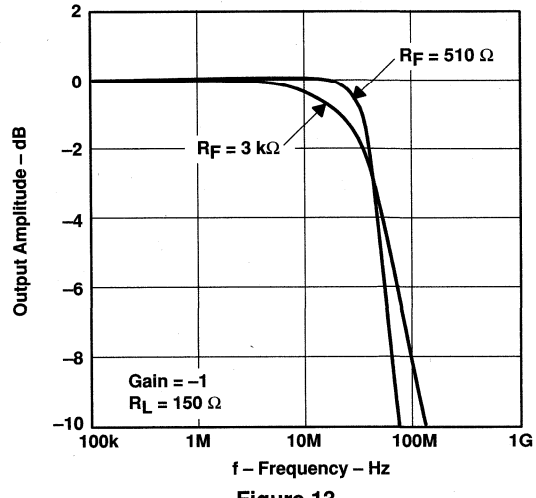


Figure 13

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

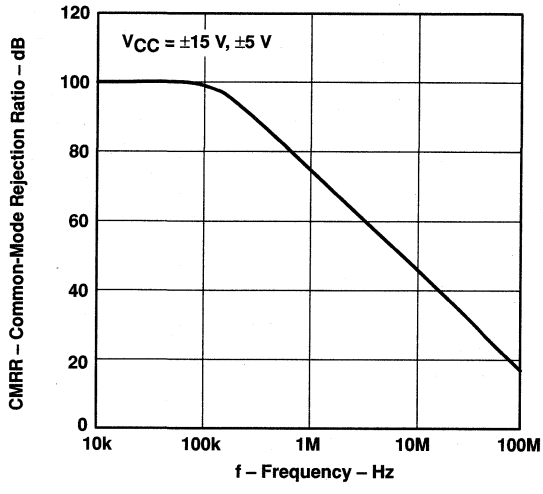


Figure 14

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

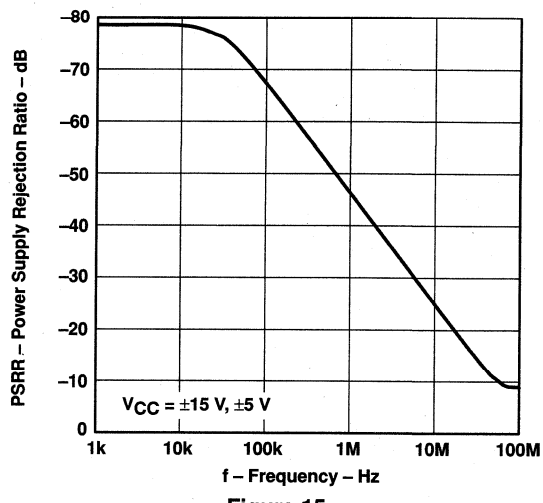


Figure 15

POWER SUPPLY REJECTION RATIO
vs
FREE-AIR TEMPERATURE

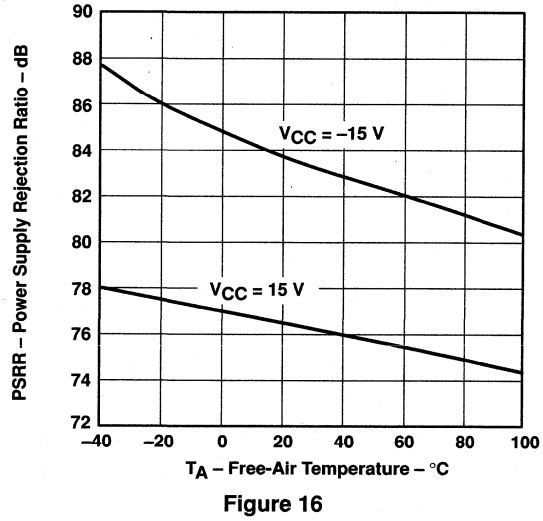


Figure 16

OUTPUT VOLTAGE SWING
vs
SUPPLY VOLTAGE

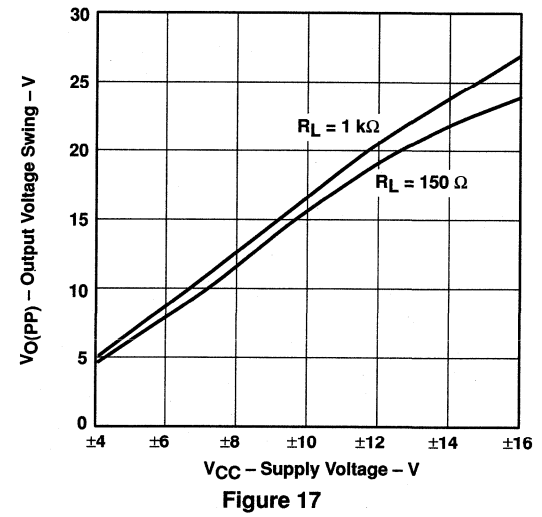


Figure 17

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

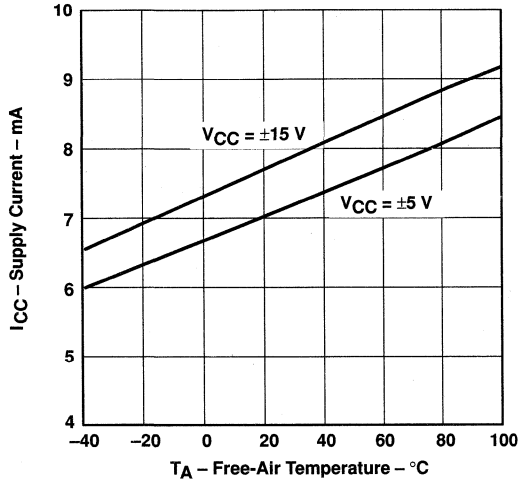


Figure 18

NOISE SPECTRAL DENSITY
vs
FREQUENCY

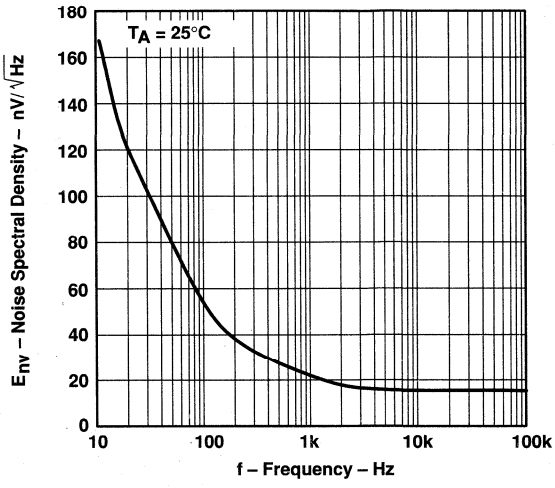


Figure 19

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

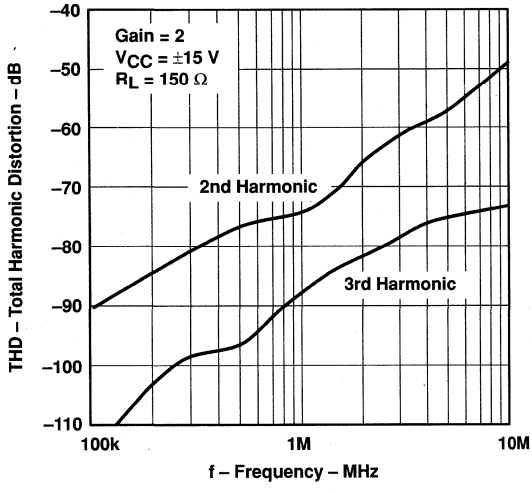


Figure 20

TOTAL HARMONIC DISTORTION
vs
FREQUENCY

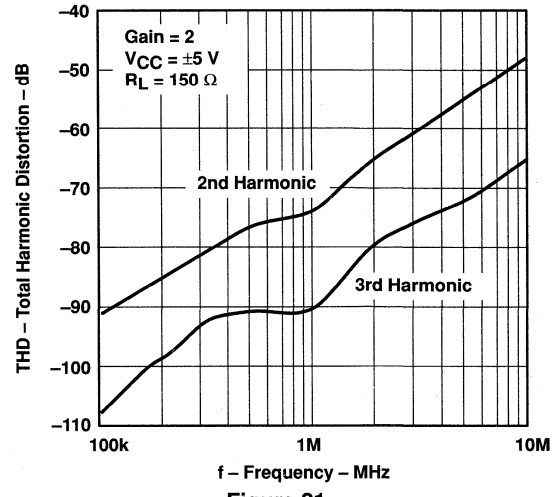


Figure 21

APPLICATION INFORMATION

theory of operation

The THS406x is a high speed, operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This results in an exceptionally high performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 22.

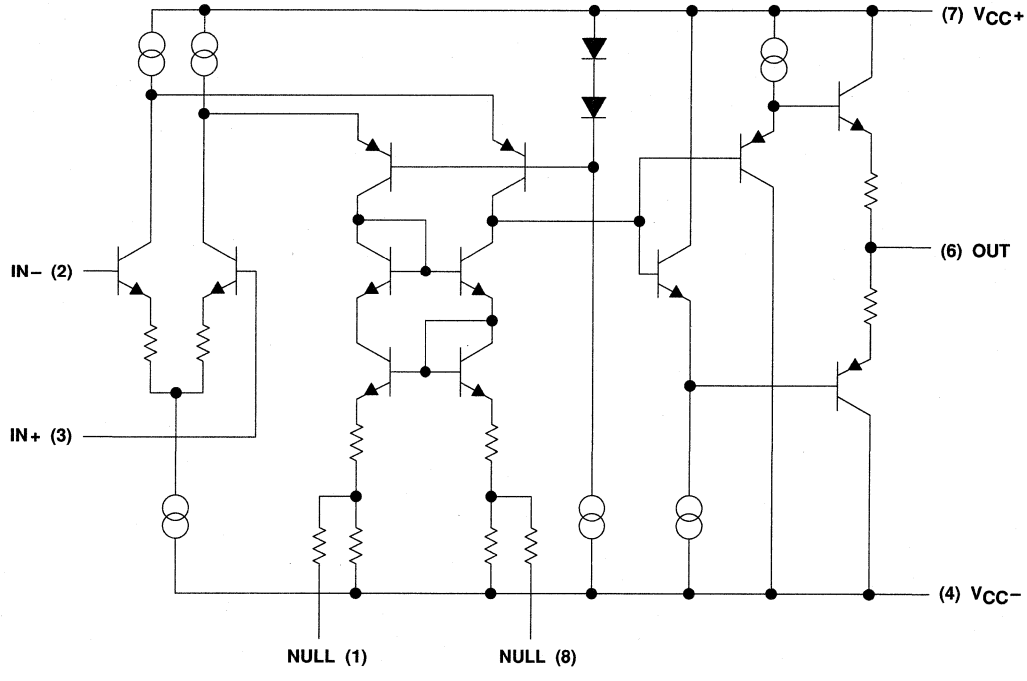


Figure 22. THS4061 Simplified Schematic

APPLICATION INFORMATION

offset nulling

The THS4061 has very low input offset voltage for a high-speed amplifier. However, if additional correction is required, an offset nulling function has been provided. By placing a potentiometer between terminals 1 and 8 and tying the wiper to the negative supply, the input offset can be adjusted. This is shown in Figure 23.

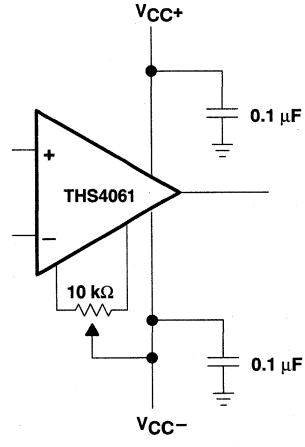


Figure 23. Offset Nulling Schematic

optimizing unity gain response

Internal frequency compensation of the THS406x was selected to provide very wideband performance yet still maintain stability when operated in a noninverting unity gain configuration. When amplifiers are compensated in this manner there is usually peaking in the closed loop response and some ringing in the step response for very fast input edges, depending upon the application. This is because a minimum phase margin is maintained for the G=+1 configuration. For optimum settling time and minimum ringing, a feedback resistor of 270 Ω should be used as shown in Figure 24. Additional capacitance can also be used in parallel with the feedback resistance if even finer optimization is required.

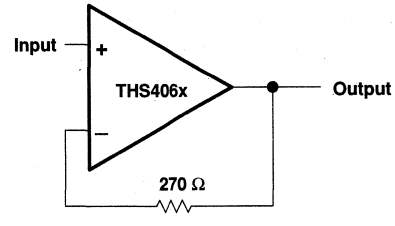


Figure 24. Noninverting, Unity Gain Schematic

APPLICATION INFORMATION

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS406x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 25. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

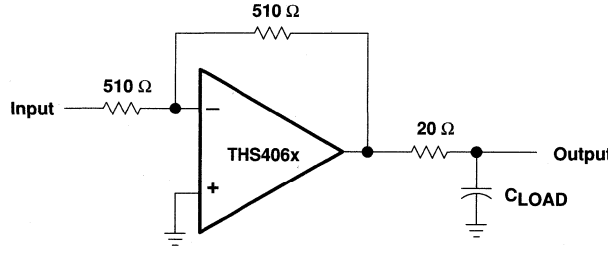


Figure 25. Driving a Capacitive Load

circuit layout considerations

In order to achieve the levels of high frequency performance of the THS406x, it is essential that proper printed-circuit board high frequency design techniques be followed. A general set of guidelines is given below. In addition, a THS406x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distances increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.

APPLICATION INFORMATION

circuit layout considerations (continued)

- Surface-mount passive components – Using surface-mount passive components is recommended for high-frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

evaluation board

An evaluation board is available for the THS4061 (literature number SLOP226) and THS4062 (literaure number SLOP235). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 26. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. To order the evaluation board contact your local TI sales office or distributor. For more detailed information, refer to the *THS4061 EVM User's Manual* (literature number SLOU038) or the *THS4062 EVM User's Manual* (literature number SLOU040)

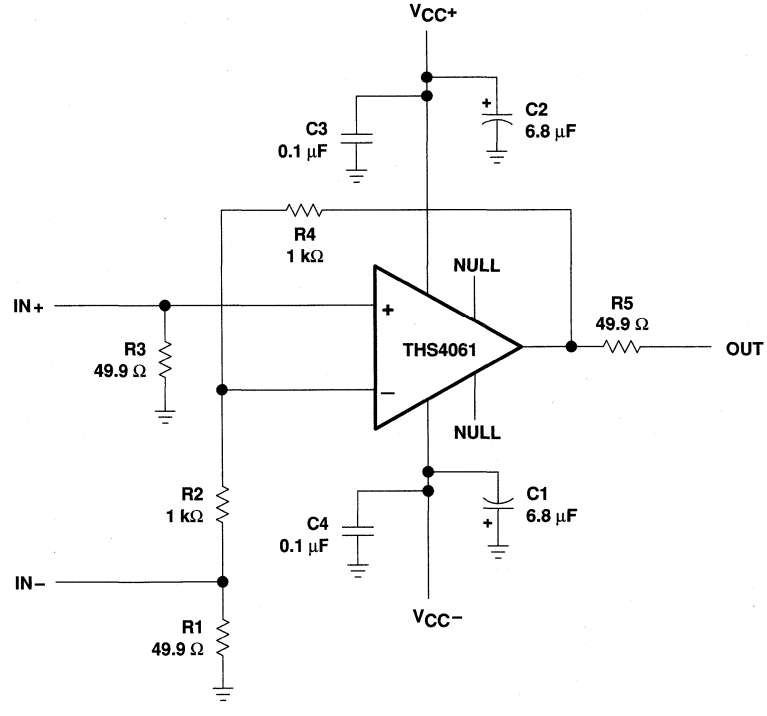
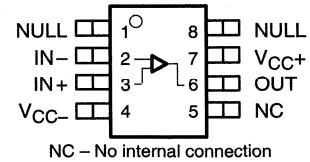


Figure 26. THS4061 Evaluation Board Schematic

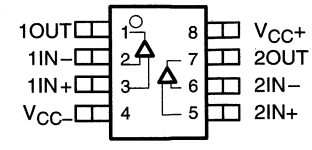
- **Ultra-Low 3.4 mA Per Channel Quiescent Current**
- **High Speed**
  - **175 MHz Bandwidth (–3 dB, G = 1)**
  - **230 V/μs Slew Rate**
  - **43 ns Settling Time (0.1%)**
- **High Output Drive, I_O = 85 mA (typ)**
- **Excellent Video Performance**
  - **35 MHz Bandwidth (0.1 dB, G = 1)**
  - **0.01% Differential Gain**
  - **0.05° Differential Phase**
- **Very Low Distortion**
  - **THD = –64 dBc (f = 1 MHz, R_L = 150 Ω)**
  - **THD = –79 dBc (f = 1 MHz, R_L = 1 kΩ)**
- **Wide Range of Power Supplies**
  - **V_{CC} = ±5 V to ±15 V**
- **Available in Standard SOIC or MSOP PowerPAD™ Package**
- **Evaluation Module Available**

THS4081
D OR DGN† PACKAGE
(TOP VIEW)



NC – No internal connection

THS4082
D OR DGN† PACKAGE
(TOP VIEW)



Cross Section View Showing
PowerPAD™ Option (DGN)

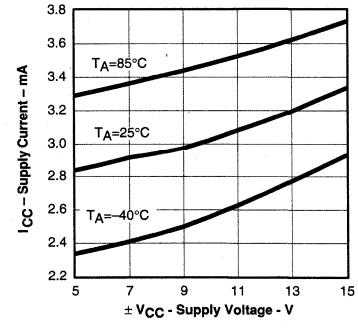
† This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

description

The THS4081 and THS4082 are ultra-low power, high-speed voltage feedback amplifiers that are ideal for communication and video applications. These amplifiers operate off of a very low 3.4-mA quiescent current per channel and have a high output drive capability of 85 mA. The signal-amplifier THS4081 and the dual-amplifier THS4082 offer very good ac performance with 175-MHz bandwidth, 230-V/μs slew rate, and 43-ns settling time (0.1%). With total harmonic distortion (THD) of –64 dBc at f = 1 MHz, the THS4081 and THS4082 are ideally suited for applications requiring low distortion.

RELATED DEVICES	
DEVICE	**DESCRIPTION**
THS4011/2	290-MHz Low Distortion High-Speed Amplifiers
THS4031/2	100-MHz Low Noise High Speed-Amplifiers
THS4051/2	70-MHz High-Speed Amplifiers

SUPPLY CURRENT
vs
SUPPLY VOLTAGE



CAUTION: The THS4081 and THS4082 provide ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

PowerPAD is a trademark of Texas Instruments.

AVAILABLE OPTIONS

T_A	NUMBER OF CHANNELS	PACKAGED DEVICES		MSOP SYMBOL	EVALUATION MODULE
		PLASTIC SMALL OUTLINE† (D)	PLASTIC MSOP† (DGN)		
0°C to 70°C	1	THS4081CD	THS4081CDGN‡	AEO	THS4081EVM
	2	THS4082CD	THS4082CDGN‡	AER	THS4082EVM
–40°C to 85°C	1	THS4081ID	THS4081IDGN‡	AEQ	—
	2	THS4082ID	THS4082IDGN‡	AEP	—

† The D and DGN packages are available taped and reeled. Add an R suffix to the device type (i.e., THS4081CDGN).
‡ This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

functional block diagram

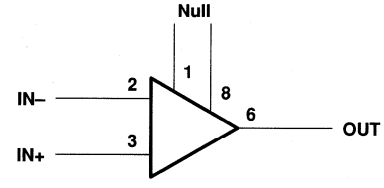


Figure 1. THS4081 – Single Channel

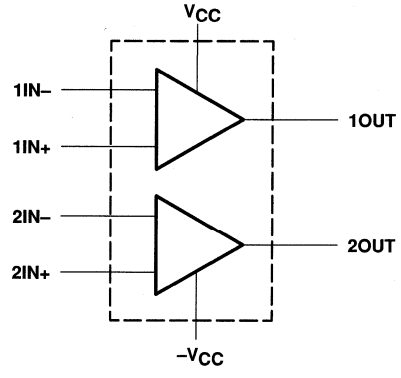


Figure 2. THS4082 – Dual Channel

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} ..... ±16.5 V
Input voltage, V_I ..... $\pm V_{CC}$
Output current, I_O ..... 150 mA
Differential input voltage, V_{IO} ..... ±4 V
Continuous total power dissipation ..... See Dissipation Rating Table
Maximum junction temperature, T_J ..... 150°C
Operating free-air temperature, T_A: C-suffix ..... 0°C to 70°C
I-suffix ..... −40°C to 85°C
Storage temperature, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING
D	167‡	38.3	740 mW
DGN§	58.4	4.7	2.14 W

‡ This data was taken using the JEDEC standard Low-K test PCB. For the JEDEC Proposed High-K test PCB, the θ_{JA} is 95°C/W with a power rating at T_A = 25°C of 1.32 W.
§ This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3 in. × 3 in. PC. For further information, refer to *Application Information* section of this data sheet.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} and V_{CC-}	Dual supply	±4.5		±16	V
	Single supply	9		32	
Operating free-air temperature, T_A	C-suffix	0		70	°C
	I-suffix	−40		85	

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
BW	Small-signal bandwidth (–3 dB)	V_{CC} = ±15 V		Gain = 1		175		MHz
		V_{CC} = ±5 V				160		
		V_{CC} = ±15 V		Gain = –1		70		MHz
		V_{CC} = ±5 V				65		
	Bandwidth for 0.1 dB flatness	V_{CC} = ±15 V		Gain = 1		35		MHz
		V_{CC} = ±5 V				35		
	Full power bandwidth†	$V_{O(pp)}$ = 20 V,	V_{CC} = ±15 V			2.7		MHz
		$V_{O(pp)}$ = 5 V,	V_{CC} = ±5 V			7.1		
SR	Slew rate‡	V_{CC} = ±15 V,	20-V step,	Gain = 5		230		V/µs
		V_{CC} = ±5 V,	5-V step	Gain = 1		170		
t_s	Settling time to 0.1%	V_{CC} = ±15 V,	5-V step	Gain = –1		43		ns
		V_{CC} = ±5 V,	2-V step			30		
	Settling time to 0.01%	V_{CC} = ±15 V,	5-V step	Gain = –1		233		ns
		V_{CC} = ±5 V,	2-V step			280		

† Slew rate is measured from an output level range of 25% to 75%.
‡ Full power bandwidth = slew rate/2π $V_{O(Peak)}$.

noise/distortion performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	$V_{O(pp)}$ = 2 V, f = 1 MHz, Gain = 2	V_{CC} = ±15 V	R_L = 150 Ω		–64		dBc
				R_L = 1 kΩ		–79		
			V_{CC} = ±5 V	R_L = 150 Ω		–64		
				R_L = 1 kΩ		–77		
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz			10		nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz			0.7		pA/√Hz
	Differential gain error	Gain = 2, 40 IRE modulation,	NTSC, ±100 IRE ramp	V_{CC} = ±15 V		0.01%		
				V_{CC} = ±5 V		0.01%		
	Differential phase error	Gain = 2, 40 IRE modulation,	NTSC, ±100 IRE ramp	V_{CC} = ±15 V		0.05°		
				V_{CC} = ±5 V		0.05°		
X_T	Channel-to-channel crosstalk (THS4082 only)	V_{CC} = ±5 V or ±15 V,	f = 1 MHz			–75		dB

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

dc performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Open loop gain		V_{CC} = ±15 V, V_O = ±10 V, R_L = 1 kΩ	T_A = 25°C	10	19		V/mV
			T_A = full range†	9			
		V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 250 Ω	T_A = 25°C	8	16		V/mV
			T_A = full range†	7			
V_{OS}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		1	7	mV
			T_A = full range†			8	
	Offset voltage drift		T_A = full range†		15		µV/°C
I_{IB}	Input bias current		T_A = 25°C		1.2	6	µA
			T_A = full range†			8	
I_{OS}	Input offset current		T_A = 25°C		20	250	nA
			T_A = full range†			400	
	Offset current drift	T_A = full range†			0.3		nA/°C

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

input characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V		±13.8	±14.1		V
		V_{CC} = ±5 V		±3.8	±3.9		
CMRR	Common mode rejection ratio	V_{CC} = ±15 V, V_{ICR} = ±12 V,	T_A = full range†	84	93		dB
		V_{CC} = ±5 V, V_{ICR} = ±2 V,	T_A = full range†	78	90		dB
R_I	Input resistance				1		MΩ
C_I	Input capacitance				1.5		pF

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

output characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 250 Ω	±12	±13.6		V
		V_{CC} = ±5 V	R_L = 150 Ω	±3.4	±3.8		
		V_{CC} = ±15 V	R_L = 1 kΩ	±13.5	±13.8		V
		V_{CC} = ±5 V		±3.5	±3.9		
I_O	Output current§	V_{CC} = ±15 V	R_L = 20 Ω	65	85		mA
		V_{CC} = ±5 V		50	70		
I_{SC}	Short-circuit current‡	V_{CC} = ±15 V			100		mA
R_O	Output resistance	Open loop			13		Ω

‡ Observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the absolute maximum ratings section of this data sheet for more information.

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (per amplifier)	V_{CC} = ±15 V	T_A = 25°C		3.4	4.2	mA
			T_A = full range†			5	
		V_{CC} = ±5 V	T_A = 25°C		2.9	3.7	
			T_A = full range†			4.5	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = full range†	79	90		dB

† Full range = 0°C to 70°C for C suffix and –40°C to 85°C for I suffix

TYPICAL CHARACTERISTICS

OPEN LOOP GAIN & PHASE RESPONCE vs FREQUENCY

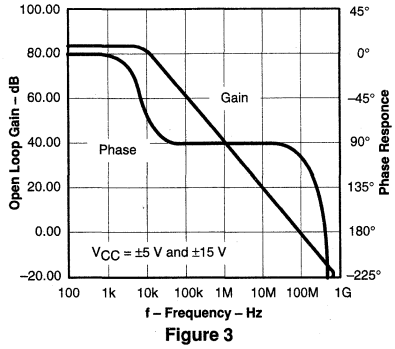


Figure 3

CROSSTALK vs FREQUENCY

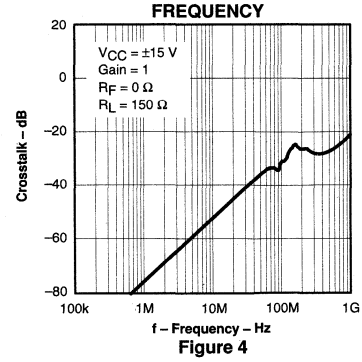


Figure 4

TOTAL HARMONIC DISTORTION vs FREQUENCY

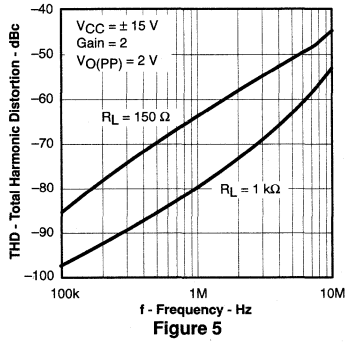


Figure 5

TOTAL HARMONIC DISTORTION vs FREQUENCY

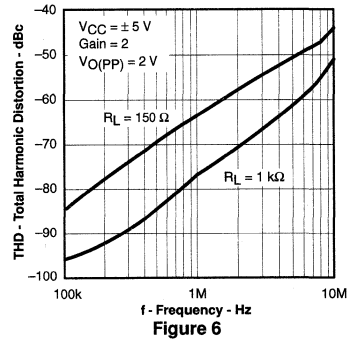


Figure 6

SETTLING vs OUTPUT STEP

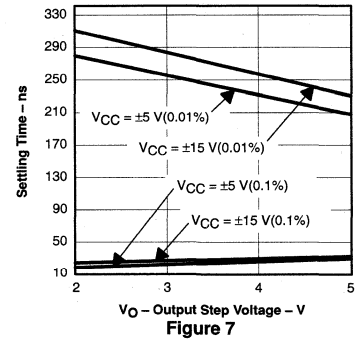


Figure 7

POWER SUPPLY REJECTION RATIO vs FREQUENCY

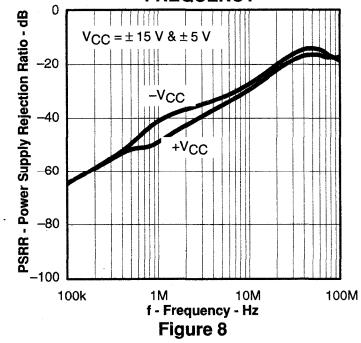


Figure 8

DISTORTION vs OUTPUT VOLTAGE

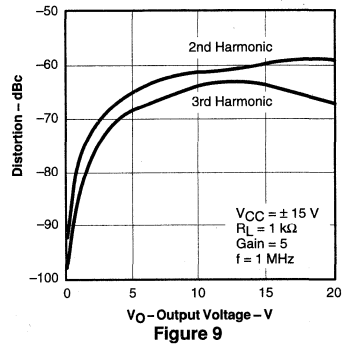


Figure 9

DISTORTION vs OUTPUT VOLTAGE

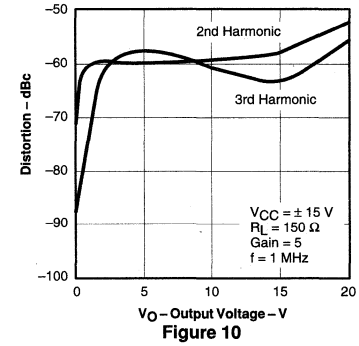


Figure 10

TYPICAL CHARACTERISTICS

DISTORTION vs FREQUENCY

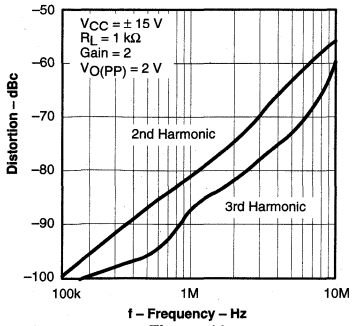


Figure 11

DISTORTION vs FREQUENCY

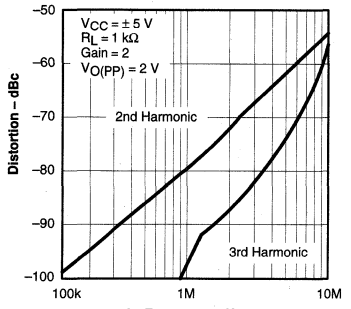


Figure 12

DISTORTION vs FREQUENCY

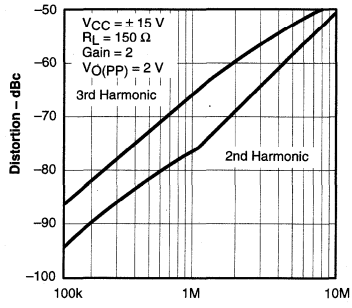


Figure 13

DISTORTION vs FREQUENCY

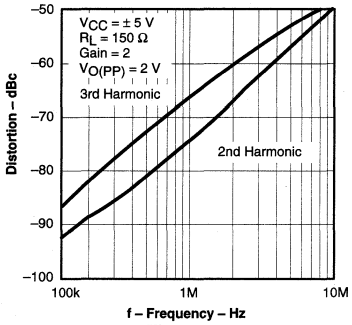


Figure 14

OUTPUT AMPLITUDE vs FREQUENCY

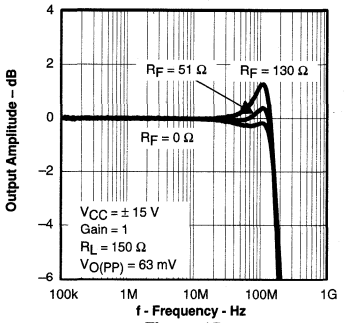


Figure 15

OUTPUT AMPLITUDE vs FREQUENCY

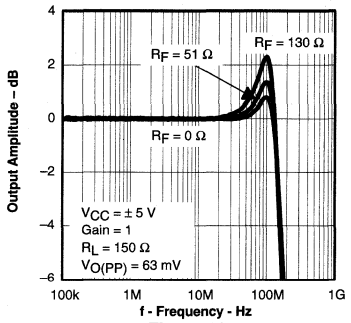


Figure 16

OUTPUT AMPLITUDE vs FREQUENCY

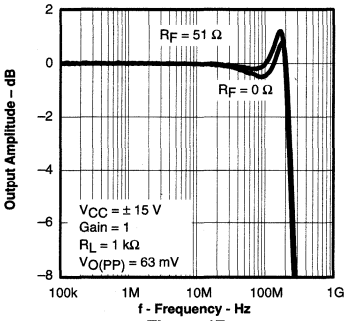


Figure 17

OUTPUT AMPLITUDE vs FREQUENCY

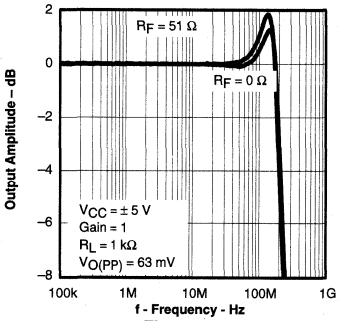


Figure 18

OUTPUT AMPLITUDE vs FREQUENCY

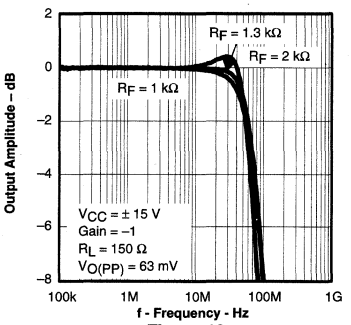


Figure 19

TYPICAL CHARACTERISTICS

OUTPUT AMPLITUDE vs FREQUENCY

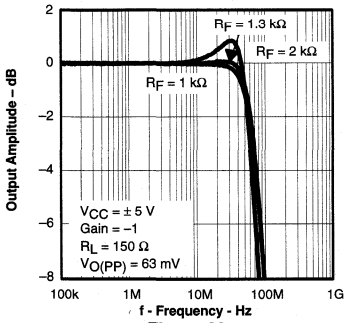


Figure 20

OUTPUT AMPLITUDE vs FREQUENCY

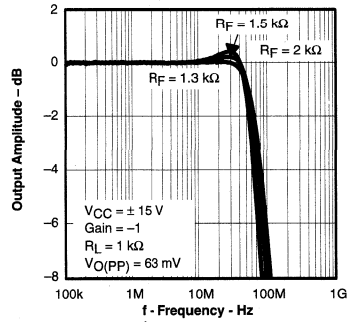


Figure 21

OUTPUT AMPLITUDE vs FREQUENCY

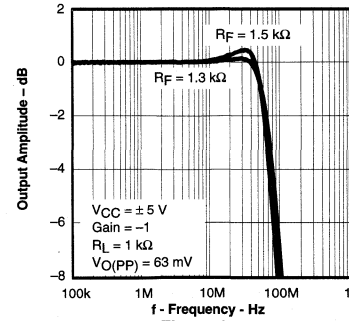


Figure 22

OUTPUT AMPLITUDE vs FREQUENCY

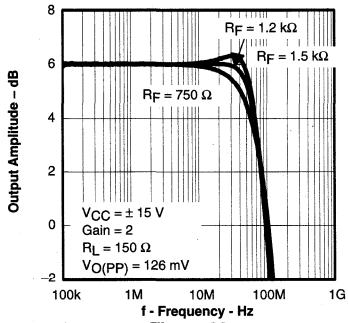


Figure 23

OUTPUT AMPLITUDE vs FREQUENCY

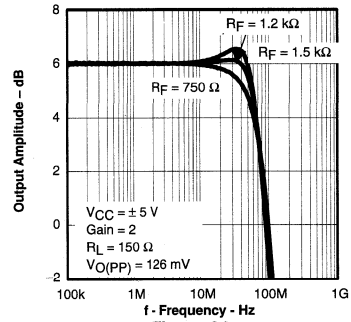


Figure 24

OUTPUT AMPLITUDE vs FREQUENCY

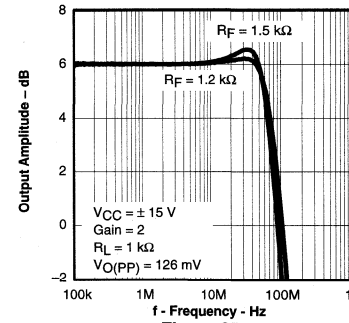


Figure 25

OUTPUT AMPLITUDE vs FREQUENCY

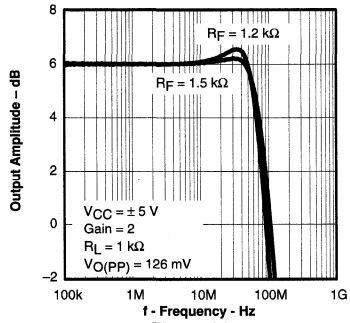


Figure 26

2-V STEP RESPONSE

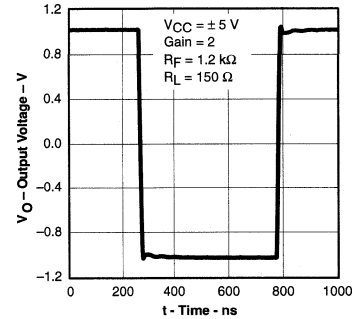


Figure 27

5-V STEP RESPONSE

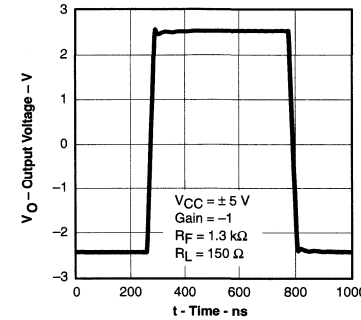


Figure 28

TYPICAL CHARACTERISTICS

2-V STEP RESPONSE

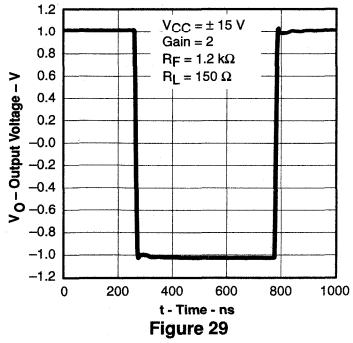


Figure 29

20-V STEP RESPONSE

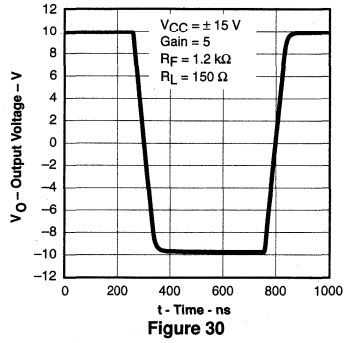


Figure 30

INPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

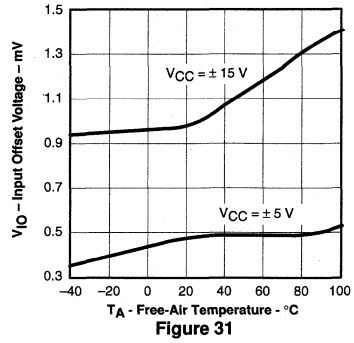


Figure 31

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

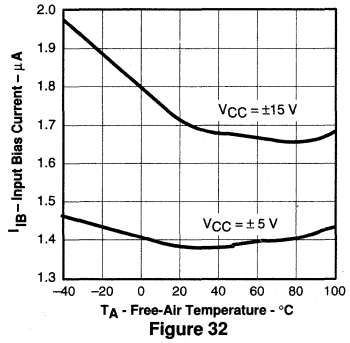


Figure 32

OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

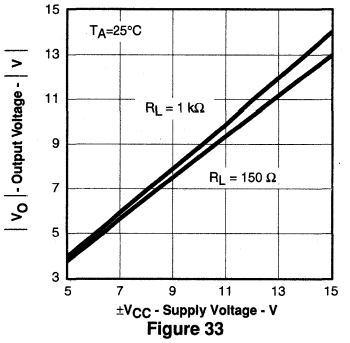


Figure 33

COMMON-MODE INPUT VOLTAGE
vs
SUPPLY VOLTAGE

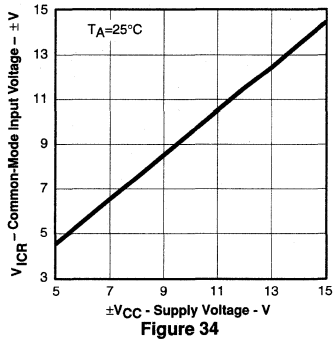


Figure 34

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

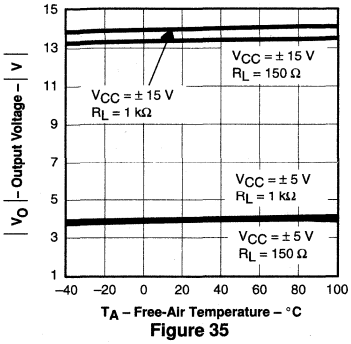


Figure 35

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

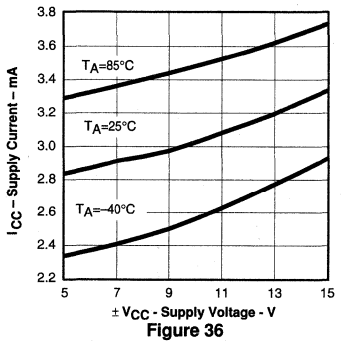


Figure 36

VOLTAGE & CURRENT NOISE
vs
FREQUENCY

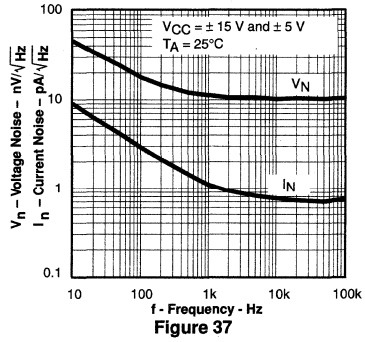


Figure 37

APPLICATION INFORMATION

theory of operation

The THS408x is a high-speed, operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This results in an exceptionally high performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 38.

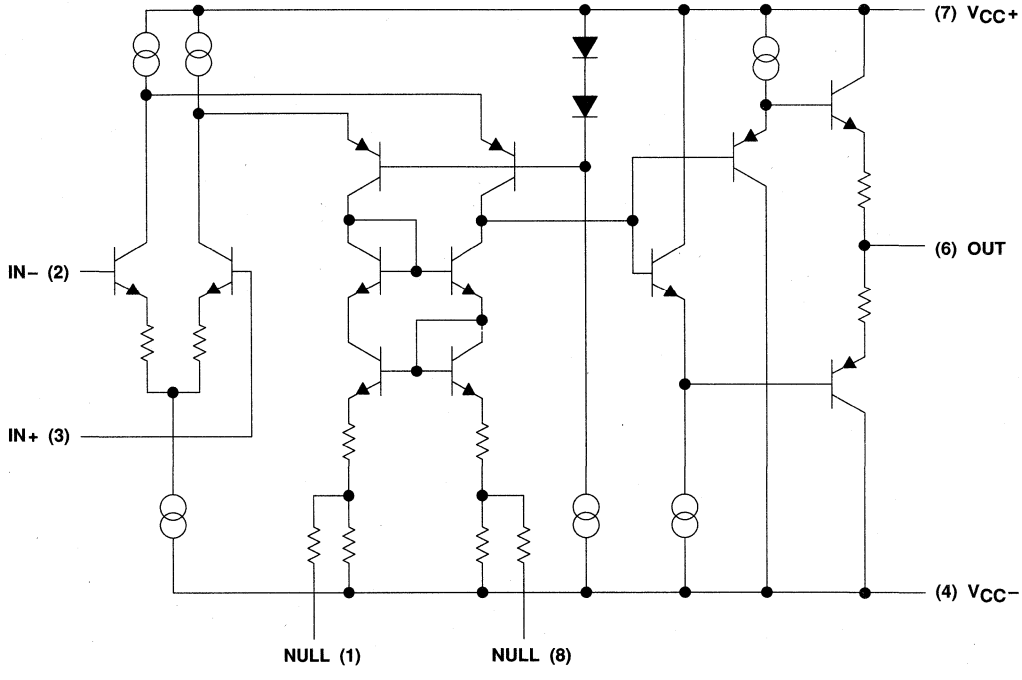


Figure 38. THS4081 Simplified Schematic

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true when amplifying small signals, where signal-to-noise ratio (SNR) is very important. The noise model for the THS408x is shown in Figure 39. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{\text{Hz}}$)
- IN+ = Noninverting current noise (pA/$\sqrt{\text{Hz}}$)
- IN– = Inverting current noise (pA/$\sqrt{\text{Hz}}$)
- e_{Rx} = Thermal voltage noise associated with each resistor ($e_{Rx} = 4\ kTR_x$)

APPLICATION INFORMATION

noise calculations and noise figure (continued)

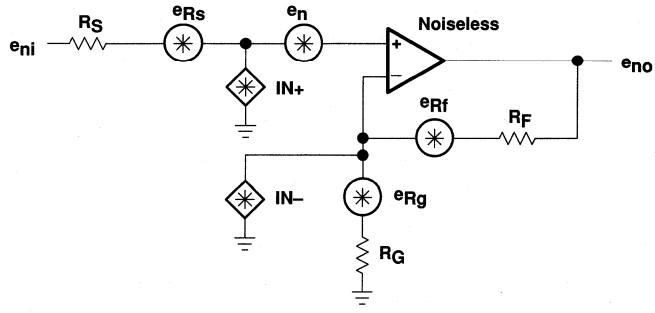


Figure 39. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN + \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\ kTR_s + 4\ kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\ A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (noninverting case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

For more information on noise analysis, please refer to the *Noise Analysis* section in *Operational Amplifier Circuits Applications Report* (literature number SLVA043).

APPLICATION INFORMATION

noise calculations and noise figure (continued)

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^2}{(e_{Rs})^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[(e_n)^2 + (IN + \times R_S)^2\right]}{4\ kTR_S}\right]$$

Figure 40 shows the noise figure graph for the THS408x.

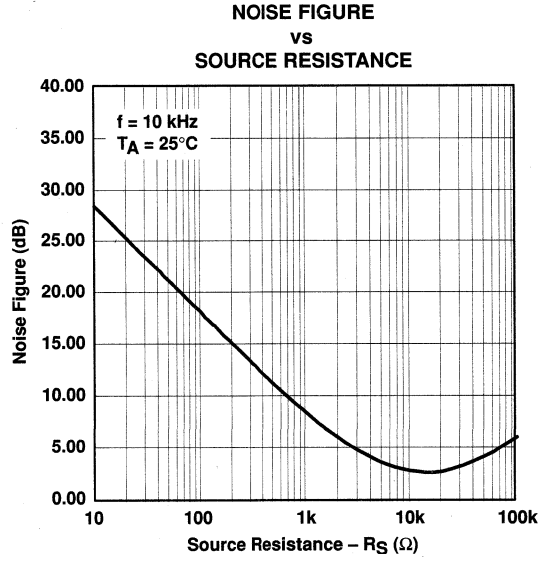


Figure 40. Noise Figure vs Source Resistance

APPLICATION INFORMATION

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS408x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 41. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

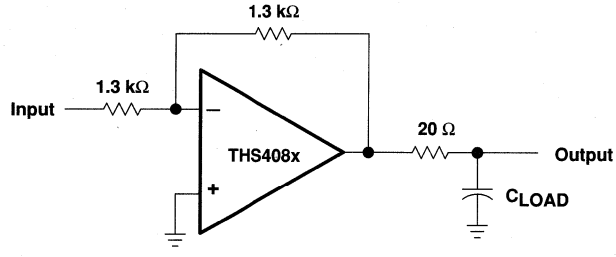


Figure 41. Driving a Capacitive Load

offset nulling

The THS408x has very low input offset voltage for a high-speed amplifier. However, if additional correction is required, an offset nulling function has been provided on the THS4081. The input offset can be adjusted by placing a potentiometer between terminals 1 and 8 of the device and tying the wiper to the negative supply. This is shown in Figure 42.

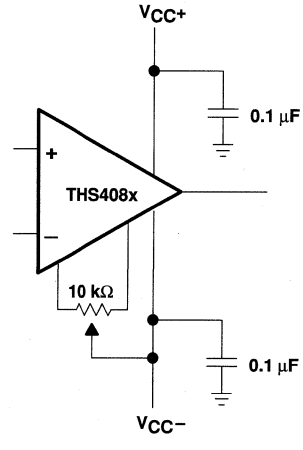
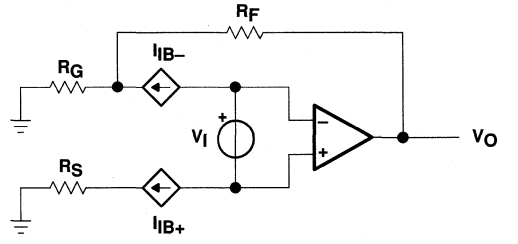


Figure 42. Offset Nulling Schematic

APPLICATION INFORMATION

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

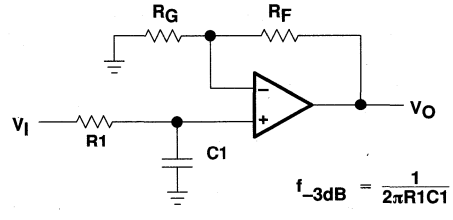


$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

Figure 43. Output Offset Voltage Model

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 44).



$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 44. Single-Pole Low-Pass Filter

APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high frequency performance of the THS408x, follow proper printed-circuit board high frequency design techniques. A general set of guidelines is given below. In addition, a THS408x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

general PowerPAD design considerations

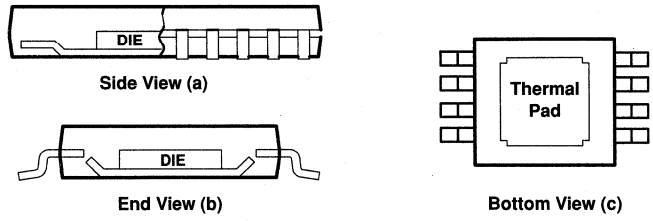
The THS408x is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 45(a) and Figure 45(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 45(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the, heretofore, awkward mechanical methods of heatsinking.

APPLICATION INFORMATION

general PowerPAD design considerations (continued)



NOTE A. The thermal pad is electrically isolated from all terminals in the package.

Figure 45. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach.

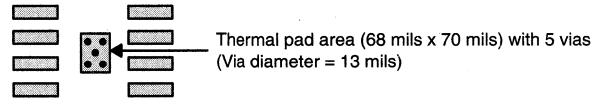


Figure 46. PowerPAD PCB Etch and Via Pattern

1. Prepare the PCB with a top side etch pattern as shown in Figure 46. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS408xDGN IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered, so wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS408xDGN package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the THS408xDGN IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

APPLICATION INFORMATION

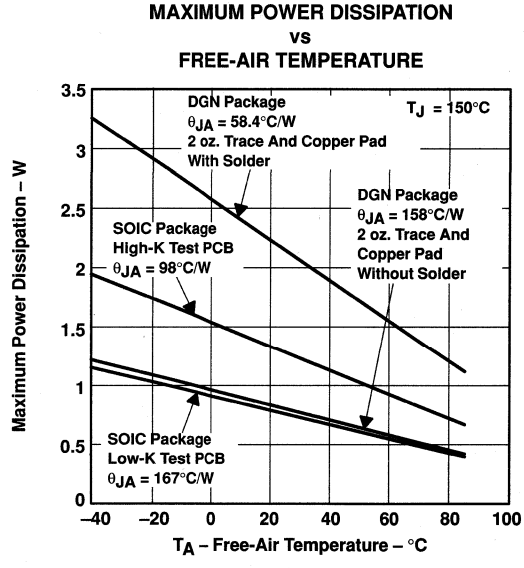
general PowerPAD design considerations (continued)

The actual thermal performance achieved with the THS408xDGN in its PowerPAD package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA}, is about 58.4°C/W. For comparison, the non-PowerPAD version of the THS408x IC (SOIC) is shown. For a given θ_{JA}, the maximum power dissipation is shown in Figure 47 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS408x IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A. Results are with no air flow and PCB size = 3"× 3"

Figure 47. Maximum Power Dissipation vs Free-Air Temperature

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

APPLICATION INFORMATION

general PowerPAD™ design considerations (continued)

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multiamplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 48 to Figure 51 show this effect, along with the quiescent heat, with an ambient air temperature of 50°C. Obviously, as the ambient temperature increases, the limit lines shown will drop accordingly. The area under each respective limit line is considered the safe operating area. Any condition above this line will exceed the amplifier's limits and failure may result. When using V_{CC} = ±5 V, there is generally not a heat problem, even with SOIC packages. But, when using V_{CC} = ±15 V, the SOIC package is severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD™ devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual amplifier package (THS4082), the sum of the RMS output currents and voltages should be used to choose the proper package. The graphs shown assume that both amplifier's outputs are identical.

THS4081
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

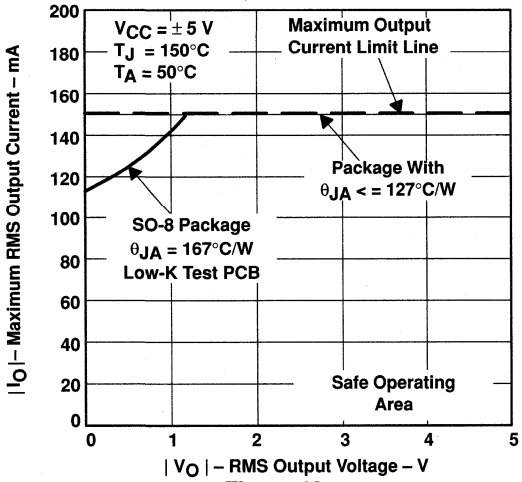


Figure 48

THS4081
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

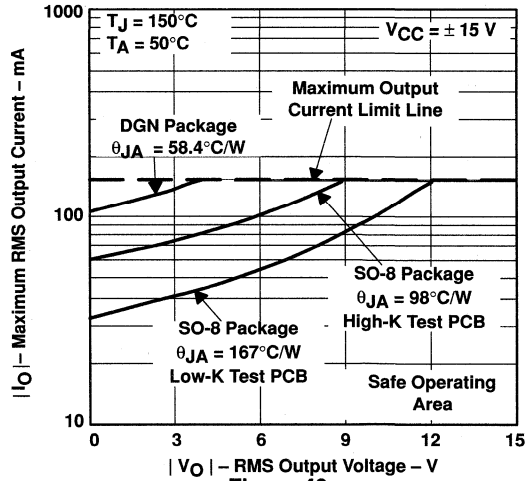


Figure 49

APPLICATION INFORMATION

general PowerPAD™ design considerations (continued)

THS4082
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

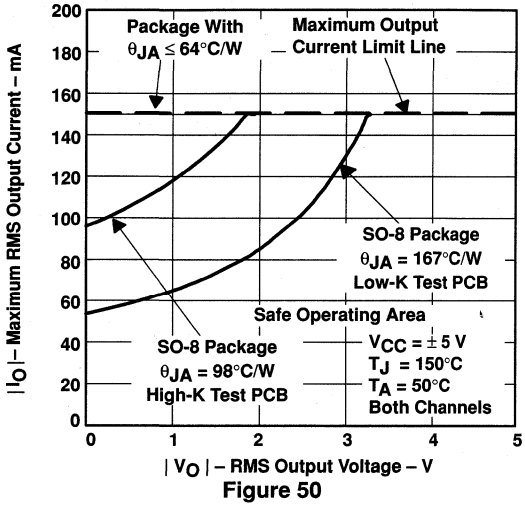


Figure 50

THS4082
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

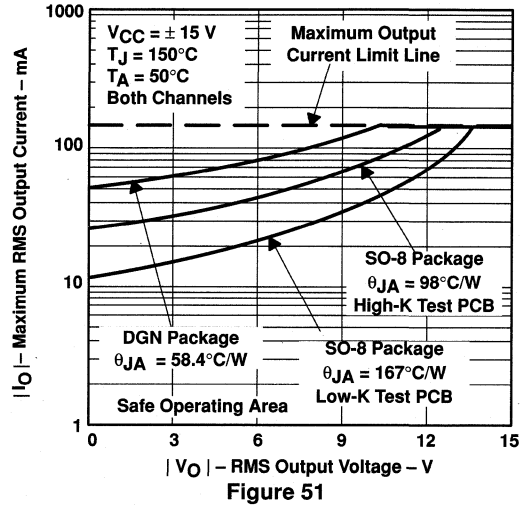


Figure 51

APPLICATION INFORMATION

evaluation board

An evaluation board is available for the THS4081 (literature number SLOP242) and THS4082 (literature number SLOP239). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 52. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. For more information, please refer to the *THS4081 EVM User's Guide* or the *THS4082 EVM User's Guide*. To order the evaluation board, contact your local TI sales office or distributor.

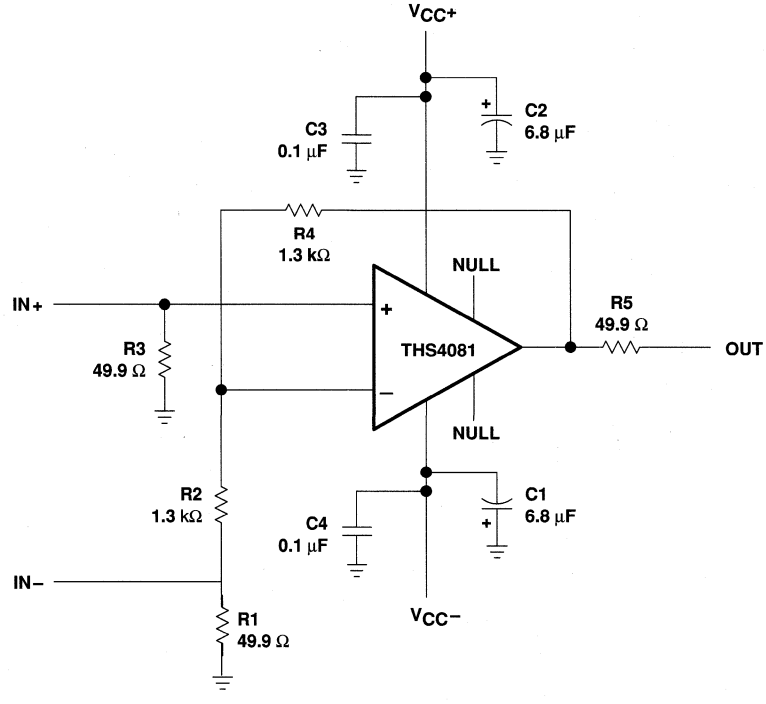
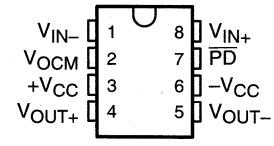


Figure 52. THS4081 Evaluation Board

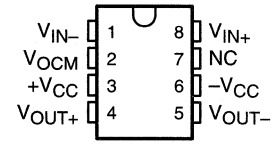
SLOS318 – MAY 2000

- **Differential-Input/Differential-Output**
  - **Simple Single-Ended to Differential Conversion**
  - **Balanced Ouputs Reject Common-Mode Noise**
- **High Performance**
  - **134 MHz –3 dB Bandwidth**
  - **51 V/μs Slew Rate**
  - **–100 dB HD3 at 10 MHz**
  - **1.3 nV/√Hz Input-Referred Noise**
- **Low-Power Shutdown Option**
  - **I_{CC} = 860 μA in Shutdown Mode**
- **Wide Power Supply Range**
  - **V_{CC} = 5 V Single Supply to ±15 V**

THS4130
D OR DGN PACKAGE
(TOP VIEW)



THS4131
D OR DGN PACKAGE
(TOP VIEW)



description

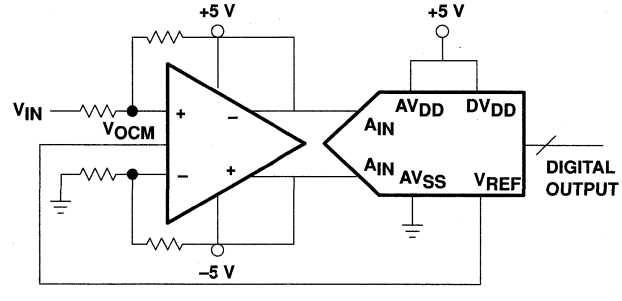
The THS413x is one in a family of differential-input/differential-output devices fabricated using Texas Instruments' state-of-the-art BiCom I complementary bipolar process.

The THS413x consists of a true differential signal path from input to output. This results in excellent common-mode noise rejection and improved total harmonic distortion. Not only does the device provide balanced, differential outputs, but internal feedback reduces the effects of parametric differences in gain-setting components between sides.

Designed for high-performance 16-bit applications, the THS413x has 134 MHz bandwidth, 51 V/μs slew rate, and –100 dB third harmonic distortion at 250 MHz. Combined with its differential outputs, these specifications make the THS413x ideal for driving high-performance analog-to-digital converters.

The THS413x also offers many advantages for improving system designs. Its differential outputs make single-ended to differential conversion simple and efficient. The V_{OCM} input provides easy level-shifting and, when driven by an ADC reference voltage, ensures that the ADC differential inputs are centered in its dynamic range.

typical ADC application circuits



PowerPAD is a trademark of Texas Instruments.

description (continued)

Its inherent common-mode noise rejection makes the THS413x ideal for distributing critical signals across a printed-circuit board.

The THS413x is also well suited for audio mixing and hi-fi applications with a THD+N of –105 dB in the audio frequency band.

The THS413x is offered in a standard 8-pin SOIC package (D) and an 8-pin MSOP PowerPAD™ package (DGN). The low-power shutdown capability is offered as an option in the THS4130. The device operates over the industrial temperature range of –40°C to 85°C.

HIGH-SPEED xDSL LINE DRIVER/RECEIVER FAMILY

DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES		SHUTDOWN
		SOIC	MSOP	
THS4130	1	8	8	X
THS4131	1	8	8	–

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	SMALL OUTLINE (D)	MSOP PowerPAD™ (DGN)
0°C to 70°C	THS4130CD THS4131CD	THS4130CDGN THS4131CDGN
–40°C to 85°C	THS4130ID THS4131ID	THS4130IDGN THS4131IDGN

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC-} to V_{CC+} ..... ±16.5 V
Input voltage, V_I ..... $\pm V_{CC}$
Output current, I_O ..... 100 mA
Differential input voltage, V_{ID} ..... ±6 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature, T_A: C suffix ..... 0°C to 70°C
I suffix ..... –40°C to 85°C
Storage temperature, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 Inch) from case for 10 seconds ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	740 mW	6 mW/°C	470 mW	380 mW
DGN	1.71 mW	17.1 mW/°C	941 mW	685 mW

PRODUCT PREVIEW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}+ and V_{CC}–		±2.5		±15	V
Operating free-air temperature, T_A	C suffix	0		70	°C
	I suffix	–40		85	

electrical characteristics, V_{CC} = 5 V, R_L = 800 Ω, T_A = 25°C (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BW	Small signal bandwidth (–3 dB)	Gain = –1		134		MHz
SR	Slew rate	Gain = –1		51		V/µs
t_s	Settling time to 0.1%	Step voltage = 2 V, Gain = –1		78		ns
	Settling time to 0.01%			213		ns

distortion performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	f = 1 MHz		–100		dBc
	Differential gain error	Gain = 2 NTSC, 40 IRE modulation				
	Differential phase error					
	Spurious free dynamic range					dB
	Third Intermodulation distortion	V_{IN} = 4 V_{PP}, G = 1, F1 = 5 MHz, F2 = 5.5 MHz		–62		dB
	Third order intercept	V_{IN} = 4 V_{PP}, G = 1, F1 = 250 MHz, F2 = 30 MHz		30.8		dB

noise performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_n	Input voltage noise	f = 10 kHz		1.3		nV/√Hz
I_n	Input current noise	f = 10 kHz		0.1		pA/√Hz

dc performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	T_A = 25°C		0.215		mV
	Offset drift	T_A = full range				µV/°C
I_{IB}	Input bias current			2		µA
I_{OS}	Input offset current					nA
	Offset drift					nA/°C

input characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMRR	Common-mode refection ratio	V_{ICR} = 0 V to 5 V, T_A = full range				dB
V_{ICR}	Common-mode input voltage range			–4 to 4.5		V
R_I	Input resistance					MΩ
C_I	Input capacitance					pF
R_O	Output resistance	Open loop				Ω

PRODUCT PREVIEW

electrical characteristics, V_{CC} = 5 V, R_L = 800 Ω, T_A = 25°C (unless otherwise noted) (continued)

output characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{IC} = 2.5 V, I_{OH} = 2.5 mA	T_A = 25°C				V
			T_A = full range				
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V, I_{OH} = 2.5 mA	T_A = 25°C				V
			T_A = full range				
I_O	Output current	R_L = 20 Ω					mA

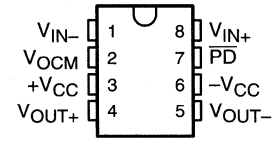
power supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	Single supply		+ 5		V
		Split supply		±15		
I_{CC}	Quiescent current (per amplifier)	T_A = full range				mA
PSRR	Power supply rejection ratio	T_A = 25°C		81		dB
		T_A = full range				

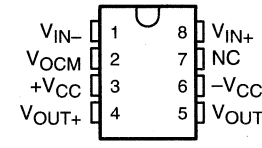
PRODUCT PREVIEW

- **Differential-Input/Differential-Output**
  - **Simple Single-Ended to Differential Conversion**
  - **Balanced Ouputs Reject Common-Mode Noise**
- **High Performance**
  - **148 MHz –3 dB Bandwidth**
  - **450 V/μs Slew Rate**
  - **–79 dB HD3 at 10 MHz**
  - **6.5 nV/√Hz Input-Referred Noise**
- **Low-Power Supply Range**
  - **I_{CC} = 880 μA in Shutdown Mode**
- **Wide Power Supply Range**
  - **V_{CC} = 5 V Single Supply to ±15 V**

THS4140
D OR DGN PACKAGE
(TOP VIEW)



THS4141
D OR DGN PACKAGE
(TOP VIEW)



description

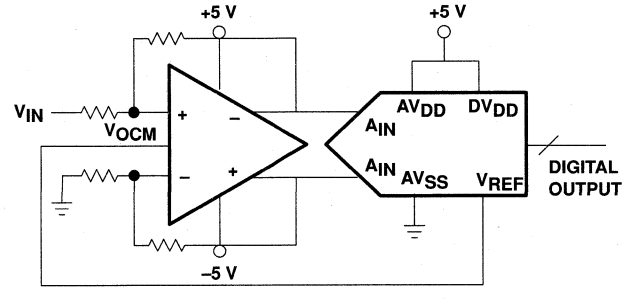
The THS414x is one in a family of differential-input/differential-output devices fabricated using Texas Instruments' state-of-the-art BiCom I complementary bipolar process.

The THS414x consists of a true differential signal path from input to output. This results in excellent common-mode noise rejection and improved total harmonic distortion. Not only does the device provide balanced, differential outputs, but internal feedback reduces the effects of parametric differences in gain-setting components between sides.

Designed for high-performance 12-bit applications, the THS414x has 148 MHz bandwidth, 450 V/μs slew rate, and ±79 dB third harmonic distortion at 1 MHz. Combined with its differential outputs, these specifications make the THS414x ideal for driving high-performance analog-to-digital converters.

The THS414x also offers many advantages for improving system designs. Its differential outputs make single-ended to differential conversion simple and efficient. The V_{OCM} input provides easy level-shifting and, when driven by an ADC reference voltage, ensures that the ADC differential inputs are centered in its dynamic range.

typical ADC application circuits



PRODUCT PREVIEW

PowerPAD is a trademark of Texas Instruments.

description (continued)

Its inherent common-mode noise rejection makes the THS414x ideal for distributing critical signals across a printed-circuit board.

The THS414x is offered in a standard 8-pin SOIC package (D) and an 8-pin MSOP PowerPAD™ package (DGN). The low-power shutdown capability is offered as an option in the THS4140. The device operates over the industrial temperature range of –40°C to 85°C.

HIGH-SPEED xDSL LINE DRIVER/RECEIVER FAMILY

DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES		SHUTDOWN
		SOIC	MSOP	
THS4140	1	8	8	X
THS4141	1	8	8	–

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	SMALL OUTLINE (D)	MSOP PowerPAD™ (DGN)
0°C to 70°C	THS4140CD THS4141CD	THS4140CDGN THS4141CDGN
–40°C to 85°C	THS4140ID THS4141ID	THS4140IDGN THS4141IDGN

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}– to V_{CC}+ ..... ±16.5 V
Input voltage, V_I ..... $\pm V_{CC}$
Output current, I_O ..... 100 mA
Differential input voltage, V_{ID} ..... ±6 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature, T_A: C suffix ..... 0°C to 70°C
I suffix ..... –40°C to 85°C
Storage temperature, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 Inch) from case for 10 seconds ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	740 mW	6 mW/°C	470 mW	380 mW
DGN	1.71 mW	17.1 mW/°C	941 mW	685 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}+ and V_{CC}–		±2.5		±15	V
Operating free-air temperature, T_A	C suffix	0		70	°C
	I suffix	–40		85	

PRODUCT PREVIEW

electrical characteristics, V_{CC} = 5 V, R_L = 800 Ω, T_A = 25°C (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BW	Small signal bandwidth (–3 dB)	Gain = –1		148		MHz
SR	Slew rate	Gain = –1		450		V/μs
t_s	Settling time to 0.1%	Step voltage = 2 V, Gain = –1		15.5		ns
	Settling time to 0.01%			308		ns

distortion performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HD2	Second harmonic distortion	1 MHz and 8 MHz		–83 –65		dB
HD3	Third harmonic distortion	1 MHz and 8 MHz		–74 –55.5		dB
	Differential gain error	Gain = 2 NTSC, 40 IRE modulation				
	Differential phase error					
	Spurious free dynamic range					dB
	Intermodulation distortion					dB
	Third-order intercept					dB

noise performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_n	Input voltage noise	f = 10 kHz		6.5		nV/√Hz
I_n	Input current noise	f = 10 kHz		1.25		pA/√Hz

dc performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{os}	Input offset voltage	T_A = 25°C		822		mV
	Offset drift	T_A = full range				μV/°C
I_{IB}	Input bias current			5.1		μA
I_{OS}	Input offset current					nA
	Offset drift					nA/°C

input characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMRR	Common-mode refection ratio	V_{ICR} = 0 V to 5 V, T_A = full range				dB
V_{ICR}	Common-mode input voltage range			±4 to 4.7		V
R_I	Input resistance					MΩ
C_I	Input capacitance					pF
R_O	Output resistance	Open loop				Ω

output characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output voltage swing	T_A = 25°C		–4 to 4		V
I_O	Output current			60		mA

PRODUCT PREVIEW

electrical characteristics, V_{CC} = 5 V, R_L = 800 Ω, T_A = 25°C (unless otherwise noted) (continued)

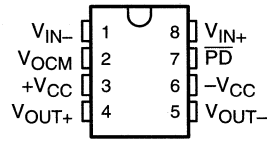
power supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	Single supply		5		V
		Split supply		±15		
I_{CC}	Quiescent current (per amplifier)	T_A = full range		13.4		mA
PSRR	Power supply rejection ratio	T_A = 25°C		100		dB
		T_A = full range				

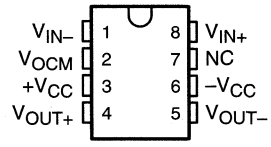
PRODUCT PREVIEW

- **Differential-Input/Differential-Output**
  - **Simple Single-Ended to Differential Conversion**
  - **Balanced Ouputs Reject Common-Mode Noise**
- **High Performance**
  - **144 MHz –3 dB Bandwidth**
  - **830 V/μs Slew Rate**
  - **–82 dB HD3 at 10 MHz**
  - **9 nV/√Hz Input-Referred Noise**
- **Low-Power Supply Range**
  - **I_{CC} = 880 μA in Shutdown Mode**
- **Wide Power Supply Range**
  - **V_{CC} = 5 V single supply to ±15 V**

THS4150
D OR DGN PACKAGE
(TOP VIEW)



THS4151
D OR DGN PACKAGE
(TOP VIEW)



description

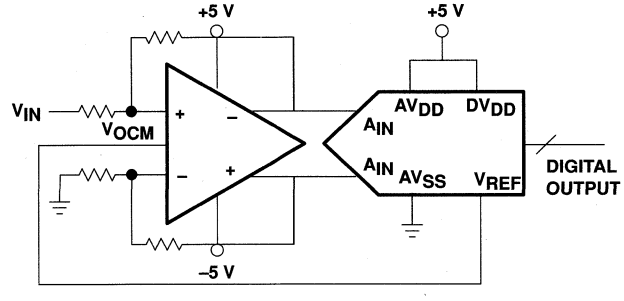
The THS415x is one in a family of differential-input/differential-output devices fabricated using Texas Instruments' state-of-the-art BiCom I complementary bipolar process.

The THS415x consists of a true differential signal path from input to output. This results in excellent common-mode noise rejection and improved total harmonic distortion. Not only does the device provide balanced, differential outputs, but internal feedback reduces the effects of parametric differences in gain-setting components between sides.

Designed for high-performance, 12-bit applications, the THS415x has 144 MHz bandwidth, 830 V/μs slew rate, and ±82 dB third harmonic distortion at 1 MHz. Combined with its differential outputs, these specifications make the THS415x ideal for driving high-performance analog-to-digital converters.

The THS415x also offers many advantages for improving system designs. Its differential outputs make single-ended to differential conversion simple and efficient. The V_{OCM} input provides easy level-shifting and, when driven by an ADC reference voltage, ensures that the ADC differential inputs are centered in its dynamic range.

typical ADC application circuits



PowerPAD is a trademark of Texas Instruments.

PRODUCT PREVIEW

description (continued)

Its inherent common-mode noise rejection makes the THS415x ideal for distributing critical signals across a printed-circuit board.

The THS415x is offered in a standard 8-pin SOIC package (D) and an 8-pin MSOP PowerPAD™ package (DGN). The low-power shutdown capability is offered as an option in the THS4150. The device operates over the industrial temperature range of –40°C to 85°C.

HIGH-SPEED xDSL LINE DRIVER/RECEIVER FAMILY

DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES		SHUTDOWN
		SOIC	MSOP	
THS4150	1	8	8	X
THS4151	1	8	8	–

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	SMALL OUTLINE (D)	MSOP PowerPAD™ (DGN)
0°C to 70°C	THS4150CD THS4151CD	THS4150CDGN THS4151CDGN
–40°C to 85°C	THS4150ID THS4151ID	THS4150IDGN THS4151IDGN

absolute maximum ratings over operating free–air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}– to V_{CC}+ ..... ±16.5 V
Input voltage, V_I ..... $\pm V_{CC}$
Output current, I_O ..... 150 mA
Differential input voltage, V_{ID} ..... ±4 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature, T_A: C suffix ..... 0°C to 70°C
I suffix ..... –40°C to 85°C
Storage temperature, T_{stg} ..... –65°C to 150°C
Lead temperature 1,6 mm (1/16 Inch) from case for 10 seconds ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	740 mW	6 mW/°C	470 mW	380 mW
DGN	1.71 mW	17.1 mW/°C	941 mW	685 mW

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC}+ and V_{CC}–		±2.5		±15	V
Operating free-air temperature, T_A	C suffix	0		70	°C
	I suffix	–40		85	

PRODUCT PREVIEW

electrical characteristics, V_{CC} = 5 V, R_L = 800 Ω, T_A = 25°C (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BW	Small signal bandwidth (–3 dB)	Gain = –1		144		MHz
SR	Slew rate	Gain = –1		830		V/μs
t_s	Settling time to 0.1%	Step voltage = 2 V, Gain = –1		15		ns
	Settling time to 0.01%			408		ns

distortion performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	f = 1 MHz				dBc
	Differential gain error	Gain = 2 NTSC, 40 IRE modulation				
	Differential phase error					
	Spurious free dynamic range					dB
	Intermodulation distortion					dB
	Third-order intercept					dB

noise performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_n	Input voltage noise	f = 10 kHz		7.5		nV/√Hz
I_n	Input current noise	f = 10 kHz		1.53		pA/√Hz

dc performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	T_A = 25°C				mV
	Offset drift	T_A = full range				μV/°C
I_{IB}	Input bias current			8.2		μA
I_{OS}	Input offset current					nA
	Offset drift					nA/°C

input characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMRR	Common-mode refection ratio	V_{ICR} = 0 V to 5 V, T_A = full range				dB
V_{ICR}	Common-mode input voltage range			–4 to 4.5		V
R_I	Input resistance					MO
C_I	Input capacitance					pF
R_O	Output resistance	Open loop				O

output characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Output voltage swing		T_A = 25°C		–3.8 to 3.8		V
I_O	Output current				60		mA

PRODUCT PREVIEW

electrical characteristics, V_{CC} = 5 V, R_L = 800 Ω, T_A = 25°C (unless otherwise noted) (continued)

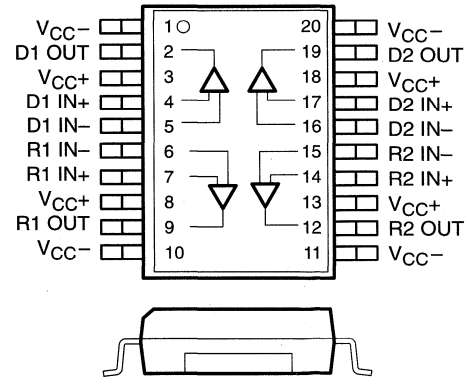
power supply

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	Single supply		5		V
		Split supply		±15		
I_{CC}	Quiescent current (per amplifier)	T_A = full range		20		mA
PSRR	Power supply rejection ratio	T_A = 25°C		89		dB
		T_A = full range				

SLOS202D– JANUARY 1998– REVISED JULY 1999

- **ADSL Differential Line Driver and Receiver**
- **Driver Features**
  - **140 MHz Bandwidth (–3dB) With 25-Ω Load**
  - **315 MHz Bandwidth (–3dB) With 100-Ω Load**
  - **1000 V/μs Slew Rate, G = 2**
  - **400 mA Output Current Minimum Into 25-Ω Load**
  - **–72 dB 3rd Order Harmonic Distortion at f = 1 MHz, 25-Ω Load, and 20 $V_{O(PP)}$**
- **Receiver Features**
  - **330 MHz Bandwidth (–3dB)**
  - **900 V/μs Slew Rate at G = 2**
  - **–76 dB 3rd Order Harmonic Distortion at f = 1 MHz, 150-Ω Load, and 20 $V_{O(PP)}$**
- **Wide Supply Range ±4.5 V to ±16 V**
- **Available in the PowerPAD™ Package**
- **Improved Replacement for AD816 or EL1501**
- **Evaluation Module Available**

DWP PACKAGE
(TOP VIEW)



Cross Section View Showing PowerPAD

description

The THS6002 contains two high-current, high-speed drivers and two high-speed receivers. These drivers and receivers can be configured differentially for driving and receiving signals over low-impedance lines. The THS6002 is ideally suited for asymmetrical digital subscriber line (ADSL) applications where it supports the high-peak voltage and current requirements of that application. Both the drivers and the receivers are current feedback amplifiers designed for the high slew rates necessary to support low total harmonic distortion (THD) in ADSL applications. Separate power supply connections for each driver are provided to minimize crosstalk.

HIGH-SPEED xDSL LINE DRIVER/RECEIVER FAMILY

DEVICE	DRIVER	RECEIVER	5 V	±5 V	±15 V	BW (MHz)	SR (V/μs)	THD f = 1 MHz (dB)	I_O (mA)	V_n (nV/√Hz)
THS6002	•	•		•	•	140	1000	–62	500	1.7
THS6012	•			•	•	140	1300	–65	500	1.7
THS6022	•			•	•	210	1900	–66	250	1.7
THS6062		•	•	•	•	100	100	–72	90	1.6
THS7002		•		•	•	70	100	–84	25	2.0

CAUTION: The THS6002 provides ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

PowerPAD is a trademark of Texas Instruments Incorporated.

description (continued)

The THS6002 is packaged in the patented PowerPAD package. This package provides outstanding thermal characteristics in a small footprint package, which is fully compatible with automated surface mount assembly procedures. The exposed thermal pad on the underside of the package is in direct contact with the die. By simply soldering the pad to the PWB copper and using other thermal outlets, the heat is conducted away from the junction.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE	
	PowerPAD PLASTIC SMALL OUTLINE† (DWP)	EVALUATION MODULE
0°C to 70°C	THS6002CDWP	THS6002EVM
–40°C to 85°C	THS6002IDWP	

† The DWP packages are available taped and reeled. Add an R suffix to the device type (i.e., THS6002CDWPR)

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC+} to V_{CC-} . . . . . 33 V
Input voltage, V_I (driver and receiver) . . . . . $\pm V_{CC}$
Output current, I_O (driver) (see Note 1) . . . . . 800 mA
Output current, I_O (receiver) (see Note 1) . . . . . 150 mA
Differential input voltage, V_{ID} (driver and receiver) . . . . . 6 V
Continuous total power dissipation at (or below) T_A = 25°C (see Note 1) . . . . . 5.8 W
Operating free air temperature, T_A . . . . . –40°C to 85°C
Storage temperature, T_{stg} . . . . . –65°C to 125°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

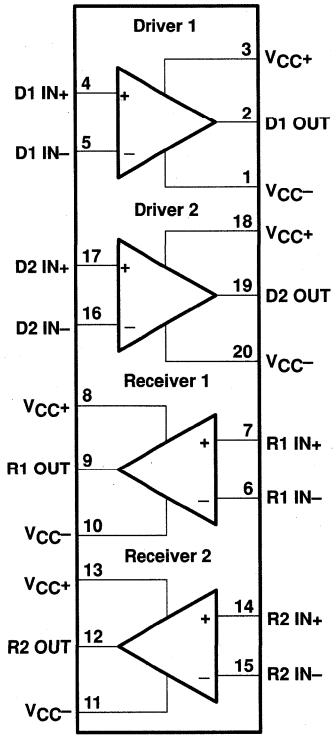
† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The THS6002 incorporates a PowerPad on the underside of the chip. This acts as a heatsink and must be connected to a thermal dissipation plane for proper power dissipation. Failure to do so can result in exceeding the maximum junction temperature, which could permanently damage the device. See the *Thermal Information* section of this document for more information about PowerPad technology.

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC+} and V_{CC-}	Split supply	±4.5		±16	V
	Single supply	9		32	
Operating free-air temperature, T_A	C suffix	0		70	°C
	I suffix	–40		85	

functional block diagram



DRIVER

electrical characteristics, V_{CC} = ±15 V, R_L = 25 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{CC}	Power supply operating range		Split supply		±4.5		±16.5	V
			Single supply		9		33	
V_O	Output voltage swing	Single ended	R_L = 25 Ω	V_{CC} = ±5 V	3 to −2.8	3.2 to −3		V
				V_{CC} = ±15 V	11.8 to −11.5	12.5 to −12.2		
		Differential	R_L = 50 Ω	V_{CC} = ±5 V	6 to −5.6	6.4 to −6		V
				V_{CC} = ±15 V	23.6 to −23	25 to −24.4		
V_{ICR}	Common-mode input voltage range		V_{CC} = ±5 V		±3.6	±3.7		V
			V_{CC} = ±15 V		±13.4	±13.5		
V_{IO}	Input offset voltage		V_{CC} = ±5 V or ±15 V	T_A = 25°C		2	5	mV
				T_A = full range			7	
	Input offset voltage drift		V_{CC} = ±5 V or ±15 V,	T_A = full range			20	µV/°C
	Differential input offset voltage		V_{CC} = ±5 V or ±15 V	T_A = 25°C		1.5	4	mV
				T_A = full range			5	
	Differential input offset voltage drift		V_{CC} = ±5 V or ±15 V,	T_A = full range			10	µV/°C
I_{IB}	Input bias current	Negative	V_{CC} = ±5 V or ±15 V	T_A = 25°C		3	9	µA
				T_A = full range			12	
		Positive		T_A = 25°C		4	10	µA
				T_A = full range			12	
		Differential		T_A = 25°C		1.5	8	µA
				T_A = full range			11	
I_O	Output current (see Note 2)		V_{CC} = ±5 V,	R_L = 5 Ω		500		mA
			V_{CC} = ±15 V,	R_L = 25 Ω	400	500		
I_{OS}	Short-circuit output current (see Note 2)					800		mA
	Open loop transresistance		V_{CC} = ±5 V			1.5		MΩ
			V_{CC} = ±15 V			5		
CMRR	Common-mode rejection ratio		V_{CC} = ±5 V or ±15 V,	T_A = full range	62	70		dB
	Differential common-mode rejection ratio					100		
	Crosstalk	Driver to driver	V_I = 200 mV,	f = 1 MHz		−62		dB

† Full range is 0°C to 70°C for the THS6002C and −40°C to 85°C for the THS6002I.

NOTE 2: A heat sink is required to keep the junction temperature below absolute maximum when an output is heavily loaded or shorted. See absolute maximum ratings and Thermal Information section.

DRIVER

electrical characteristics, V_{CC} = ±15 V, R_L = 25 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
PSRR	Power supply rejection ratio	V_{CC} = ±5 V	T_A = 25°C	−68	−74		dB
			T_A = full range	−65			
		V_{CC} = ±15 V	T_A = 25°C	−64	−72		dB
			T_A = full range	−62			
C_I	Differential input capacitance				1.4		pF
R_I	Input resistance				300		kΩ
R_O	Output resistance	Open loop			13		Ω
I_{CC}	Quiescent current	V_{CC} = ±5 V	T_A = 25°C		8.5	10	mA
			T_A = full range			12	
		V_{CC} = ±15 V	T_A = 25°C		11.5	13	
			T_A = full range			15	

† Full range is 0°C to 70°C for the THS6002C and −40°C to 85°C for the THS6002I.

operating characteristics, V_{CC} = ±15 V, R_L = 25 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Differential slew rate		V_O = 20 $V_{(PP)}$,	G = 2		1000		V/μs
t_s	Settling time to 0.1%		0 V to 10 V Step,	G = 2		70		ns
THD	Total harmonic distortion		$V_{O(PP)}$ = 20 V, R_F = 4 kΩ, G = 5,	f = 1 MHz		−62		dBc
V_n	Input voltage noise		V_{CC} = ±5 V or ±15 V, G = 2,	f = 10 kHz, Single-ended		1.7		nV/√Hz
I_n	Input noise current	Positive (IN+)	V_{CC} = ±5 V or ±15 V, G = 2	f = 10 kHz,		11.5		pA/√Hz
		Negative (IN–)				16		
BW	Small-signal bandwidth (–3 dB)		V_I = 200 mV, G = 1, R_F = 680 Ω	V_{CC} = ±5 V	90	110		MHz
				V_{CC} = ±15 V	110	140		MHz
			V_I = 200 mV, G = 2, R_F = 620 Ω	V_{CC} = ±15 V		120		MHz
			V_I = 200 mV, G = 1, R_F = 820 Ω, R_L = 100 Ω	V_{CC} = ±15 V		315		MHz
			V_I = 200 mV, G = 2, R_F = 560 Ω, R_L = 100 Ω	V_{CC} = ±15 V		265		MHz
	Bandwidth for 0.1 dB flatness		V_I = 200 mV, G = 1, R_F = 680 Ω	V_{CC} = ±5 V		30		MHz
				V_{CC} = ±15 V		40		
	Full power bandwidth (see Note 3)		V_O = 20 $V_{(PP)}$			16		MHz
A_D	Differential gain error		G = 2, R_L = 150 Ω, NTSC, 40 IRE	V_{CC} = ±5 V		0.04%		
				V_{CC} = ±15 V		0.05%		
ϕ_D	Differential phase error		G = 2, R_L = 150 Ω, NTSC, 40 IRE	V_{CC} = ±5 V		0.07°		
				V_{CC} = ±15 V		0.08°		

NOTE 3: Full power bandwidth = slew rate/$2\pi V_{peak}$

RECEIVER

electrical characteristics, V_{CC} = ±15 V, R_L = 150 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{CC}	Power supply operating range		Split supply		±4.5		±16.5	V
			Single supply		9		33	
V_O	Output voltage swing	Single ended	V_{CC} = ±5 V		±3	±3.3		V
			V_{CC} = ±15 V		±12.4	±12.8		
V_{ICR}	Common-mode input voltage range		V_{CC} = ±5 V		±3.6	±3.7		V
			V_{CC} = ±15 V		±13.4	±13.5		
V_{IO}	Input offset voltage	Single ended	V_{CC} = ±5 V or ±15 V	T_A = 25°C		1	4	mV
				T_A = full range			6	
		Differential		T_A = 25°C		1.5	4	
				T_A = full range			5	
	Input offset voltage drift	Single ended	V_{CC} = ±5 V or ±15 V				20	µV/°C
		Differential					10	
I_{IB}	Input bias current	Negative	V_{CC} = ±5 V or ±15 ,	T_A = 25°C		2	8	µA
				T_A = full range			10	
		Positive	V_{CC} = ±5 V or ±15 V	T_A = 25°C		3.5	9	
				T_A = full range			11	
		Differential	V_{CC} = ±5 V or ±15 V	T_A = 25°C		1.5	8	
				T_A = full range			10	
I_O	Output current (see Note 2)		V_{CC} = ±5 V	R_L = 25 Ω		95		mA
			V_{CC} = ±15 V	R_L = 150 Ω	80	85		
I_{OS}	Short-circuit output current (see Note 2)		R_L = 25 Ω			110		mA
	Open loop transresistance		V_{CC} = ±5 V			1.5		MΩ
			V_{CC} = ±15 V			5		
CMRR	Common-mode rejection ratio	Single ended	V_{CC} = ±5 V or ±15 V,	T_A = full range	60	70		dB
		Differential				100		
	Crosstalk (receiver to receiver)		V_I = 200 mV,	f = 1 MHz		–67		dB
PSRR	Power supply rejection ratio		V_{CC} = ±5 V	T_A = 25°C	–66	–74		dB
				T_A = full range	–63			
			V_{CC} = ±15 V	T_A = 25°C	–65	–72		
				T_A = full range	–62			
R_I	Input resistance					300		kΩ
C_I	Differential input capacitance					1.4		pF
R_O	Output resistance		Open loop			10		Ω

† Full range is 0°C to 70°C for the THS6002C and –40°C to 85°C for the THS6002I.

NOTE 2: A heat sink is required to keep junction temperature below absolute maximum when an output is heavily loaded or shorted. See absolute maximum ratings and Thermal Information section.

RECEIVER

electrical characteristics, V_{CC} = ±15 V, R_L = 150 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
I_{CC}	Quiescent current	V_{CC} = ±5 V	T_A = 25°C		4.2	5.5	mA
			T_A = full range			7.5	
		V_{CC} = ±15 V	T_A = 25°C		5	7	
			T_A = full range			9	

† Full range is 0°C to 70°C for the THS6002C and –40°C to 85°C for the THS6002I.

operating characteristics, V_{CC} = ±15 V, R_L = 150 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Differential slew rate		V_O = 10 $V_{(PP)}$,	G = 2		900		V/μs
t_s	Settling time to 0.1%		10 V Step,	G = 2		50		ns
THD	Total harmonic distortion		$V_{O(PP)}$ = 20 V, G = 5,	R_F = 510 Ω, f =1 MHz		–68		dBc
V_n	Input voltage noise		V_{CC} = ±5 V or ±15 V G = 2	f = 10 kHz,		1.7		nV/√Hz
I_n	Input current noise	Positive (IN+)	V_{CC} = ±5 V or ±15 V, G = 2	f = 10 kHz,		11.5		pA/√Hz
		Negative (IN–)				16		
BW	Small-signal bandwidth (–3 dB)		V_I = 200 mV, R_F = 560 Ω	G = 1, V_{CC} = ±5 V	270	300		MHz
				V_{CC} = ±15 V	300	330		
			V_I = 200 mV, R_F = 430 Ω	G = 2, V_{CC} = ±15 V		285		MHz
	Bandwidth for 0.1 dB flatness		V_I = 200 mV, R_F = 560 Ω	G = 1, V_{CC} = ±5 V		20		MHz
				V_{CC} = ±15 V		25		
	Full power bandwidth (see Note 3)		V_O = 20 $V_{(PP)}$			14		MHz
A_D	Differential gain error		40 IRE, R_L = 150 Ω,	G = 2, NTSC, V_{CC} = ±5 V		0.09%		
				V_{CC} = ±15 V		0.1%		
ϕ_D	Differential phase error		40 IRE, R_L = 150 Ω,	G = 2, NTSC, V_{CC} = ±5 V		0.13°		
				V_{CC} = ±15 V		0.16°		

NOTE 3: Full power bandwidth = slew rate/$2\pi V_{peak}$

PARAMETER MEASUREMENT INFORMATION

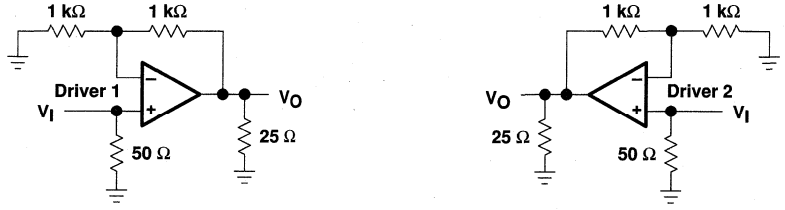


Figure 1. Driver Input-to-Output Crosstalk Test Circuit

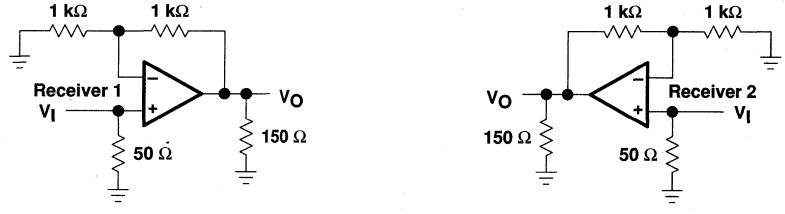


Figure 2. Receiver Input-to-Output Crosstalk Test Circuit

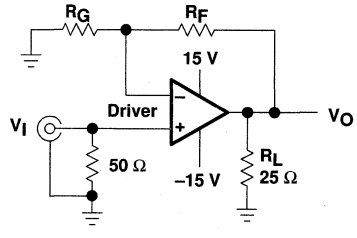


Figure 3. Driver Test Circuit, Gain = 1 + (R_F/R_G)

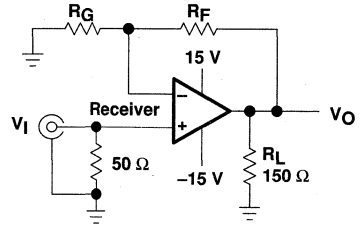


Figure 4. Receiver Test Circuit, Gain = 1 + (R_F/R_G)

TYPICAL CHARACTERISTICS

Table of Graphs

				FIGURE
	Supply current	Driver and Receiver	vs Supply voltage	5
	Input voltage noise	Driver and Receiver	vs Frequency	6
	Input current noise	Driver and Receiver	vs Frequency	6
	Closed-loop output impedance	Driver and Receiver	vs Frequency	7
	Peak-to-peak output voltage swing	Driver	vs Supply voltage	8
		Receiver	vs Supply voltage	31
	Peak-to-peak output voltage	Driver	vs Load resistance	9
		Receiver	vs Load resistance	32
V_{IO}	Input offset voltage	Driver	vs Free-air temperature	10
		Receiver	vs Free-air temperature	33
I_{IB}	Input bias current	Driver	vs Free-air temperature	11
		Receiver	vs Free-air temperature	34
CMMR	Common-mode rejection ratio	Driver	vs Free-air temperature	12
		Receiver	vs Free-air temperature	35
	Input-to-output crosstalk	Driver	vs Frequency	13
		Receiver	vs Frequency	36
	Driver-to-receiver crosstalk		vs Frequency	14
	Receiver-to-driver crosstalk		vs Frequency	37
PSSR	Power supply rejection ratio	Driver	vs Free-air temperature	15
		Receiver	vs Free-air temperature	38
I_{CC}	Supply current	Driver	vs Free-air temperature	16
		Receiver	vs Free-air temperature	39
	Normalized frequency response	Driver	vs Frequency	17, 18
		Receiver	vs Frequency	40, 41
	Normalized output response	Driver	vs Frequency	19 – 22
	Single-ended output distortion	Driver	vs Output voltage	23
	Output distortion	Receiver	vs Output voltage	42
	Small and large signal frequency response	Receiver		43, 44
	Differential gain	Driver	DC input offset voltage	24, 25
			Number of 150-Ω loads	26, 27
		Receiver	DC input offset voltage	45, 46
			Number of 150-Ω loads	47, 48
	Differential phase	Driver	DC input offset voltage	24, 25
			Number of 150-Ω loads	26, 27
		Receiver	DC input offset voltage	45, 46
			Number of 150-Ω loads	47, 48
	Output step response	Driver		28 – 30
		Receiver		49 – 51

TYPICAL CHARACTERISTICS

DRIVER AND RECEIVER
SUPPLY CURRENT
vs
SUPPLY VOLTAGE

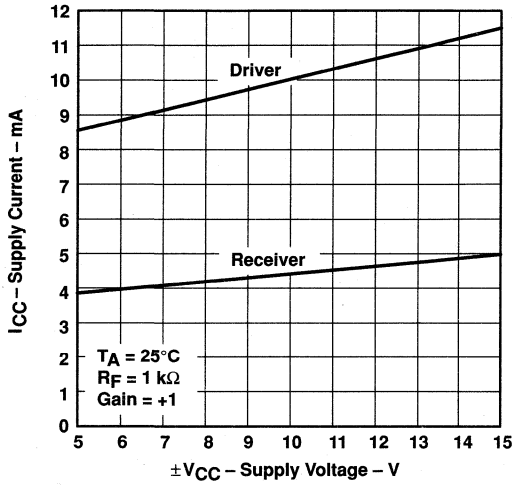


Figure 5

DRIVER AND RECEIVER
INPUT VOLTAGE AND CURRENT NOISE
vs
FREQUENCY

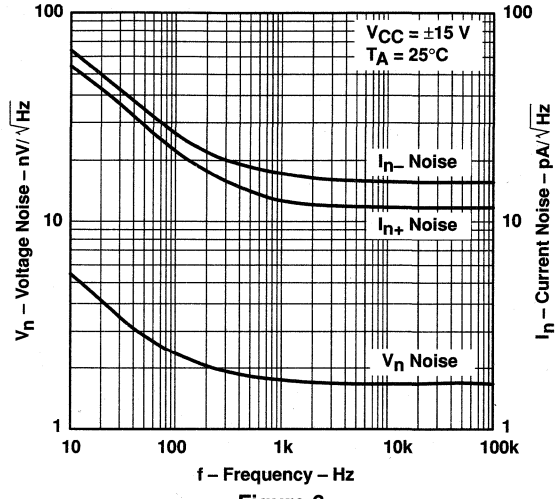


Figure 6

DRIVER AND RECEIVER
CLOSED-LOOP OUTPUT IMPEDANCE
vs
FREQUENCY

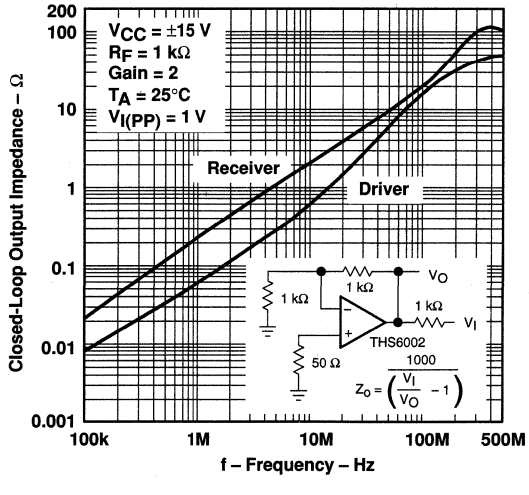


Figure 7

TYPICAL CHARACTERISTICS

DRIVER
PEAK-TO-PEAK OUTPUT VOLTAGE SWING
vs
SUPPLY VOLTAGE

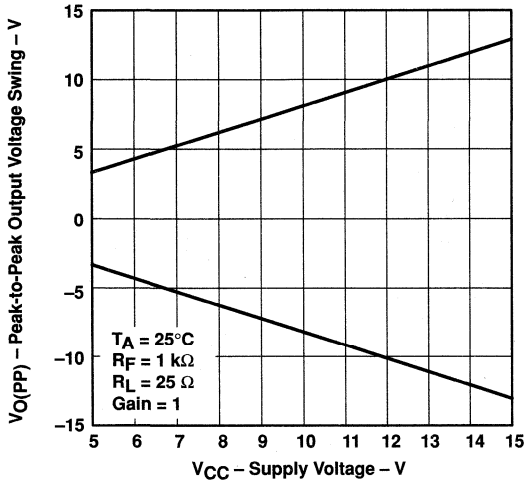


Figure 8

DRIVER
PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

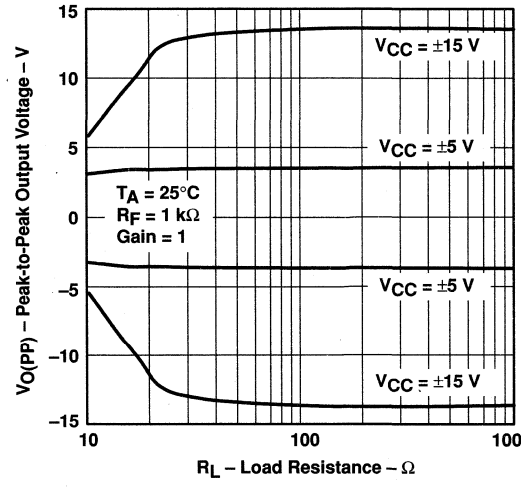


Figure 9

DRIVER
INPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

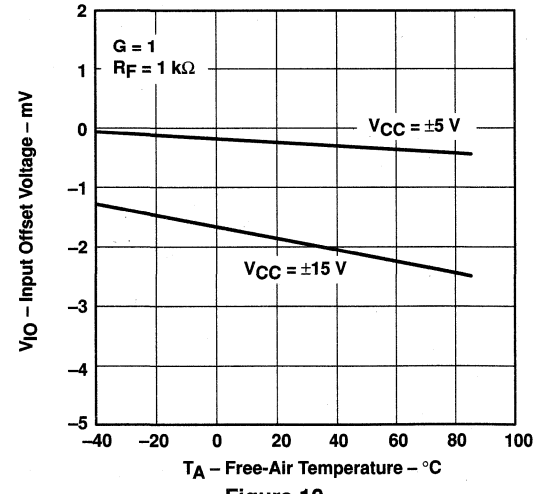


Figure 10

DRIVER
INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

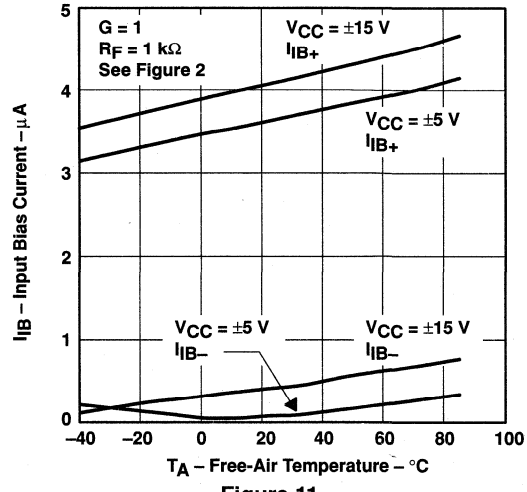


Figure 11

TYPICAL CHARACTERISTICS

DRIVER
COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

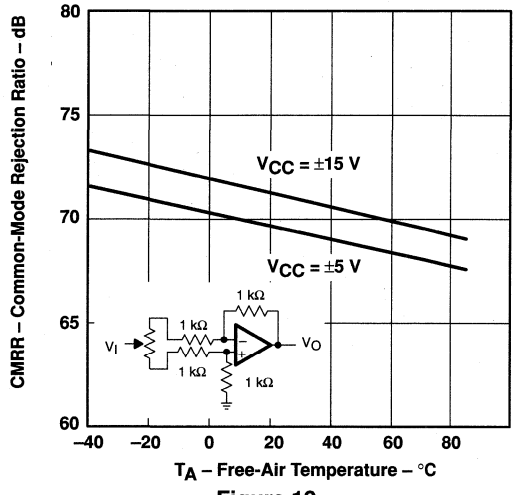


Figure 12

DRIVER
INPUT-TO-OUTPUT CROSSTALK
vs
FREQUENCY

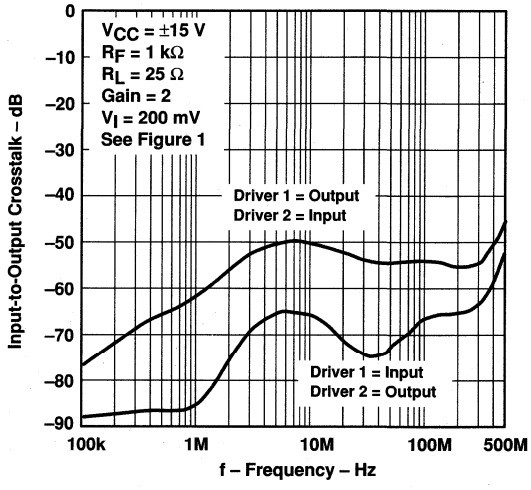


Figure 13

DRIVER-TO-RECEIVER CROSSTALK
vs
FREQUENCY

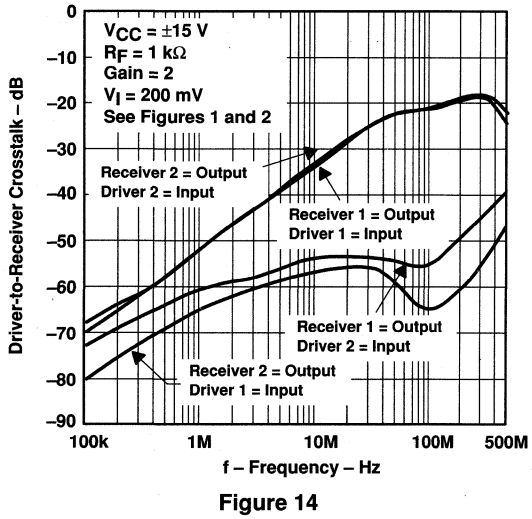


Figure 14

DRIVER
POWER SUPPLY REJECTION RATIO
vs
FREE-AIR TEMPERATURE

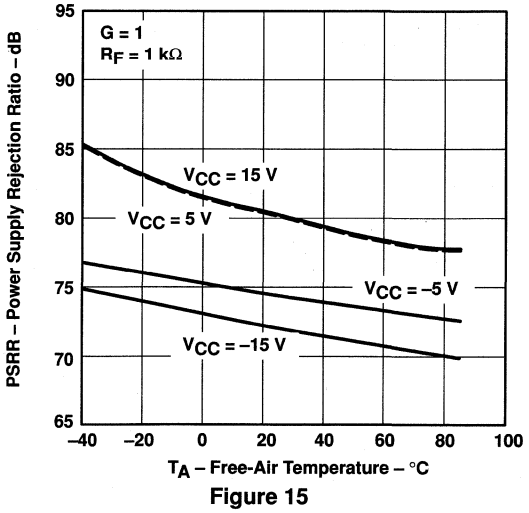


Figure 15

TYPICAL CHARACTERISTICS

DRIVER
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

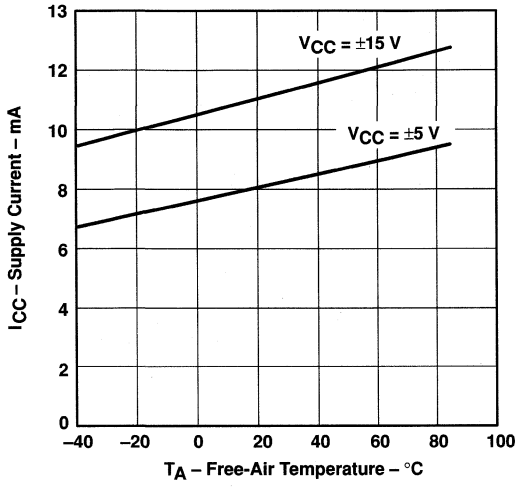


Figure 16

DRIVER
NORMALIZED FREQUENCY RESPONSE
vs
FREQUENCY

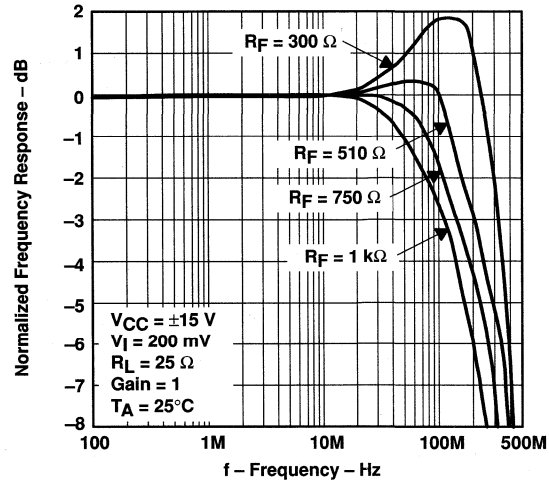


Figure 17

DRIVER
NORMALIZED FREQUENCY RESPONSE
vs
FREQUENCY

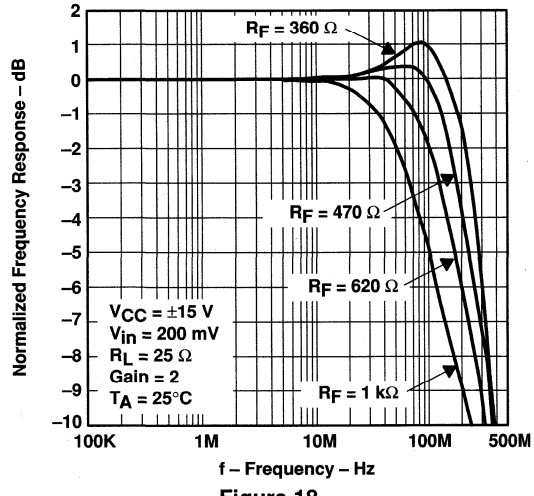


Figure 18

DRIVER
NORMALIZED OUTPUT RESPONSE
vs
FREQUENCY

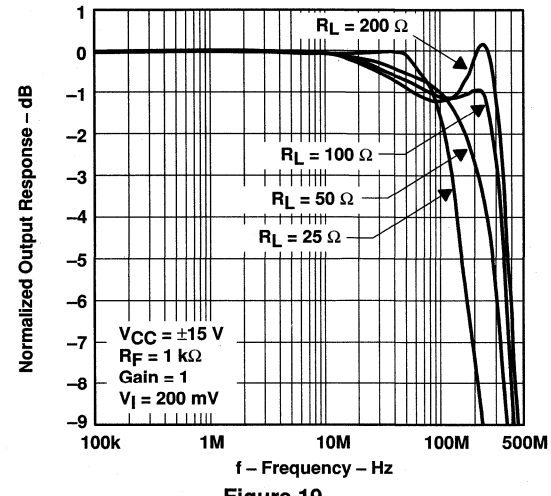


Figure 19

TYPICAL CHARACTERISTICS

DRIVER
NORMALIZED OUTPUT RESPONSE
vs
FREQUENCY

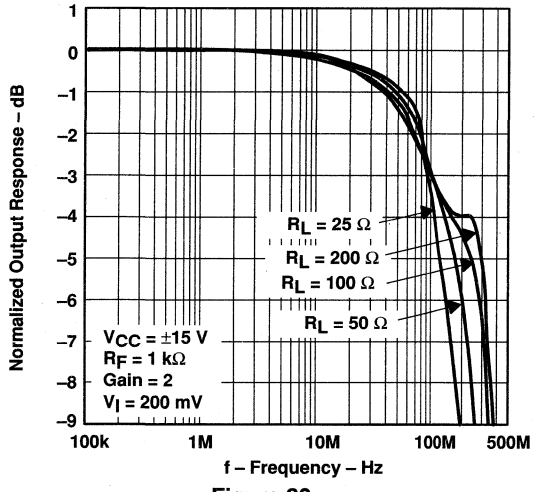


Figure 20

DRIVER
NORMALIZED OUTPUT RESPONSE
vs
FREQUENCY

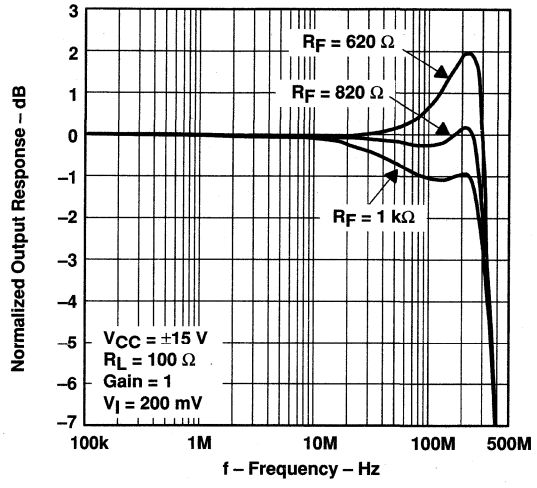


Figure 21

DRIVER
NORMALIZED OUTPUT RESPONSE
vs
FREQUENCY

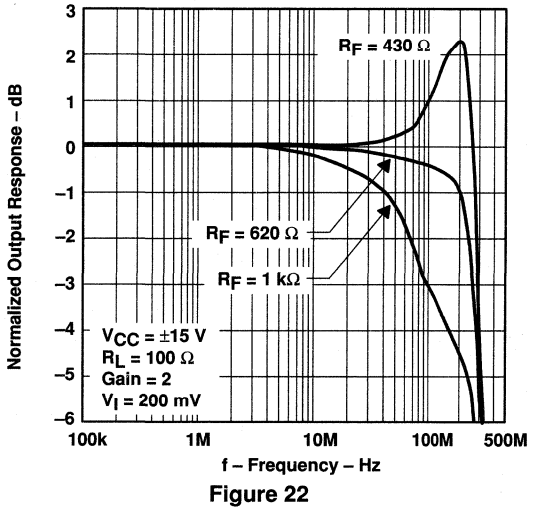


Figure 22

DRIVER
SINGLE-ENDED OUTPUT DISTORTION
vs
OUTPUT VOLTAGE

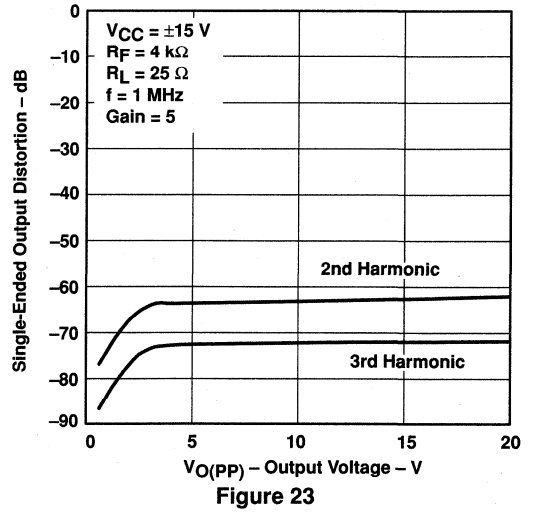


Figure 23

TYPICAL CHARACTERISTICS

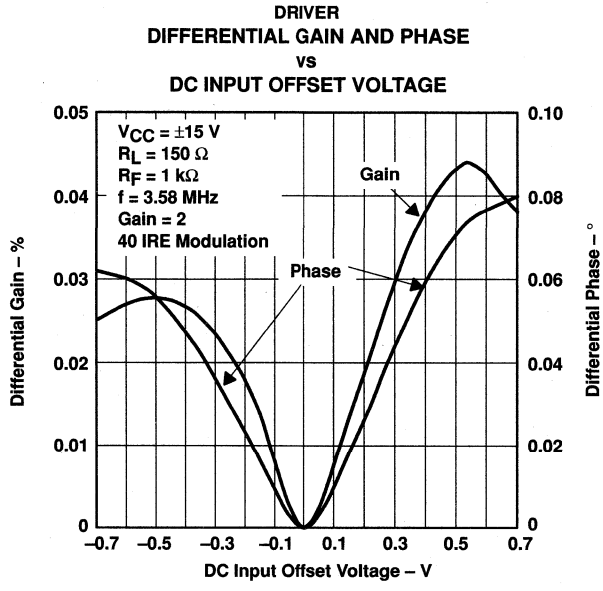


Figure 24

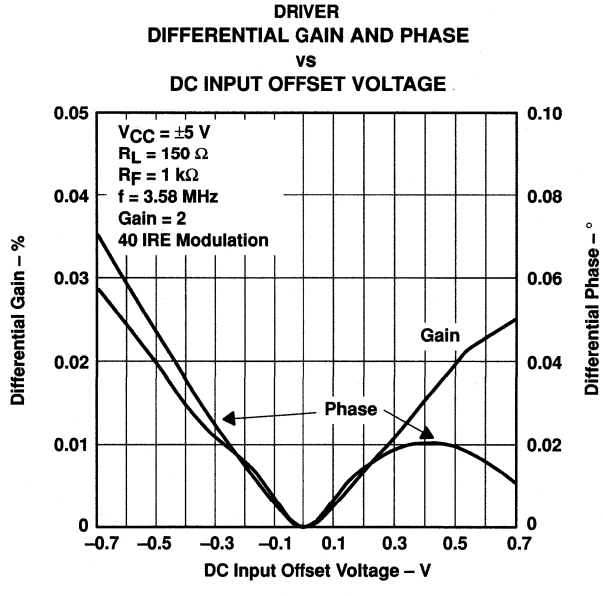


Figure 25

TYPICAL CHARACTERISTICS

DRIVER
DIFFERENTIAL GAIN AND PHASE
vs
NUMBER OF 150-Ω LOADS

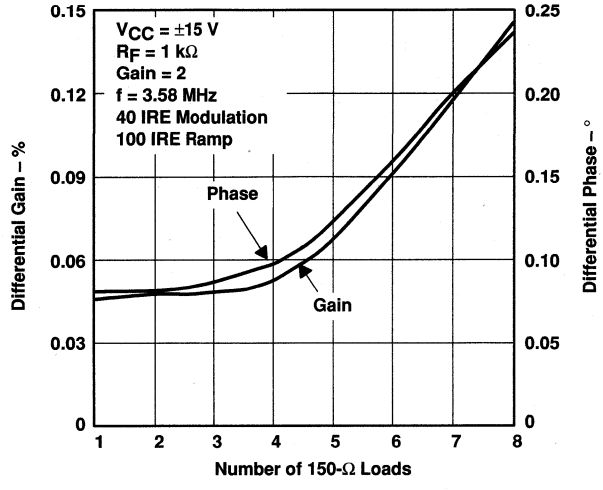


Figure 26

DRIVER
DIFFERENTIAL GAIN AND PHASE
vs
NUMBER OF 150-Ω LOADS

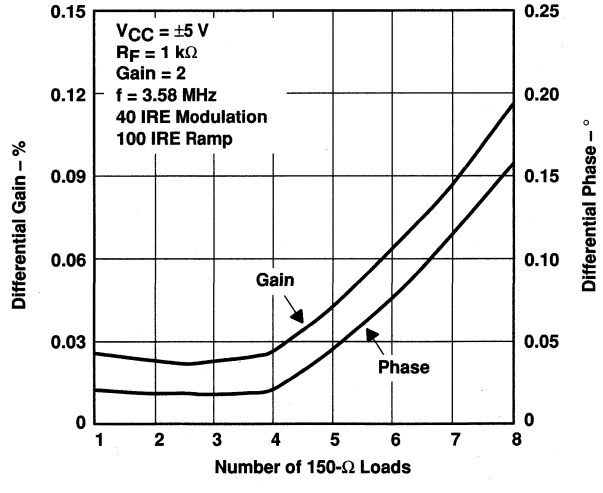


Figure 27

TYPICAL CHARACTERISTICS

DRIVER OUTPUT
400 mV STEP RESPONSE

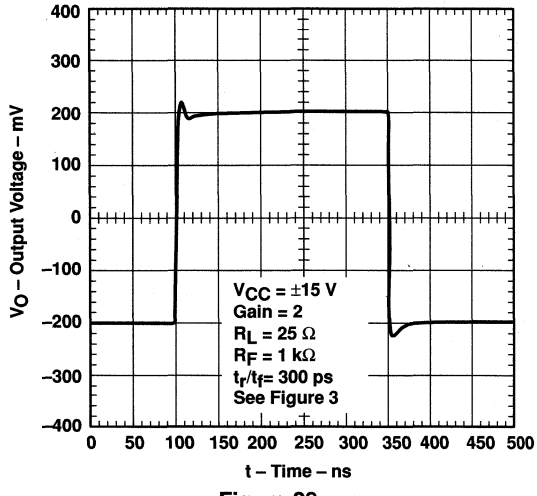


Figure 28

DRIVER OUTPUT
10 V STEP RESPONSE

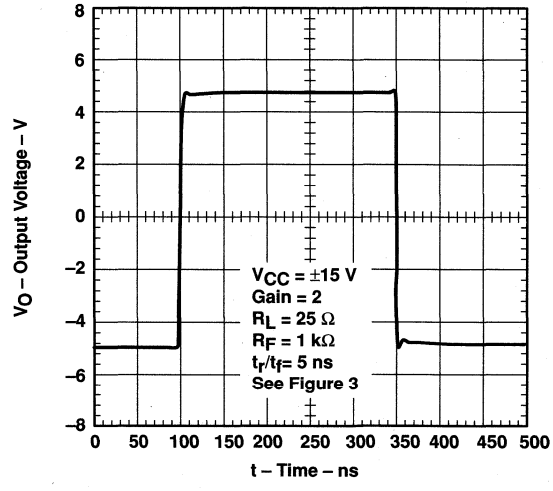


Figure 29

DRIVER OUTPUT
20 V STEP RESPONSE

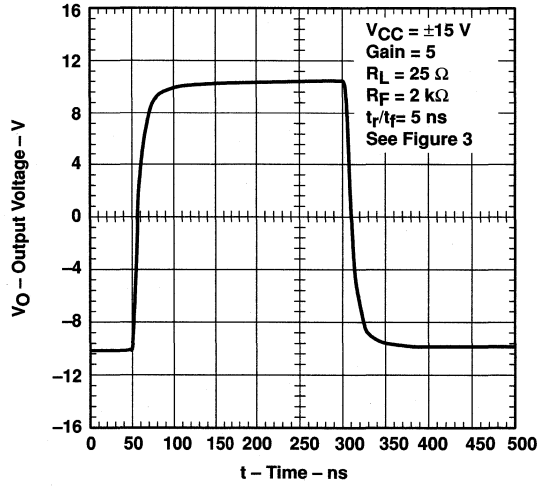


Figure 30

TYPICAL CHARACTERISTICS

RECEIVER
PEAK-TO-PEAK OUTPUT VOLTAGE SWING
vs
SUPPLY VOLTAGE

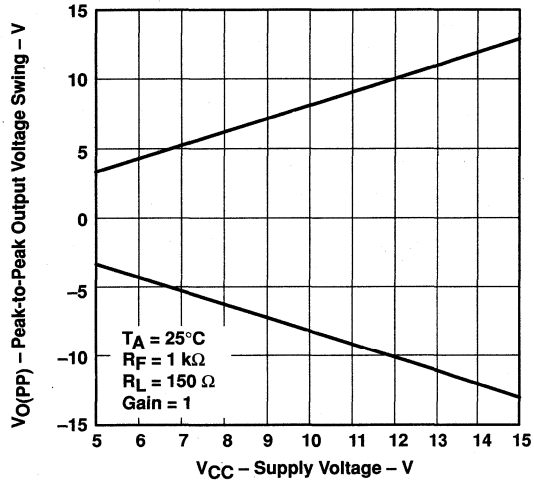


Figure 31

RECEIVER
PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

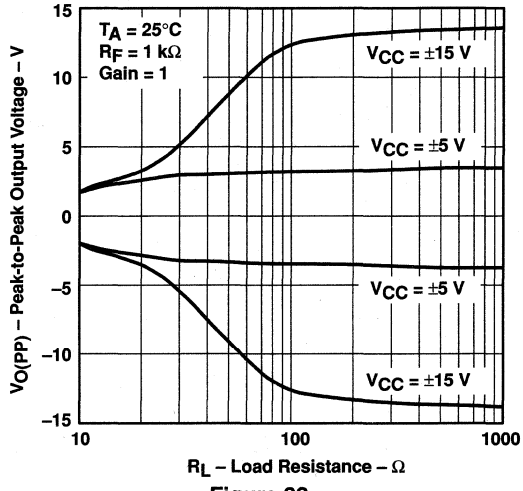


Figure 32

RECEIVER
INPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

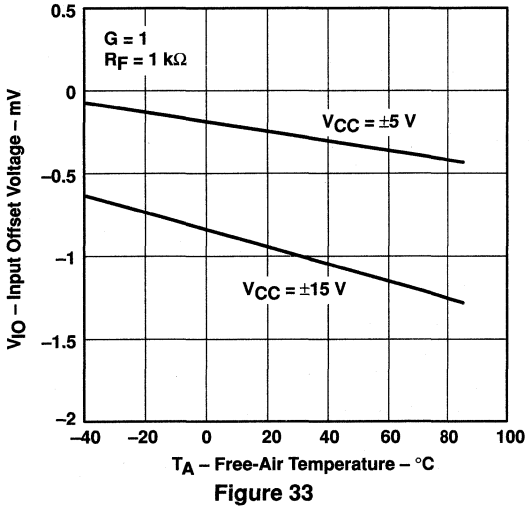


Figure 33

RECEIVER
INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

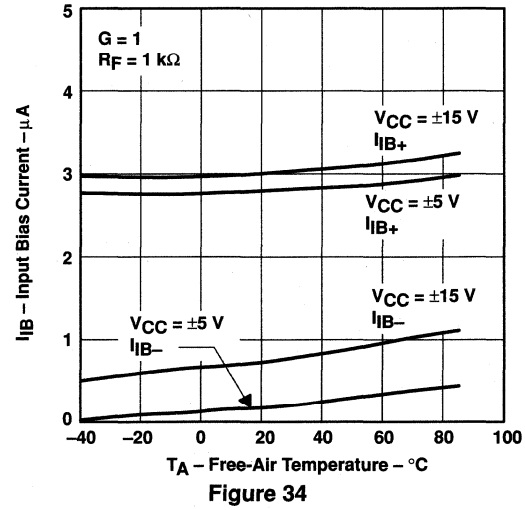


Figure 34

TYPICAL CHARACTERISTICS

RECEIVER
COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

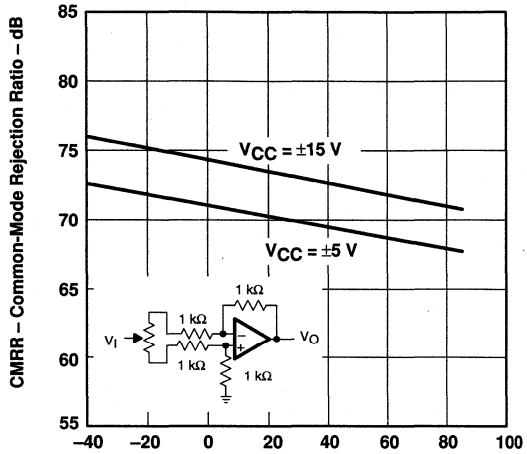


Figure 35

RECEIVER
INPUT-TO-OUTPUT CROSSTALK
vs
FREQUENCY

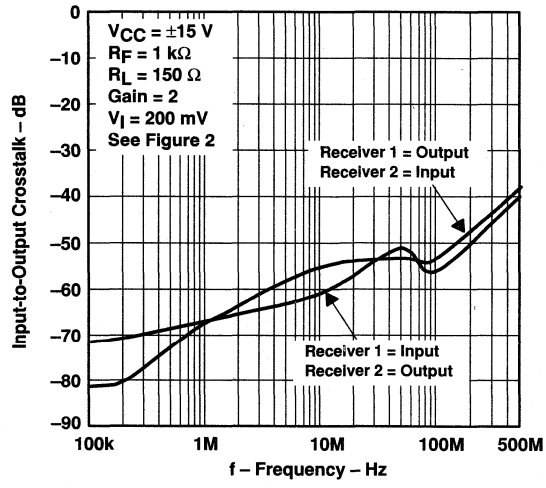


Figure 36

RECEIVER-TO-DRIVER CROSSTALK
vs
FREQUENCY

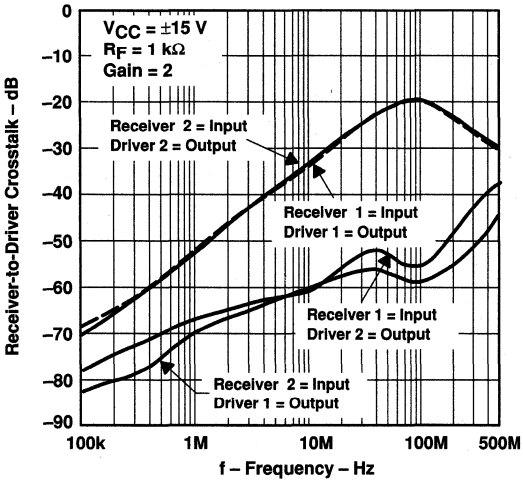


Figure 37

RECEIVER
POWER SUPPLY REJECTION RATIO
vs
FREE-AIR TEMPERATURE

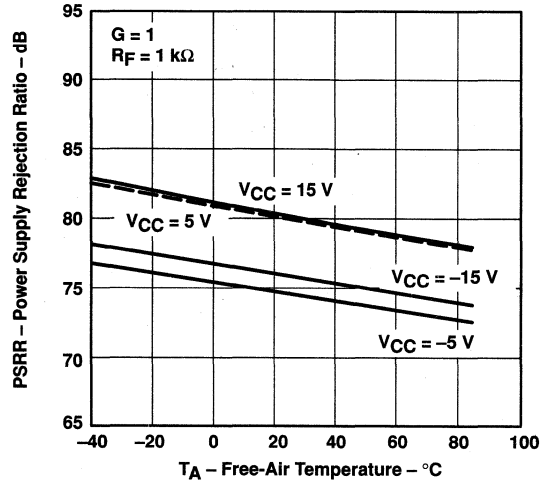


Figure 38

TYPICAL CHARACTERISTICS

RECEIVER
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

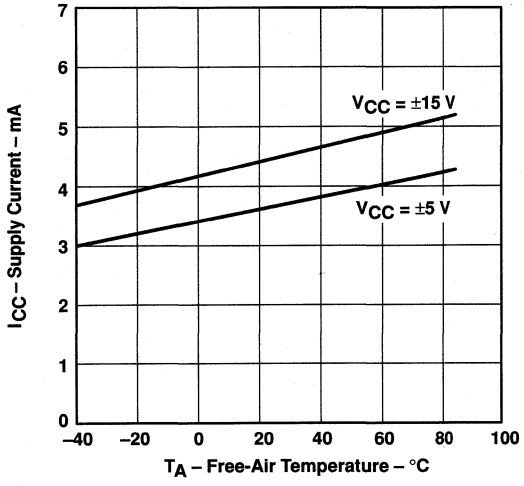


Figure 39

RECEIVER
NORMALIZED OUTPUT RESPONSE
vs
FREQUENCY

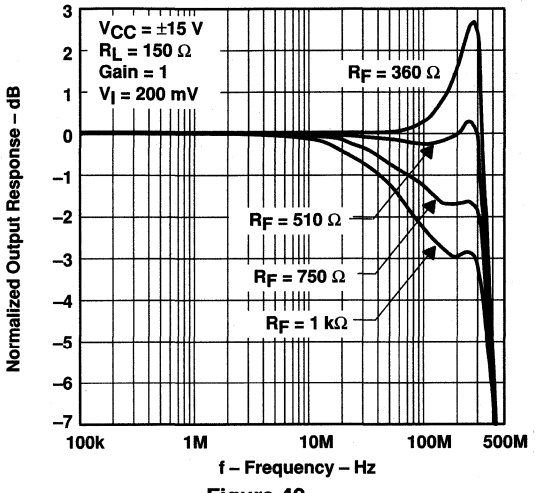


Figure 40

RECEIVER
NORMALIZED OUTPUT RESPONSE
vs
FREQUENCY

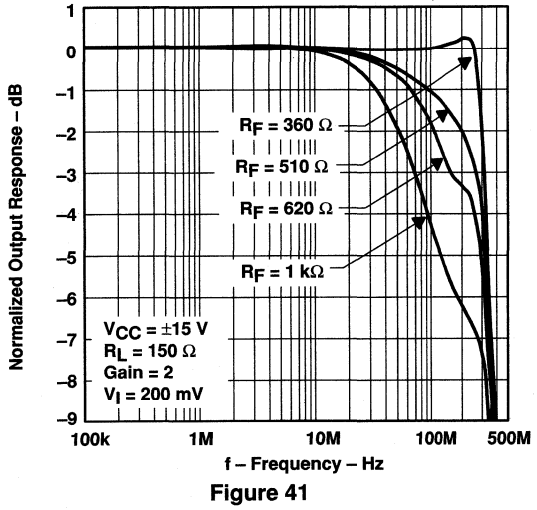


Figure 41

RECEIVER
OUTPUT DISTORTION
vs
OUTPUT VOLTAGE

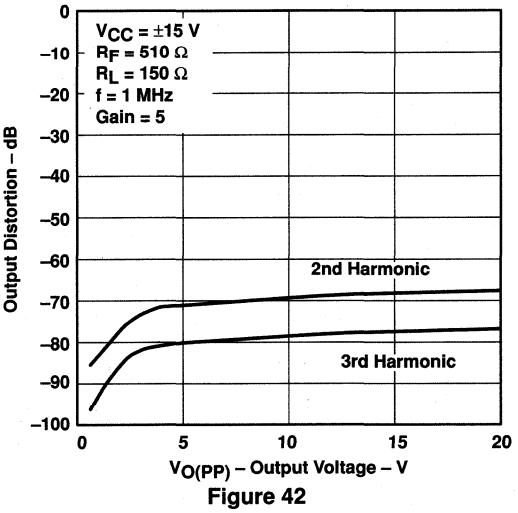


Figure 42

TYPICAL CHARACTERISTICS

RECEIVER
SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

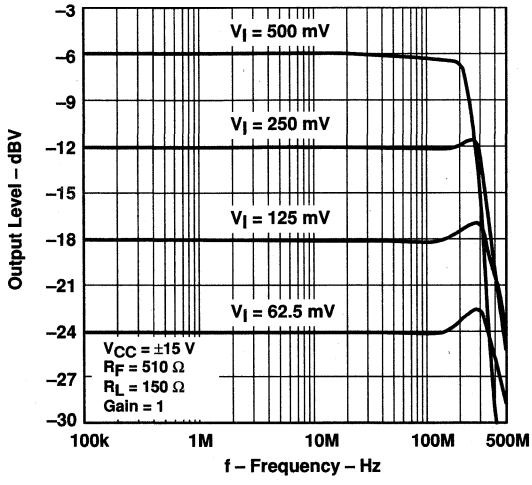


Figure 43

RECEIVER
SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

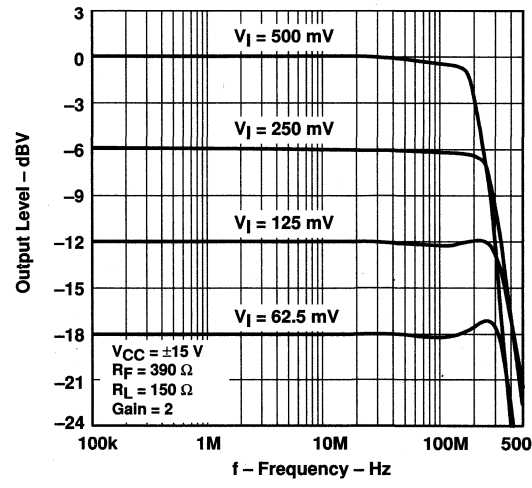


Figure 44

RECEIVER
DIFFERENTIAL GAIN AND PHASE
vs
DC INPUT OFFSET VOLTAGE

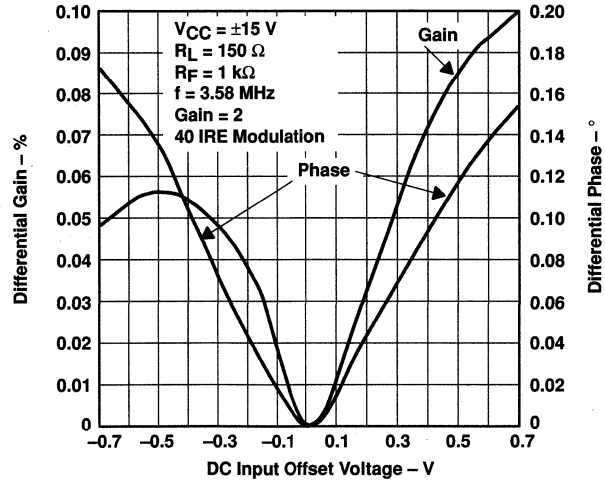


Figure 45

TYPICAL CHARACTERISTICS

RECEIVER
DIFFERENTIAL GAIN AND PHASE
vs
DC INPUT OFFSET VOLTAGE

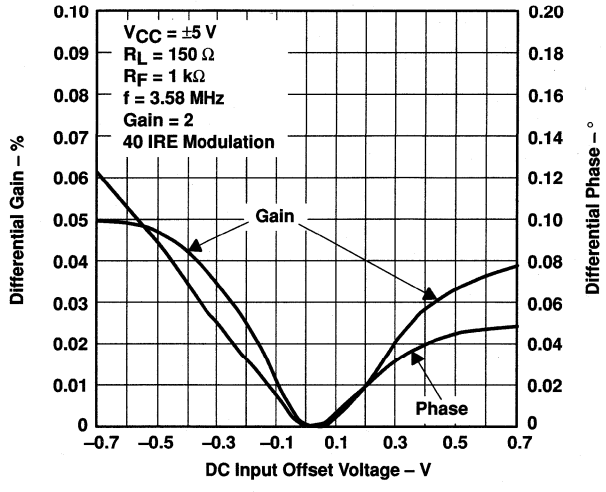


Figure 46

RECEIVER
DIFFERENTIAL GAIN AND PHASE
vs
NUMBER OF 150-Ω LOADS

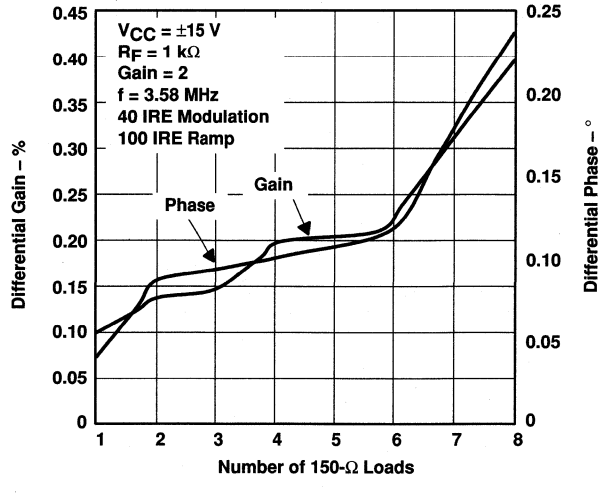


Figure 47

TYPICAL CHARACTERISTICS

RECEIVER
DIFFERENTIAL GAIN AND PHASE
vs
NUMBER OF 150-Ω LOADS

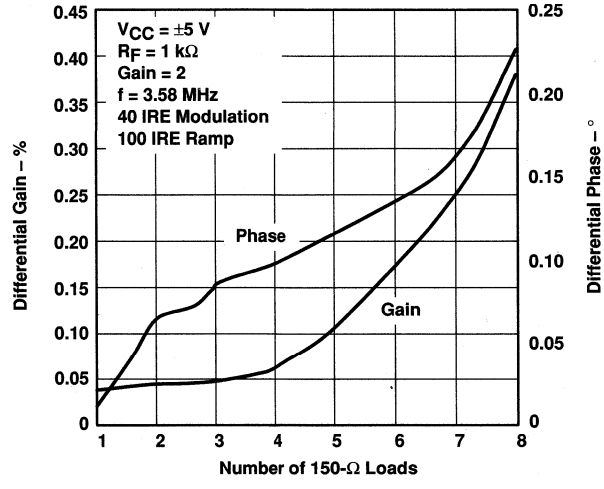


Figure 48

RECEIVER OUTPUT
400-mV STEP RESPONSE

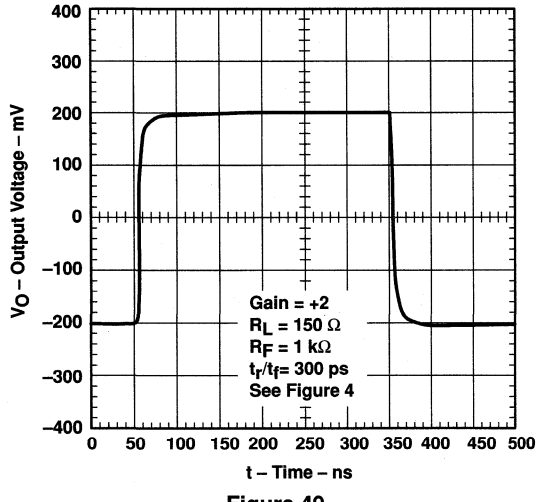


Figure 49

RECEIVER OUTPUT
10-V STEP RESPONSE

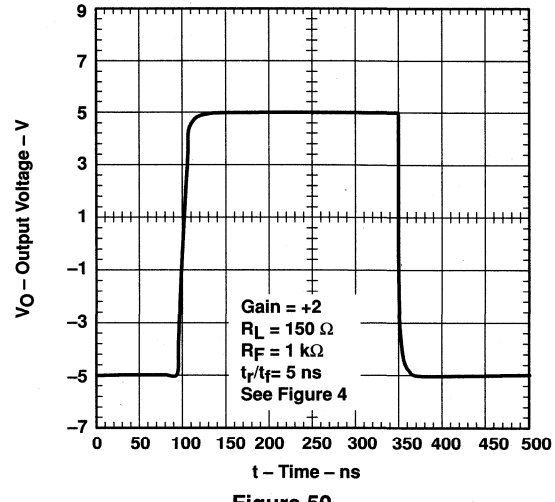


Figure 50

TYPICAL CHARACTERISTICS

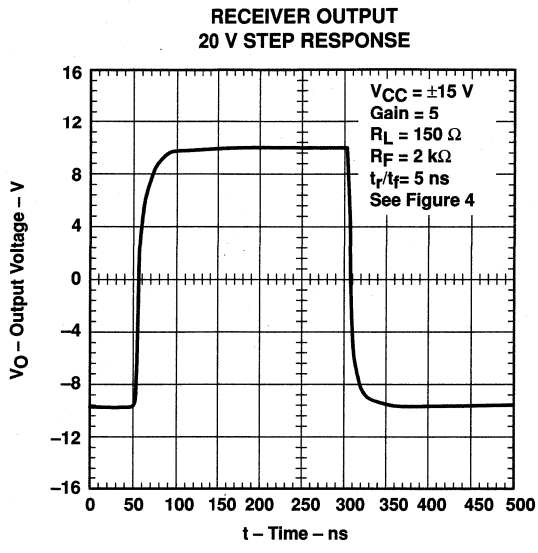


Figure 51

APPLICATION INFORMATION

The THS6002 contains four independent operational amplifiers. Two are designated as drivers because of their high output current capability, and two are designated as receivers. The receiver amplifiers are current feedback topology amplifiers made for high-speed operation and are capable of driving output loads of at least 80 mA. The drivers are also current feedback topology amplifiers. However, the drivers have been specifically designed to deliver the full power requirements of ADSL and therefore can deliver output currents of at least 400 mA at full output voltage.

The THS6002 is fabricated using Texas Instruments 30-V complementary bipolar process, HVBiCOM. This process provides excellent isolation and high slew rates that result in the device's excellent crosstalk and extremely low distortion.

independent power supplies

Each amplifier of the THS6002 has its own power supply pins. This was specifically done to solve a problem that often occurs when multiple devices in the same package share common power pins. This problem is crosstalk between the individual devices caused by currents flowing in common connections. Whenever the current required by one device flows through a common connection shared with another device, this current, in conjunction with the impedance in the shared line, produces an unwanted voltage on the power supply. Proper power supply decoupling and good device power supply rejection helps to reduce this unwanted signal. What is left is crosstalk.

However, with independent power supply pins for each device, the effects of crosstalk through common impedance in the power supplies is more easily managed. This is because it is much easier to achieve low common impedance on the PCB with copper etch than it is to achieve low impedance within the package with either bond wires or metal traces on silicon.

APPLICATION INFORMATION

power supply restrictions

Although the THS6002 is specified for operation from power supplies of ±5 V to ±15 V (or singled-ended power supply operation from 10 V to 30 V), and each amplifier has its own power supply pins, several precautions must be taken to assure proper operation.

1. The power supplies for each amplifier must be the same value. For example, if the drivers use ±15 volts, then the receivers must also use ±15 volts. Using ±15 volts for one amplifier and ±5 volts for another amplifier is not allowed.
2. To save power by powering down some of the amplifiers in the package, the following rules must be followed.
   - The amplifier designated Receiver 1 must always receive power whenever any other amplifier(s) within the package is used. This is because the internal startup circuitry uses the power from the Receiver 1 device.
   - The $-V_{CC}$ pins from all four devices must always be at the same potential.
   - Individual amplifiers are powered down by simply opening the $+V_{CC}$ connection.

As an example, if only the two drivers within the THS6002 are used, then the package power is reduced by removing the $+V_{CC}$ connection to Receiver 2. This reduces the power consumption by an amount equal to the quiescent power of a single receiver amplifier. The $+V_{CC}$ connections to Receiver 1 and both drivers are required. Also, all four amplifiers must be connected to $-V_{CC}$, including Receiver 2.

The THS6002 incorporates a standard Class A-B output stage. This means that some of the quiescent current is directed to the load as the load current increases. So under heavy load conditions, accurate power dissipation calculations are best achieved through actual measurements. For small loads, however, internal power dissipation for each amplifier in the THS6002 can be approximated by the following formula:

$$P_D \cong \left(2\ V_{CC}\ I_{CC}\right) + \left(V_{CC} - V_O\right) \times \left(\frac{V_O}{R_L}\right)$$

Where:

P_D = power dissipation for one amplifier
V_{CC} = split supply voltage
I_{CC} = supply current for that particular amplifier
V_O = output voltage of amplifier
R_L = load resistance

To find the total THS6002 power dissipation, we simply sum up all four amplifier power dissipation results. Generally, the worst case power dissipation occurs when the output voltage is one-half the V_{CC} voltage. One last note, which is often overlooked: the feedback resistor (R_F) is also a load to the output of the amplifier and should be taken into account for low value feedback resistors.

APPLICATION INFORMATION

device protection features

The THS6002 has two built-in protection features that protect the device against improper operation. The first protection mechanism is output current limiting. Should the output become shorted to ground the output current is automatically limited to the value given in the data sheet. While this protects the output against excessive current, the device internal power dissipation increases due to the high current and large voltage drop across the output transistors. Continuous output shorts are not recommended and could damage the device. Additionally, connection of the amplifier output to one of the supply rails ($\pm V_{CC}$) can cause failure of the device and is not recommended.

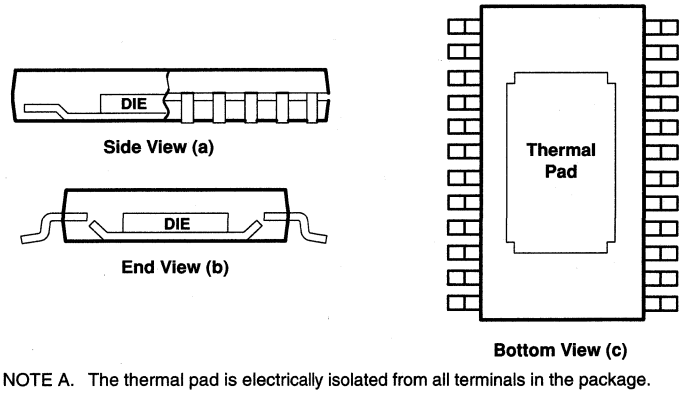
The second built-in protection feature is thermal shutdown. Should the internal junction temperature rise above approximately 180°C, the device automatically shuts down. Such a condition could exist with improper heat sinking or if the output is shorted to ground. When the abnormal condition is fixed, the internal thermal shutdown circuit automatically turns the device back on.

thermal information

The THS6002 is packaged in a thermally-enhanced DWP package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 52(a) and Figure 52(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 52(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device. This is discussed in more detail in the *PCB design considerations* section of this document.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.



NOTE A. The thermal pad is electrically isolated from all terminals in the package.

Figure 52. Views of Thermally Enhanced DWP Package

APPLICATION INFORMATION

recommended feedback and gain resistor values

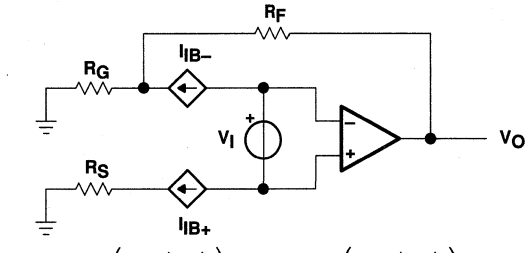
As with all current feedback amplifiers, the bandwidth of the THS6002 is an inversely proportional function of the value of the feedback resistor. This can be seen from Figures 17 and 18. For the driver, the recommended resistors for the optimum frequency response for a 25-Ω load system are 680-Ω for a gain = 1 and 620-Ω for a gain = 2 or –1. For the receivers, the recommended resistors for the optimum frequency response are 560 Ω for a gain = 1 and 390 Ω for a gain = 2 or –1. These should be used as a starting point and once optimum values are found, 1% tolerance resistors should be used to maintain frequency response characteristics. Because there is a finite amount of output resistance of the operational amplifier, load resistance can play a major part in frequency response. This is especially true with the drivers, which tend to drive low-impedance loads. This can be seen in Figure 7, Figure 19, and Figure 20. As the load resistance increases, the output resistance of the amplifier becomes less dominant at high frequencies. To compensate for this, the feedback resistor should change. For 100-Ω loads, it is recommended that the feedback resistor be changed to 820 Ω for a gain of 1 and 560 Ω for a gain of 2 or –1. Although, for most applications, a feedback resistor value of 1 kΩ is recommended, which is a good compromise between bandwidth and phase margin that yields a very stable amplifier.

Consistent with current feedback amplifiers, increasing the gain is best accomplished by changing the gain resistor, not the feedback resistor. This is because the bandwidth of the amplifier is dominated by the feedback resistor value and internal dominant-pole capacitor. The ability to control the amplifier gain independently of the bandwidth constitutes a major advantage of current feedback amplifiers over conventional voltage feedback amplifiers. Therefore, once a frequency response is found suitable to a particular application, adjust the value of the gain resistor to increase or decrease the overall amplifier gain.

Finally, it is important to realize the effects of the feedback resistance on distortion. Increasing the resistance decreases the loop gain and increases the distortion. It is also important to know that decreasing load impedance increases total harmonic distortion (THD). Typically, the third order harmonic distortion increases more than the second order harmonic distortion.

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

Figure 53. Output Offset Voltage Model

APPLICATION INFORMATION

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true for the receiver amplifiers which are generally used for amplifying small signals coming over a transmission line. The noise model for current feedback amplifiers (CFB) is the same as voltage feedback amplifiers (VFB). The only difference between the two is that the CFB amplifiers generally specify different current noise parameters for each input while VFB amplifiers usually only specify one noise current parameter. The noise model is shown in Figure 54. This model includes all of the noise sources as follows:

- e_n = amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = noninverting current noise (pA/$\sqrt{Hz}$)
- IN– = inverting current noise (pA/$\sqrt{Hz}$)
- e_{Rx} = thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR_x)

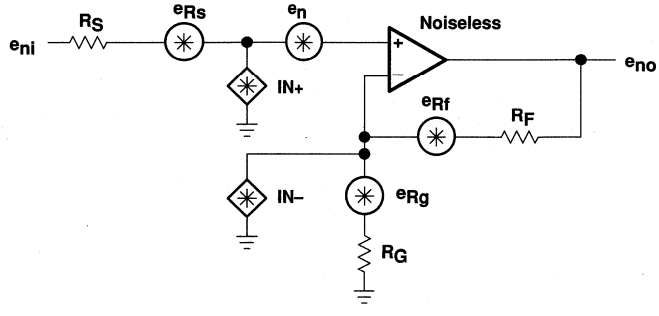


Figure 54. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN+ \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\ kTR_s + 4\ kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\ A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)}$$

APPLICATION INFORMATION

noise calculations and noise figure (continued)

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^2}{e_{Rs}}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\ kTR_S}\right]$$

The Figure 55 shows the noise figure graph for the THS6002.

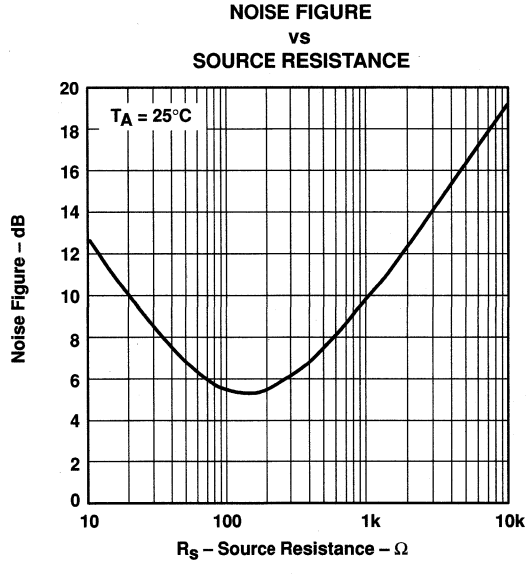


Figure 55. Noise Figure vs. Source Resistance

APPLICATION INFORMATION

PCB design considerations

Proper PCB design techniques in two areas are important to assure proper operation of the THS6002. These areas are high-speed layout techniques and thermal-management techniques. Because the THS6002 is a high-speed part, the following guidelines are recommended.

- Ground plane – It is essential that a ground plane be used on the board to provide all components with a low inductive ground connection. Although a ground connection directly to a terminal of the THS6002 is not necessarily required, it is recommended that the thermal pad of the package be tied to ground. This serves two functions. It provides a low inductive ground to the device substrate to minimize internal crosstalk and it provides the path for heat removal.
- Input stray capacitance – To minimize potential problems with amplifier oscillation, the capacitance at the inverting input of the amplifiers must be kept to a minimum. To do this, PCB trace runs to the inverting input must be as short as possible, the ground plane must be removed under any etch runs connected to the inverting input, and external components should be placed as close as possible to the inverting input. This is especially true in the noninverting configuration. An example of this can be seen in Figure 56, which shows what happens when 1.8 pF is added to the inverting input terminal in the noninverting configuration. The bandwidth increases dramatically at the expense of peaking. This is because some of the error current is flowing through the stray capacitor instead of the inverting node of the amplifier. Although, in the inverting mode, stray capacitance at the inverting input has little effect. This is because the inverting node is at a *virtual ground* and the voltage does not fluctuate nearly as much as in the noninverting configuration.

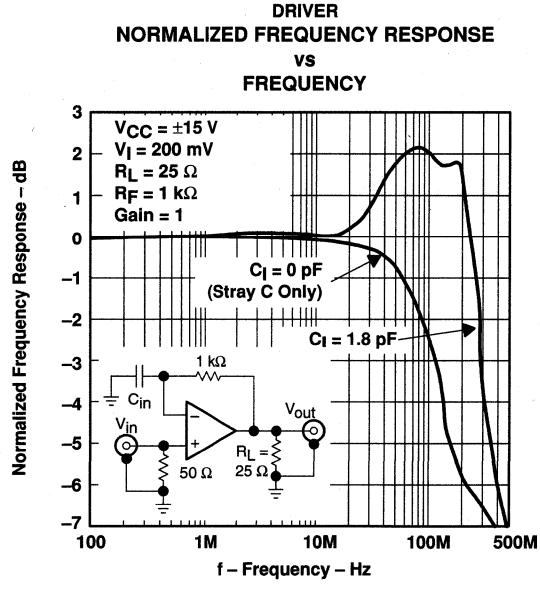


Figure 56. Driver Normalized Frequency Response vs. Frequency

APPLICATION INFORMATION

PCB design considerations (continued)

- Proper power supply decoupling – Use a minimum of a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting etch makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminal and the ceramic capacitors.

Because of its power dissipation, proper thermal management of the THS6002 is required. Although there are many ways to properly heatsink this device, the following steps illustrate one recommended approach for a multilayer PCB with an internal ground plane.

1. Prepare the PCB with a top side etch pattern as shown in Figure 57. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
3. Place four more holes under the package, but outside the thermal pad area. These holes are 25 mils in diameter. They may be larger because they are not in the area to be soldered so that wicking is not a problem.
4. Connect all nine holes, the five within the thermal pad area and the four outside the pad area, to the internal ground plane.
5. When connecting these holes to the ground plane, do **not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS6002 package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated through hole.
6. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area with its five holes. The four larger holes outside the thermal pad area, but still under the package, should be covered with solder mask.
7. Apply solder paste to the exposed thermal pad area and all of the operational amplifier terminals.
8. With these preparatory steps in place, the THS6002 is simply placed in position and run through the solder reflow operation as any standard surface mount component. This results in a part that is properly installed.

APPLICATION INFORMATION

PCB design considerations (continued)

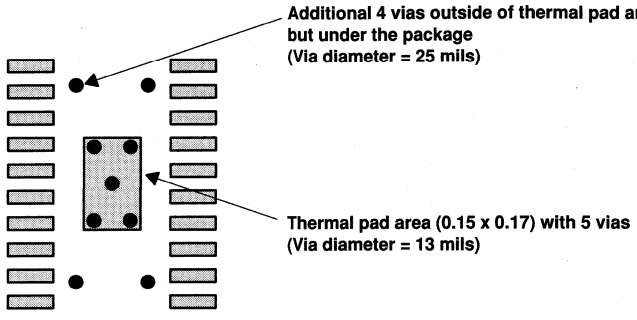


Figure 57. PowerPad PCB Etch and Via Pattern

The actual thermal performance achieved with the THS6002 in its PowerPAD package depends on the application. In the previous example, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA}, is about 21.5°C/W. For a given θ_{JA}, the maximum power dissipation is shown in Figure 58 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS6002 (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case (0.37°C/W)
θ_{CA} = Thermal coefficient from case to ambient

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

APPLICATION INFORMATION

PCB design considerations (continued)

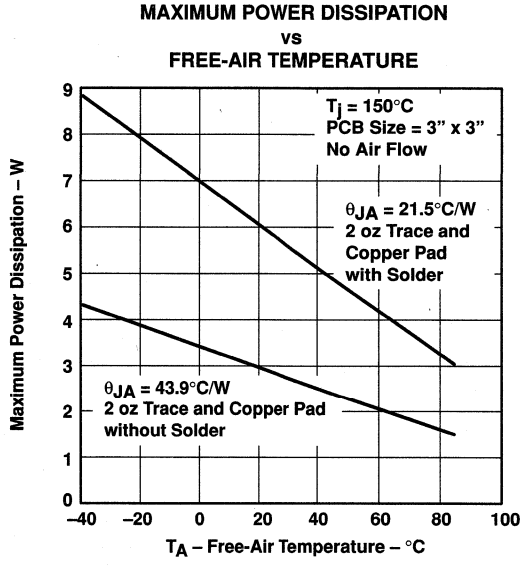


Figure 58. Maximum Power Dissipation vs Free-Air Temperature

APPLICATION INFORMATION

ADSL

The THS6002 was primarily designed as a line driver and line receiver for ADSL (asymmetrical digital subscriber line). The driver output stage has been sized to provide full ADSL power levels of 20 dBm onto the telephone lines. Although actual driver output peak voltages and currents vary with each particular ADSL application, the THS6002 is specified for a minimum full output current of 400 mA at its full output voltage of approximately 12 V. This performance meets the demanding needs of ADSL at the central office end of the telephone line. A typical ADSL schematic is shown in Figure 59.

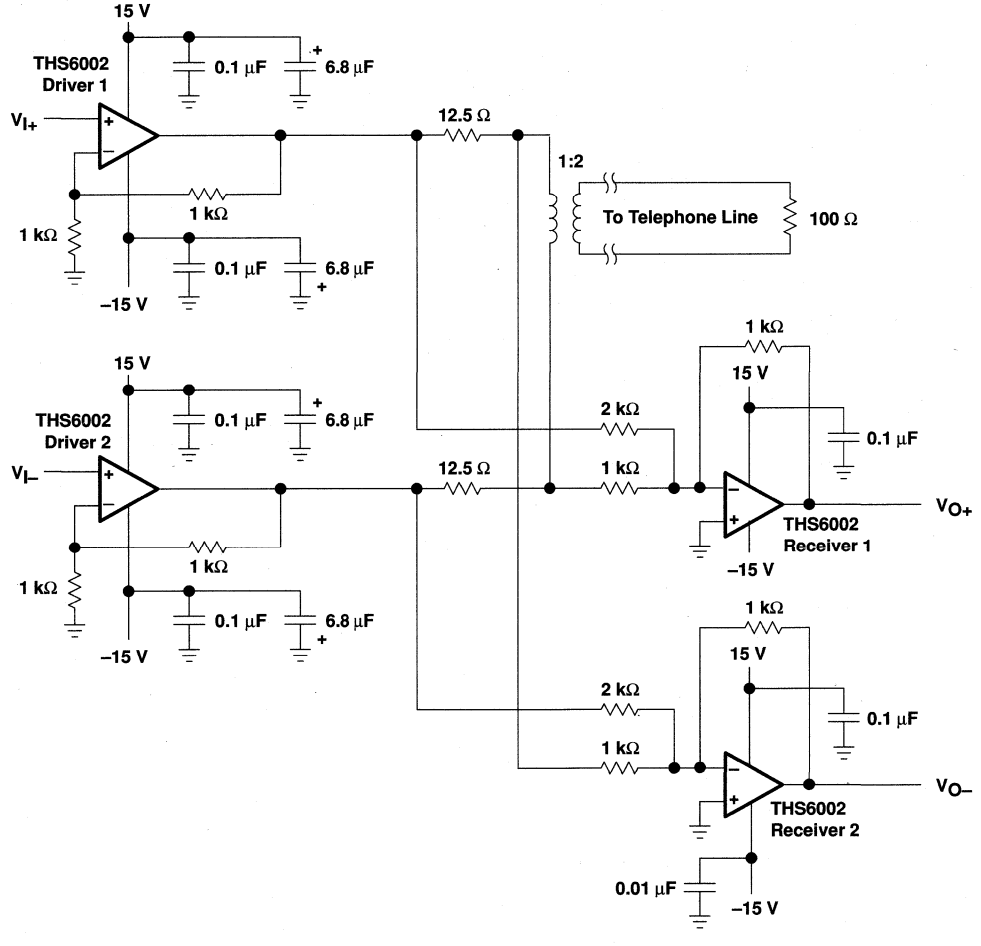


Figure 59. THS6002 ADSL Application

APPLICATION INFORMATION

ADSL (continued)

The ADSL transmit band consists of 255 separate carrier frequencies each with its own modulation and amplitude level. With such an implementation, it is imperative that signals put onto the telephone line have as low a distortion as possible. This is because any distortion either interferes directly with other ADSL carrier frequencies or it creates intermodulation products that interfere with ADSL carrier frequencies.

The THS6002 has been specifically designed for ultra low distortion by careful circuit implementation and by taking advantage of the superb characteristics of the complementary bipolar process. Driver single-ended distortion measurements are shown in Figure 23. It is commonly known that in the differential driver configuration, the second order harmonics tend to cancel out. Thus, the dominant total harmonic distortion (THD) will be primarily due to the third order harmonics. For this test, the load was 25 Ω and the output signal produced a 20 $V_{O(PP)}$ signal. Thus, the test was run at full signal and full load conditions. Because the feedback resistor used for the test was 4 kΩ, the distortion numbers are actually in a worst-case scenario. Distortion should be reduced as the feedback resistance drops. This is because the bandwidth of the amplifier increases dramatically, which allows the amplifier to react faster to any nonlinearities in the closed-loop system.

Another significant point is the fact that distortion decreases as the impedance load increases. This is because the output resistance of the amplifier becomes less significant as compared to the output load resistance.

APPLICATION INFORMATION

HDSL

Shown in Figure 60 is an example of the THS6002 being used for HDSL-2 applications. The receiver amplifiers within the THS6002 have been configured as predrivers for the driver amplifiers. This dual composite amplifier setup has the effect of raising the open loop gain for the combination of both amplifiers, thereby giving improved distortion performance.

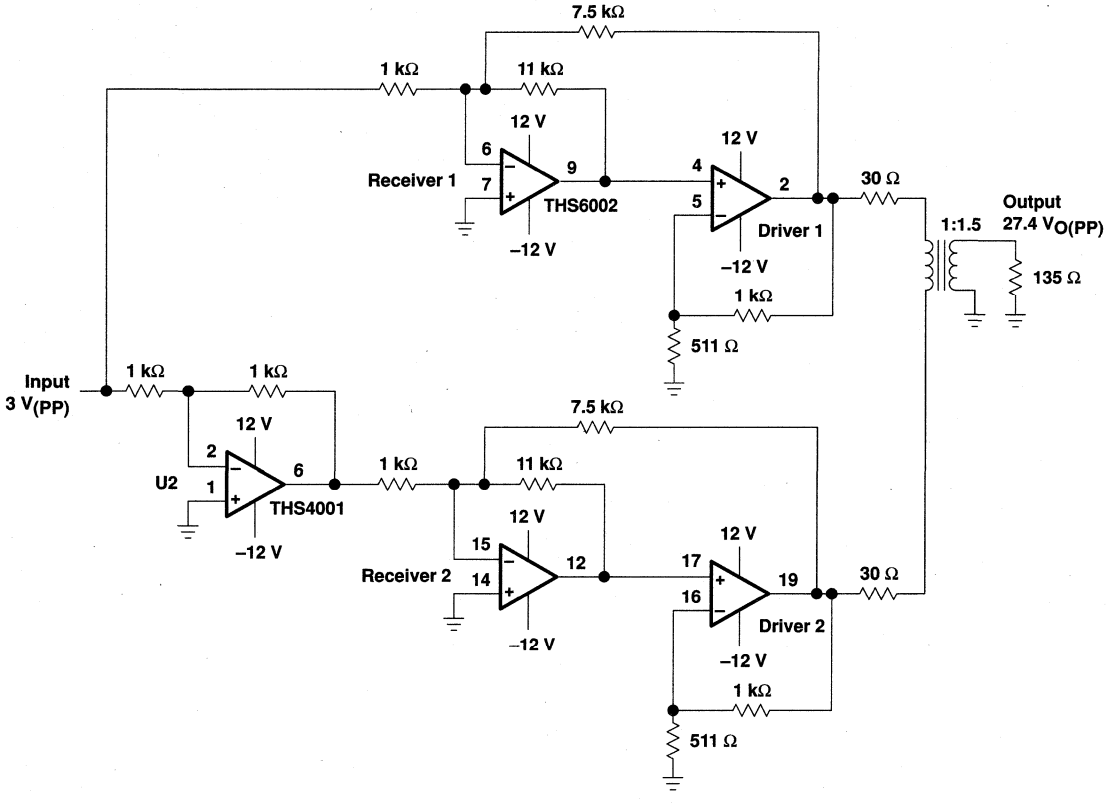


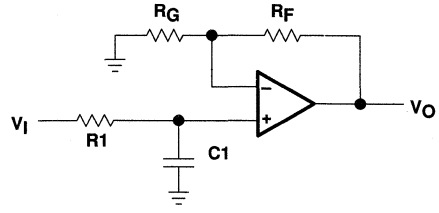
Figure 60. HDSL-2 Line Driver

general configurations

A common error for the first-time CFB user is to create a unity gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration is now commonly referred to as an oscillator. The THS6002, like all CFB amplifiers, **must** have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a very low impedance. This results in an unstable amplifier and should not be considered when using a current-feedback amplifier. Because of this, integrators and simple low-pass filters, which are easily implemented on a VFB amplifier, have to be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see Figure 61).

APPLICATION INFORMATION

general configurations (continued)

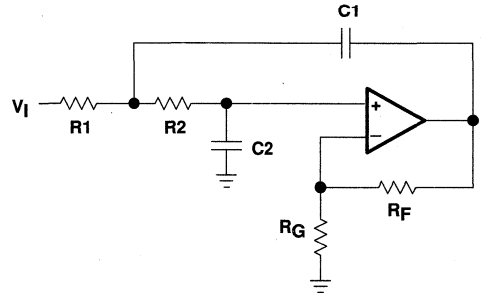


$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

Figure 61. Single-Pole Low-Pass Filter

If a multiple pole filter is required, the use of a Sallen-Key filter can work very well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew-rates and high bandwidths, CFB amplifiers can create very accurate signals and help minimize distortion. An example is shown in Figure 62.



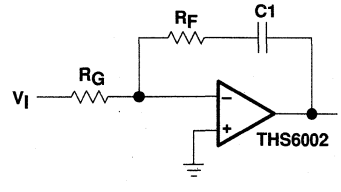
R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 62. 2-Pole Low-Pass Sallen-Key Filter

There are two simple ways to create an integrator with a CFB amplifier. The first one shown in Figure 63 adds a resistor in series with the capacitor. This is acceptable because at high frequencies, the resistor is dominant and the feedback impedance never drops below the resistor value. The second one shown in Figure 64 uses positive feedback to create the integration. Caution is advised because oscillations can occur because of the positive feedback.

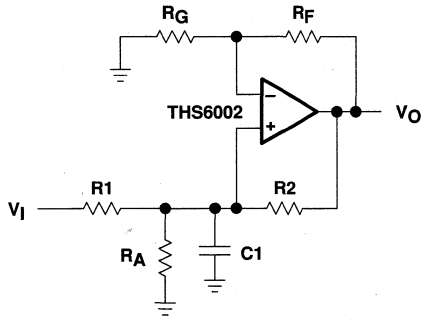


$$\frac{V_O}{V_I} = \left(\frac{R_F}{R_G}\right)\left[\frac{S + \frac{1}{R_F C1}}{S}\right]$$

Figure 63. Inverting CFB Integrator

APPLICATION INFORMATION

general configurations (continued)



For Stable Operation:

$$\frac{R2}{R1 \parallel R_A} \geq \frac{R_F}{R_G}$$

$$V_O \cong V_I \left(\frac{1 + \frac{R_F}{R_G}}{sR1C1} \right)$$

Figure 64. Non-Inverting CFB Integrator

Another good use for the THS6002 driver amplifiers are as very good video distribution amplifiers. One characteristic of distribution amplifiers is the fact that the differential phase (DP) and the differential gain (DG) are compromised as the number of lines increases and the closed-loop gain increases. Be sure to use termination resistors throughout the distribution system to minimize reflections and capacitive loading.

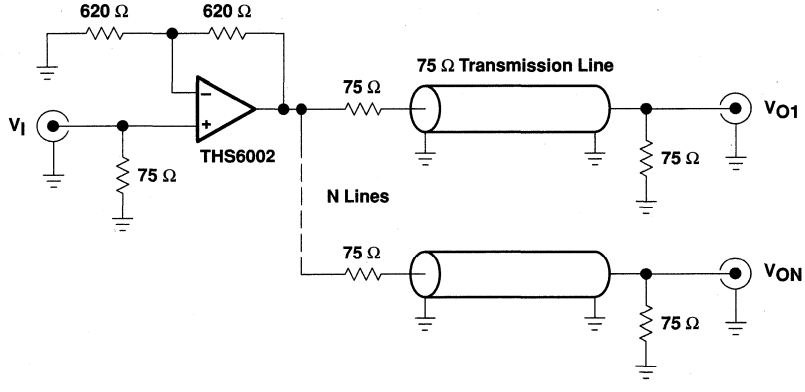


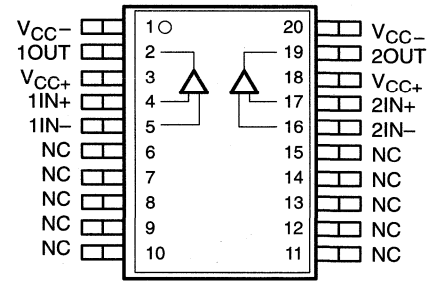
Figure 65. Video Distribution Amplifier Application

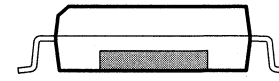
evaluation board

An evaluation board is available for the THS6002 (literature number SLOP117). This board has been configured for proper thermal management of the THS6002. The circuitry has been designed for a typical ADSL application as shown previously in this document. For more detailed information, refer to the *THS6002EVM User's Manual* (literature number SLOU018). To order the evaluation board contact your local TI sales office or distributor.

- **ADSL Differential Line Driver**
- **400 mA Minimum Output Current Into 25-Ω Load**
- **High Speed**
  - **140 MHz Bandwidth (–3dB) With 25-Ω Load**
  - **315 MHz Bandwidth (–3dB) With 100-Ω Load**
  - **1300 V/μs Slew Rate, G = 5**
- **Low Distortion**
  - **–72 dB 3rd Order Harmonic Distortion at f = 1 MHz, 25-Ω Load, and 20 V_{PP}**
- **Independent Power Supplies for Low Crosstalk**
- **Wide Supply Range ±4.5 V to ±16 V**
- **Thermal Shutdown and Short Circuit Protection**
- **Improved Replacement for AD815**
- **Evaluation Module Available**

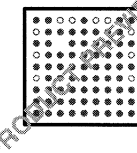
Thermally Enchanced SOIC (DWP)
PowerPAD™ Package
(TOP VIEW)



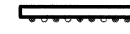


Cross Section View Showing PowerPAD

MicroStar™ Junior (GQE) Package
(TOP VIEW)



(SIDE VIEW)



description

The THS6012 contains two high-speed drivers capable of providing 400 mA output current (min) into a 25 Ω load. These drivers can be configured differentially to drive a 50-Vp-p output signal over low-impedance lines. The drivers are current feedback amplifiers, designed for the high slew rates necessary to support low total harmonic distortion (THD) in xDSL applications. The THS6012 is ideally suited for asymmetrical digital subscriber line (ADSL) applications at the central office, where it supports the high-peak voltage and current requirements of this application.

Separate power supply connections for each driver are provided to minimize crosstalk. The THS6012 is available in the small surface-mount, thermally enhanced 20-pin PowerPAD package.

HIGH-SPEED xDSL LINE DRIVER/RECEIVER FAMILY

DEVICE	DRIVER	RECEIVER	DESCRIPTION
THS6002	•	•	Dual differential line drivers and receivers
THS6012	•		500-mA dual differential line driver
THS6022	•		250-mA dual differential line driver
THS6032	•		Low-power ADSL central office line driver
THS6062		•	Low-noise ADSL receiver
THS7002		•	Low-noise programmable gain ADSL receiver

CAUTION: The THS6012 provides ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

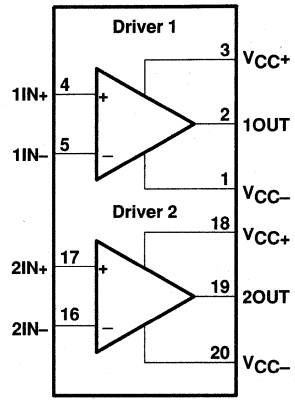
PowerPAD is a trademark of Texas Instruments Incorporated.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE		
	PowerPAD PLASTIC SMALL OUTLINE† (DWP)	MicroStar Junior (GQE)	EVALUATION MODULE
0°C to 70°C	THS6012CDWP	THS6012CGQE	THS6012EVM
–40°C to 85°C	THS6012IDWP	THS6012IGQE	—

† The PWP packages are available taped and reeled. Add an R suffix to the device type (i.e., THS6012CPWPR)

functional block diagram

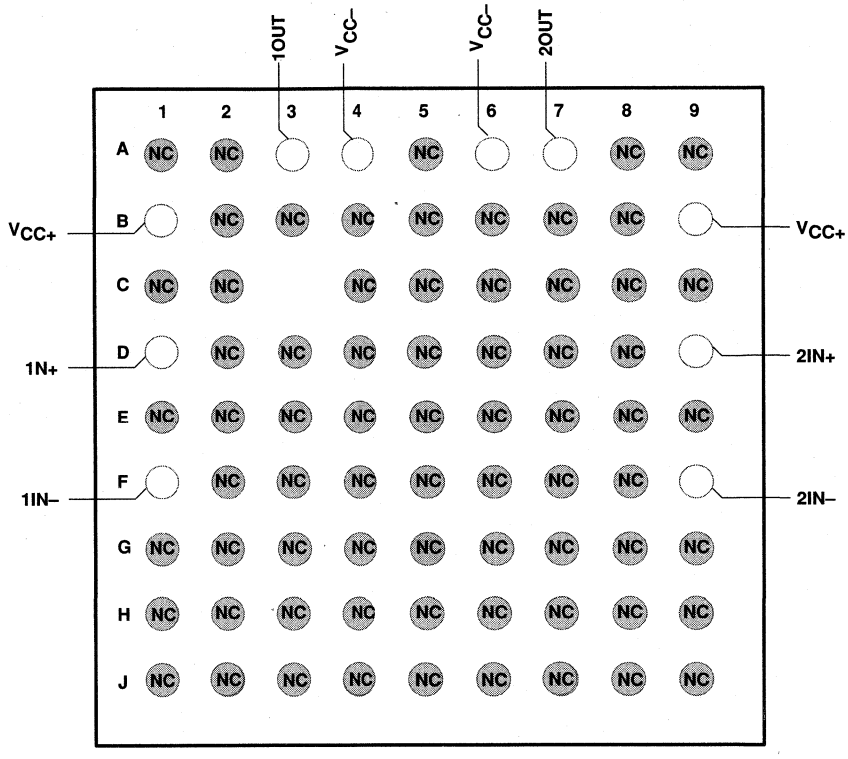


Terminal Functions

TERMINAL		
NAME	DWP PACKAGE TERMINAL NO.	GQE PACKAGE TERMINAL NO.
1OUT	2	A3
1IN–	5	F1
1IN+	4	D1
2OUT	19	A7
2IN–	16	F9
2IN+	17	D9
V_{CC+}	3, 18	B1, B9
$V_{CC–}$	1, 20	A4, A6
NC	6, 7, 8 ,9, 10, 11, 12, 13, 14, 15	NA

pin assignments

MicroStar™ Junior (GQE) Package
(TOP VIEW)



NOTE: Shaded terminals are used for thermal connection to the ground plane.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC+} to V_{CC-} . . . . . 33 V
Input voltage, V_I (driver and receiver) . . . . . $\pm V_{CC}$
Output current, I_O (driver) (see Note 1) . . . . . 800 mA
Differential input voltage, V_{ID} . . . . . 6 V
Continuous total power dissipation at (or below) T_A = 25°C (see Note 1) . . . . . 5.8 W
Operating free air temperature, T_A . . . . . –40°C to 85°C
Storage temperature, T_{stg} . . . . . –65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The THS6012 incorporates a PowerPad on the underside of the chip. This acts as a heatsink and must be connected to a thermal dissipation plane for proper power dissipation. Failure to do so can result in exceeding the maximum junction temperature, which could permanently damage the device. See the *Thermal Information* section of this document for more information about PowerPad technology.

recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, V_{CC+} and V_{CC-}	Split supply	±4.5		±16	V
	Single supply	9		32	
Operating free-air temperature, T_A	C suffix	0		70	°C
	I suffix	–40		85	

electrical characteristics, V_{CC} = ±15 V, R_L = 25 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
BW	Small-signal bandwidth (–3 dB)	V_I = 200 mV, R_F = 680 Ω,	G = 1, R_L = 25 Ω	V_{CC} = ±15 V		140		MHz
		V_I = 200 mV, R_F = 1 kΩ,	G = 1, R_L = 25 Ω	V_{CC} = ±5 V		100		
		V_I = 200 mV, R_F = 620 Ω,	G = 2, R_L = 25 Ω	V_{CC} = ±15 V		120		
		V_I = 200 mV, R_L = 25 Ω,	G = 2, R_F = 820 Ω	V_{CC} = ±5 V		100		
		V_I = 200 mV, R_F = 820 Ω,	G = 1, R_L = 100 Ω	V_{CC} = ±15 V		315		
		V_I = 200 mV, R_F = 560 Ω,	G = 2, R_L = 100 Ω	V_{CC} = ±15 V		265		
	Bandwidth for 0.1 dB flatness	V_I = 200 mV,	G = 1	V_{CC} = ±5 V, R_F = 820 Ω		30		MHz
				V_{CC} = ±15 V, R_F = 680 Ω		40		
	Full power bandwidth (see Note 3)	V_{CC} = ±15 V,	$V_{O(PP)}$ = 20 V			20		MHz
		V_{CC} = ±5 V,	$V_{O(PP)}$ = 4 V			35		
SR	Slew rate	V_{CC} = ±15 V,	V_O = 20 $V_{(PP)}$,	G = 5		1300		V/μs
		V_{CC} = ±5 V,	V_O = 5 $V_{(PP)}$,	G = 2		900		
t_s	Settling time to 0.1%	0 V to 10 V Step,		G = 2		70		ns

noise/distortion performance

PARAMETER			TEST CONDITIONS			MIN	TYP	MAX	UNIT
THD	Total harmonic distortion		V_{CC} = ±15 V, G = 2,	R_F = 680 Ω, f = 1 MHz	$V_{O(PP)}$ = 20 V		–65		dBc
					$V_{O(PP)}$ = 2 V		–79		
			V_{CC} = ±5 V, G = 2,	R_F = 680 Ω, f = 1 MHz	$V_{O(PP)}$ = 2 V		–76		
V_n	Input voltage noise		V_{CC} = ±5 V or ±15 V, G = 2,		f = 10 kHz, Single-ended		1.7		nV/√Hz
I_n	Input noise current	Positive (IN+)	V_{CC} = ±5 V or ±15 V, G = 2		f = 10 kHz,		11.5		pA/√Hz
		Negative (IN–)					16		
A_D	Differential gain error		G = 2, R_L = 150 Ω,	NTSC, 40 IRE Modulation	V_{CC} = ±5 V		0.04%		
					V_{CC} = ±15 V		0.05%		
ϕ_D	Differential phase error		G = 2, R_L = 150 Ω,	NTSC, 40 IRE Modulation	V_{CC} = ±5 V		0.07°		
					V_{CC} = ±15 V		0.08°		
	Crosstalk	Driver to driver	V_I = 200 mV,	f = 1 MHz			–62		dB

electrical characteristics, V_{CC} = ±15 V, R_L = 25 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted) (continued)

dc performance

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
	Open loop transresistance		V_{CC} = ±5 V			1.5		MΩ
			V_{CC} = ±15 V			5		
V_{IO}	Input offset voltage		V_{CC} = ±5 V or ±15 V	T_A = 25°C		2	5	mV
				T_A = full range			7	
	Input offset voltage drift		V_{CC} = ±5 V or ±15 V,	T_A = full range			20	µV/°C
	Differential input offset voltage		V_{CC} = ±5 V or ±15 V	T_A = 25°C		1.5	4	mV
				T_A = full range			5	
I_{IB}	Input bias current	Negative	V_{CC} = ±5 V or ±15 V	T_A = 25°C		3	9	µA
				T_A = full range			12	
		Positive		T_A = 25°C		4	10	µA
				T_A = full range			12	
		Differential		T_A = 25°C		1.5	8	µA
				T_A = full range			11	
	Differential input offset voltage drift		V_{CC} = ±5 V or ±15 V,	T_A = full range			10	µV/°C

input characteristics

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{ICR}	Common-mode input voltage range	V_{CC} = ±5 V		±3.6	±3.7		V
		V_{CC} = ±15 V		±13.4	±13.5		
CMRR	Common-mode rejection ratio	V_{CC} = ±5 V or ±15 V,	T_A = full range	62	70		dB
	Differential common-mode rejection ratio				100		
R_I	Input resistance				300		kΩ
C_I	Differential input capacitance				1.4		pF

output characteristics

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_O	Output voltage swing	Single ended	R_L = 25 Ω	V_{CC} = ±5 V	3 to −2.8	3.2 to −3		V
				V_{CC} = ±15 V	11.8 to −11.5	12.5 to −12.2		
		Differential	R_L = 50 Ω	V_{CC} = ±5 V	6 to −5.6	6.4 to −6		V
				V_{CC} = ±15 V	23.6 to −23	25 to −24.4		
I_O	Output current (see Note 2)		V_{CC} = ±5 V,	R_L = 5 Ω		500		mA
			V_{CC} = ±15 V,	R_L = 25 Ω	400	500		
I_{OS}	Short-circuit output current (see Note 2)					800		mA
R_O	Output resistance		Open loop			13		Ω

NOTE 2: A heat sink is required to keep the junction temperature below absolute maximum when an output is heavily loaded or shorted. See absolute maximum ratings and *Thermal Information* section.

electrical characteristics, V_{CC} = ±15 V, R_L = 25 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted)

power supply

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{CC}	Power supply operating range	Split supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Quiescent current (each driver)	V_{CC} = ±5 V	T_A = full range			12	mA
		V_{CC} = ±15 V	T_A = 25°C		11.5	13	
			T_A = full range			15	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V	T_A = 25°C	−68	−74		dB
			T_A = full range	−65			
		V_{CC} = ±15 V	T_A = 25°C	−64	−72		dB
			T_A = full range	−62			

† Full range is 0°C to 70°C for the THS6012C and −40°C to 85°C for the THS6012I.

PARAMETER MEASUREMENT INFORMATION

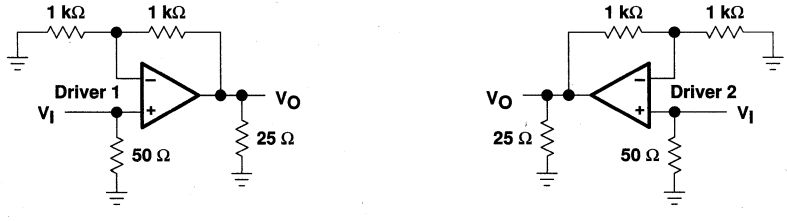


Figure 1. Input-to-Output Crosstalk Test Circuit

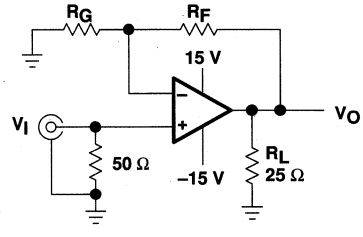


Figure 2. Test Circuit, Gain = 1 + (R_F/R_G)

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$V_{O(PP)}$	Peak-to-peak output voltage	vs Supply voltage	3
		vs Load resistance	4
V_{IO}	Input offset voltage	vs Free-air temperature	5
I_{IB}	Input bias current	vs Free-air temperature	6
CMRR	Common-mode rejection ratio	vs Free-air temperature	7
	Input-to-output crosstalk	vs Frequency	8
PSRR	Power supply rejection ratio	vs Free-air temperature	9
	Closed-loop output impedance	vs Frequency	10
I_{CC}	Supply current	vs Supply voltage	11
		vs Free-air temperature	12
SR	Slew rate	vs Output step	13, 14
V_n	Input voltage noise	vs Frequency	15
I_n	Input current noise	vs Frequency	
	Normalized frequency response	vs Frequency	16, 17
	Output amplitude	vs Frequency	18–21
	Normalized output response	vs Frequency	22–25
	Small and large frequency response		26, 27
	Single-ended harmonic distortion	vs Frequency	28, 29
		vs Output voltage	30, 31
	Differential gain	DC input offset voltage	32, 33
		Number of 150-Ω loads	34, 35
	Differential phase	DC input offset voltage	32, 33
		Number of 150-Ω loads	34, 35
	Output step response		36–38

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

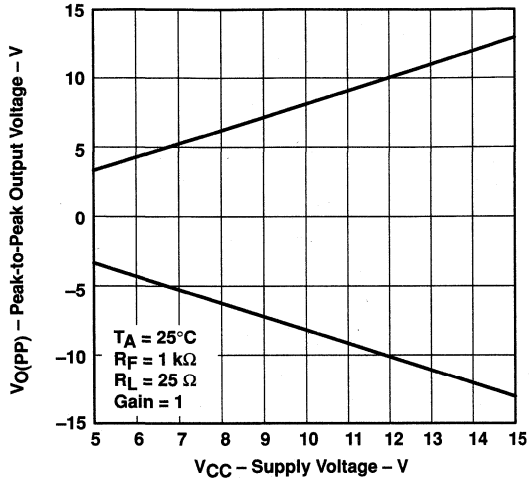


Figure 3

PEAK-TO-PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE

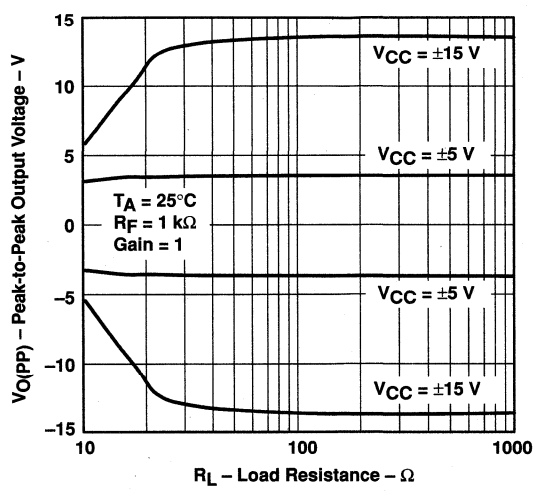


Figure 4

INPUT OFFSET VOLTAGE
vs
FREE-AIR TEMPERATURE

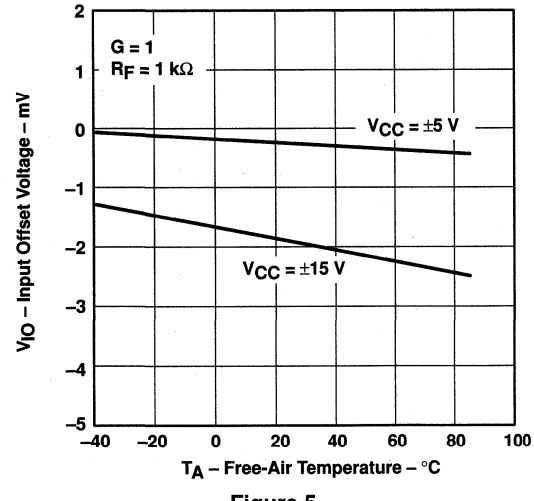


Figure 5

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

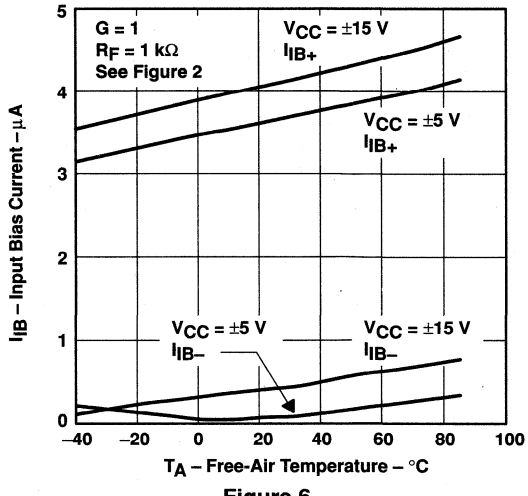


Figure 6

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

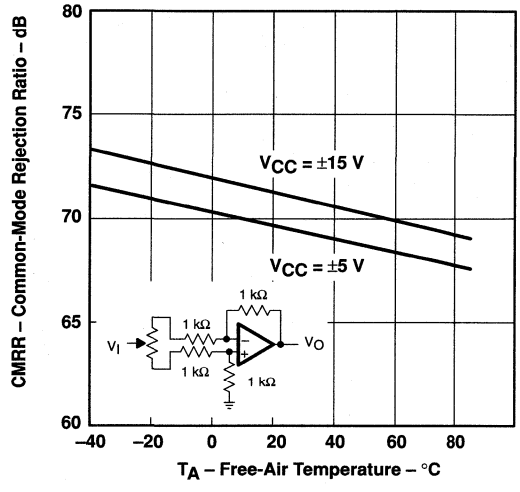


Figure 7

INPUT–TO–OUTPUT CROSSTALK vs FREQUENCY

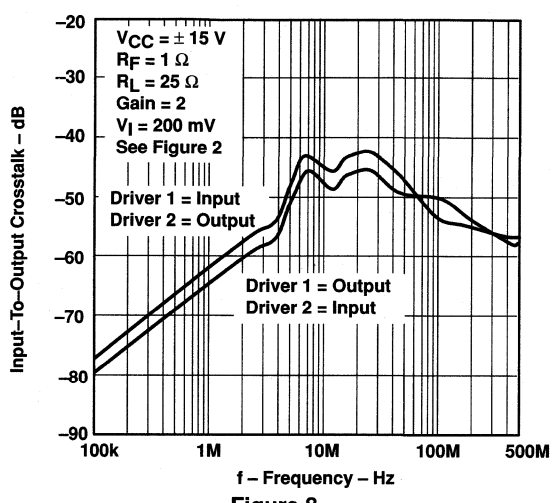


Figure 8

POWER SUPPLY REJECTION RATIO vs FREE-AIR TEMPERATURE

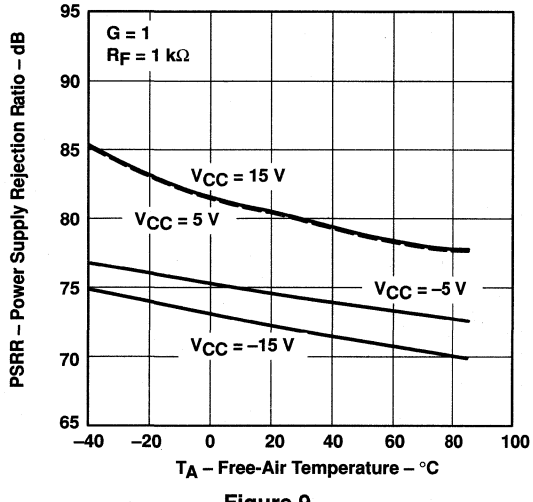


Figure 9

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

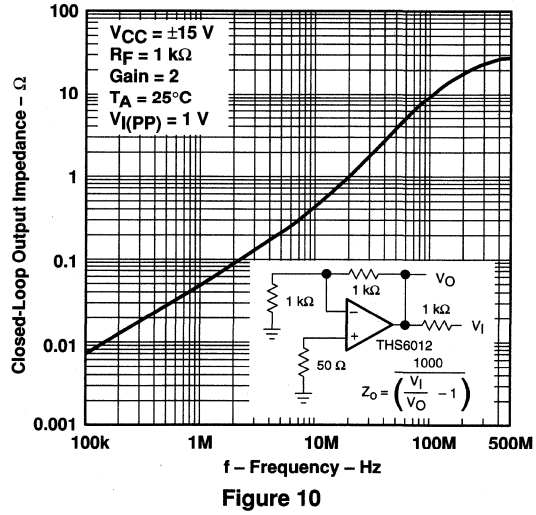


Figure 10

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

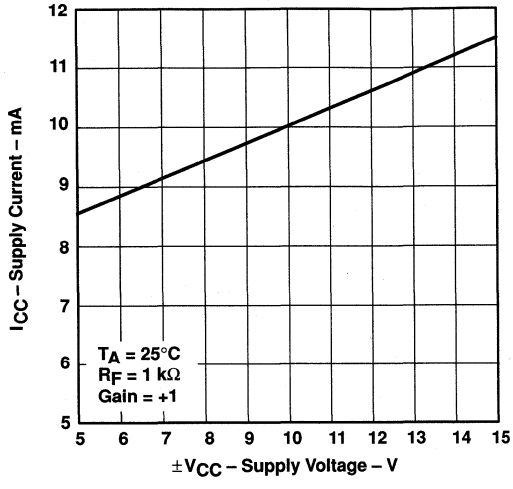


Figure 11

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

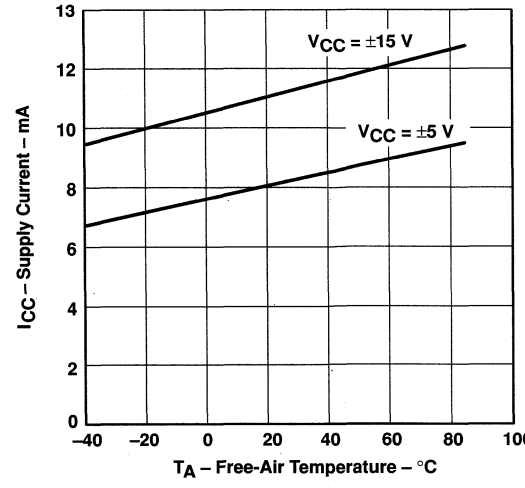


Figure 12

SLEW RATE
vs
OUTPUT STEP

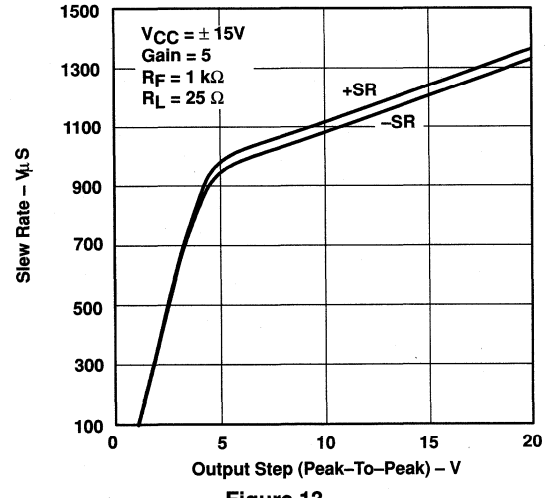


Figure 13

SLEW RATE
vs
OUTPUT STEP

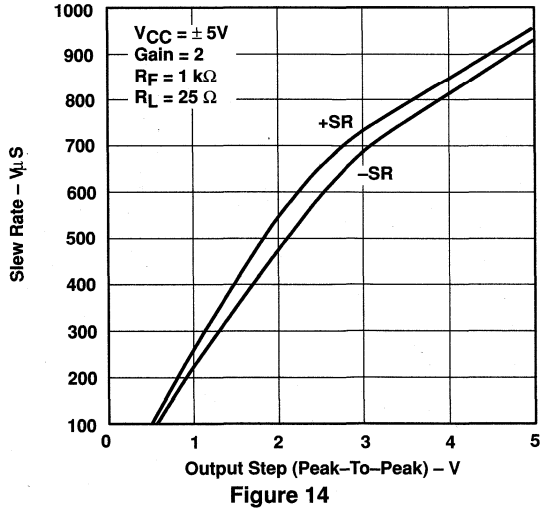


Figure 14

TYPICAL CHARACTERISTICS

INPUT VOLTAGE AND CURRENT NOISE vs FREQUENCY

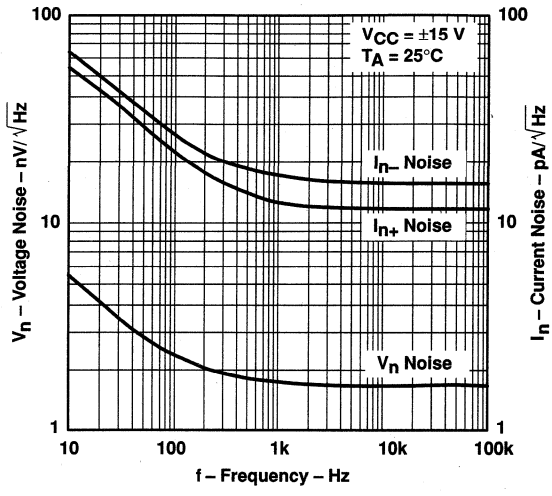


Figure 15

NORMALIZED FREQUENCY RESPONSE vs FREQUENCY

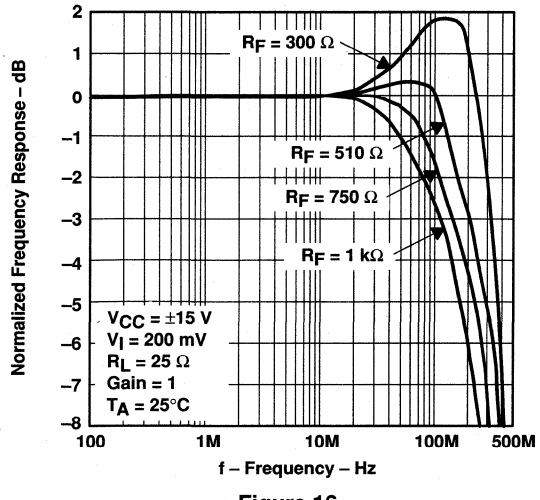


Figure 16

NORMALIZED FREQUENCY RESPONSE vs FREQUENCY

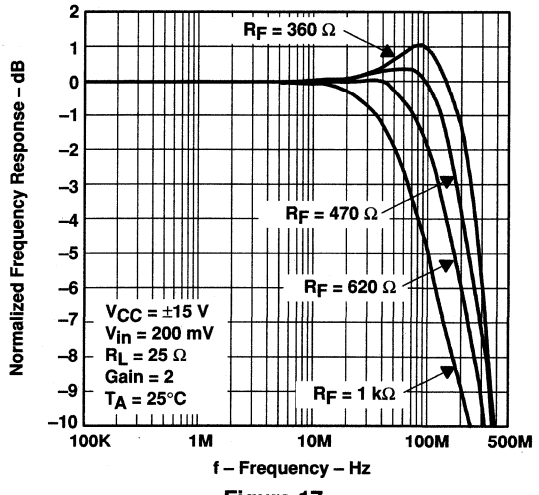


Figure 17

TYPICAL CHARACTERISTICS

OUTPUT AMPLITUDE
vs
FREQUENCY

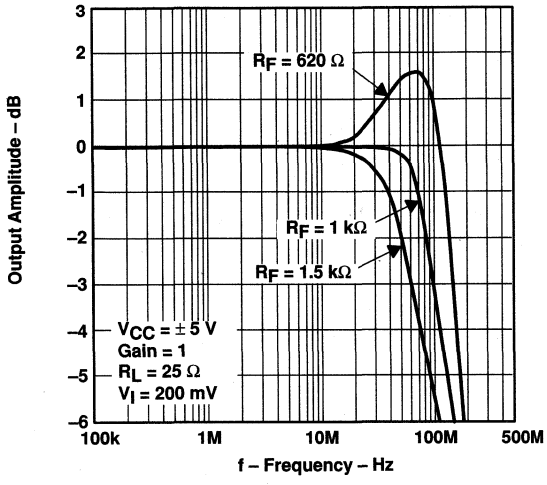


Figure 18

OUTPUT AMPLITUDE
vs
FREQUENCY

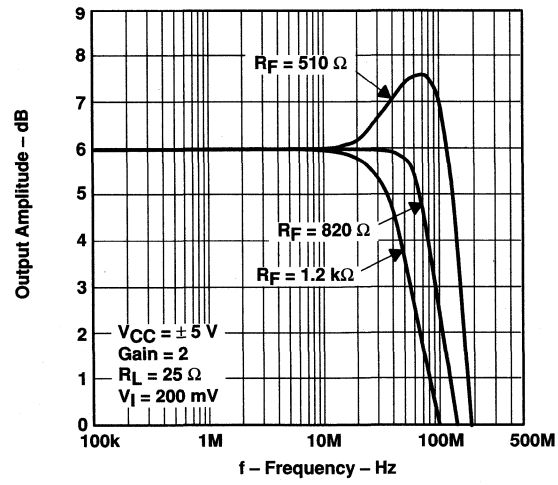


Figure 19

OUTPUT AMPLITUDE
vs
FREQUENCY

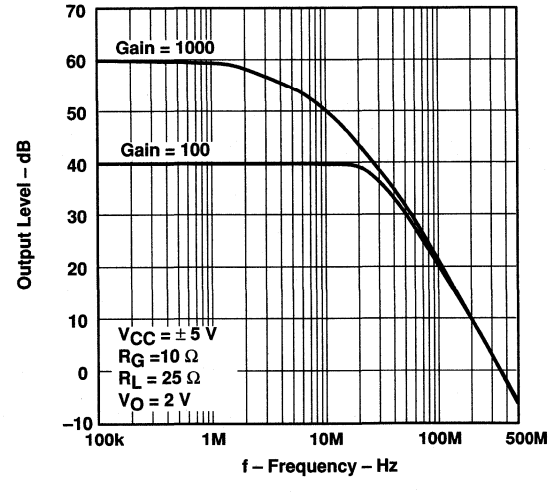


Figure 20

OUTPUT AMPLITUDE
vs
FREQUENCY

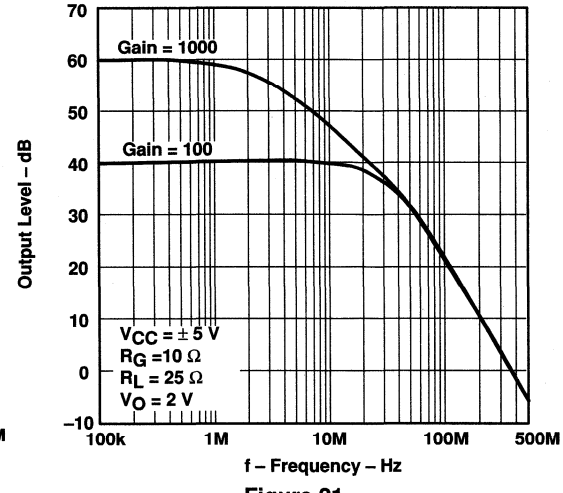


Figure 21

TYPICAL CHARACTERISTICS

NORMALIZED OUTPUT RESPONSE
vs
FREQUENCY

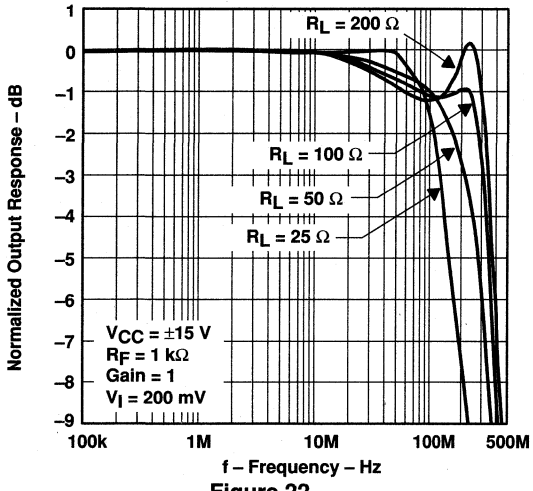


Figure 22

NORMALIZED OUTPUT RESPONSE
vs
FREQUENCY

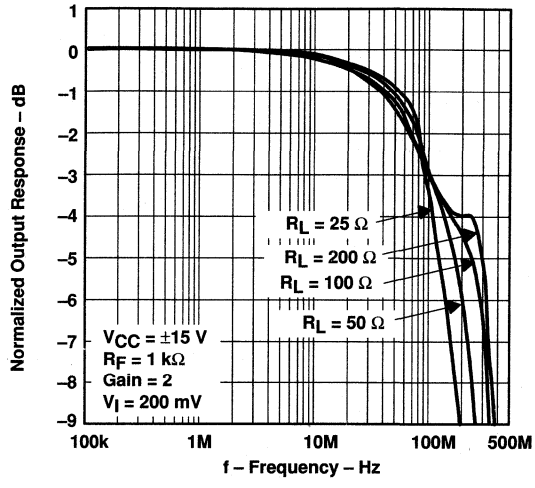


Figure 23

NORMALIZED OUTPUT RESPONSE
vs
FREQUENCY

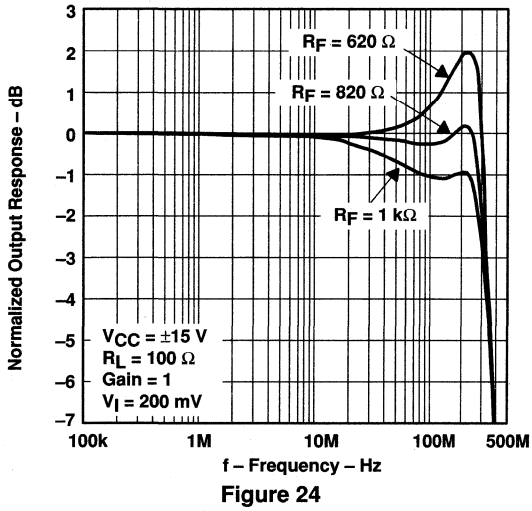


Figure 24

NORMALIZED OUTPUT RESPONSE
vs
FREQUENCY

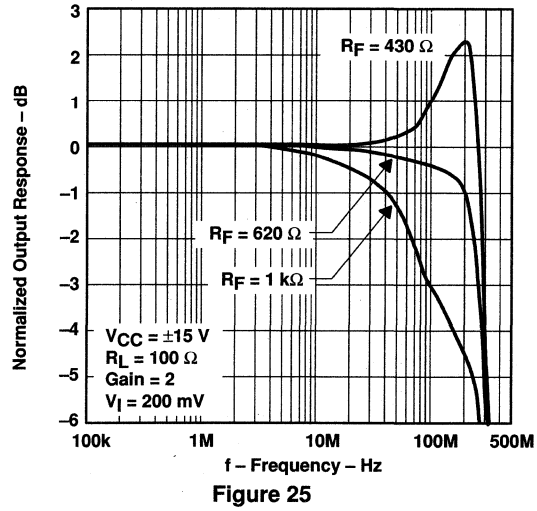


Figure 25

TYPICAL CHARACTERISTICS

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

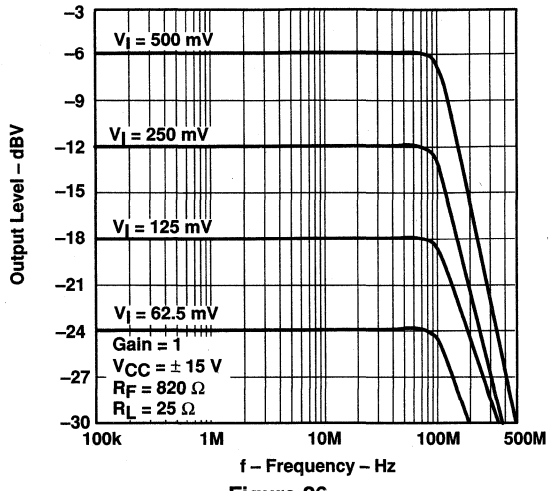


Figure 26

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

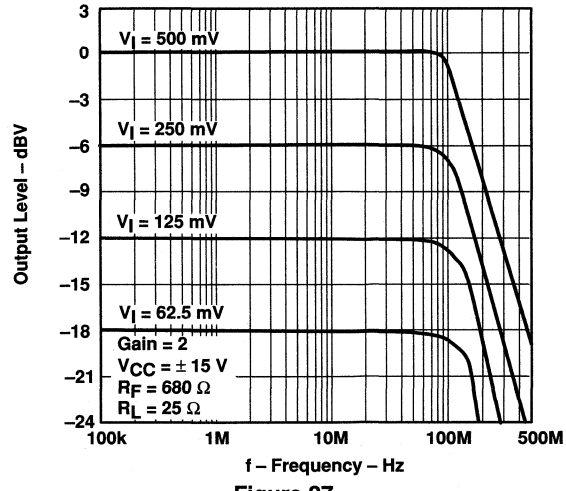


Figure 27

SINGLE–ENDED HARMONIC DISTORTION vs FREQUENCY

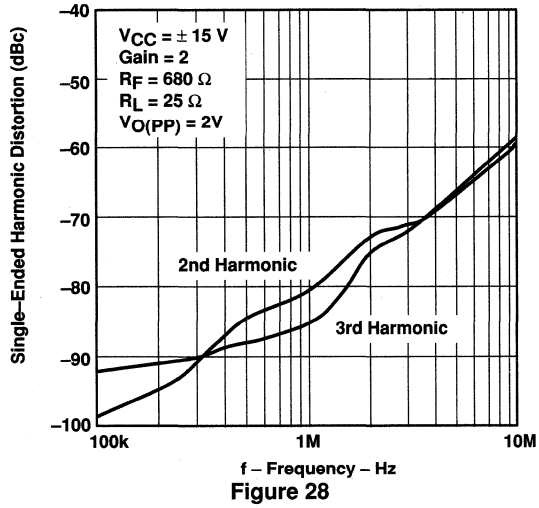


Figure 28

SINGLE–ENDED HARMONIC DISTORTION vs FREQUENCY

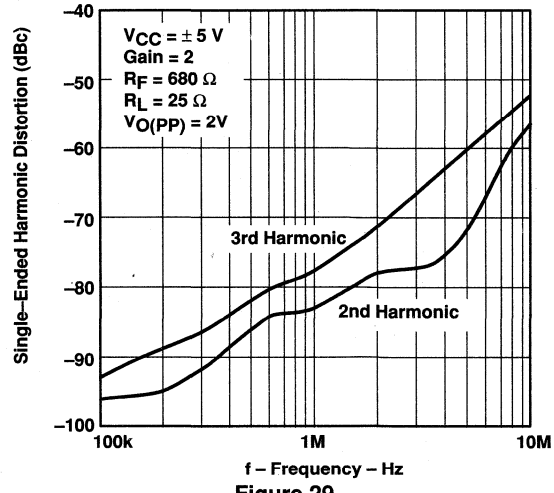


Figure 29

TYPICAL CHARACTERISTICS

SINGLE–ENDED HARMONIC DISTORTION vs OUTPUT VOLTAGE

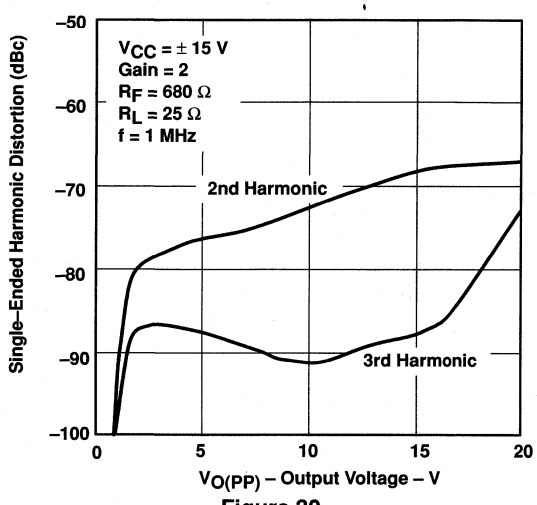


Figure 30

SINGLE–ENDED HARMONIC DISTORTION vs OUTPUT VOLTAGE

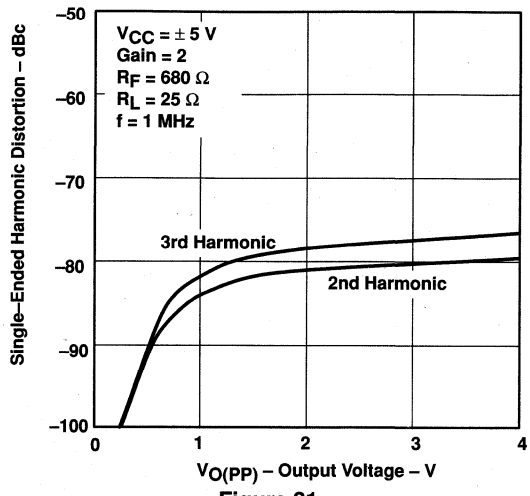


Figure 31

DIFFERENTIAL GAIN AND PHASE vs DC INPUT OFFSET VOLTAGE

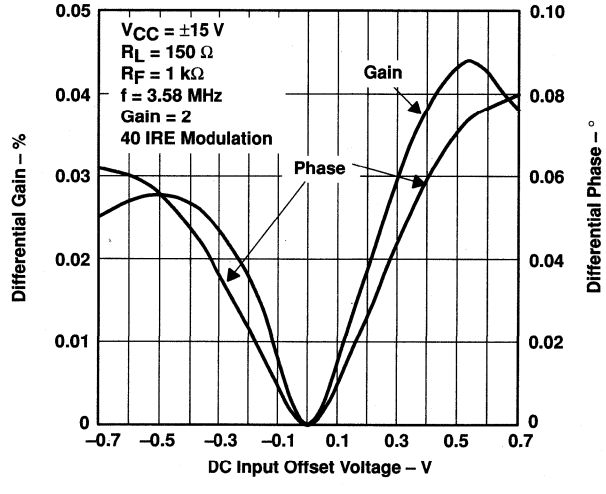


Figure 32

TYPICAL CHARACTERISTICS

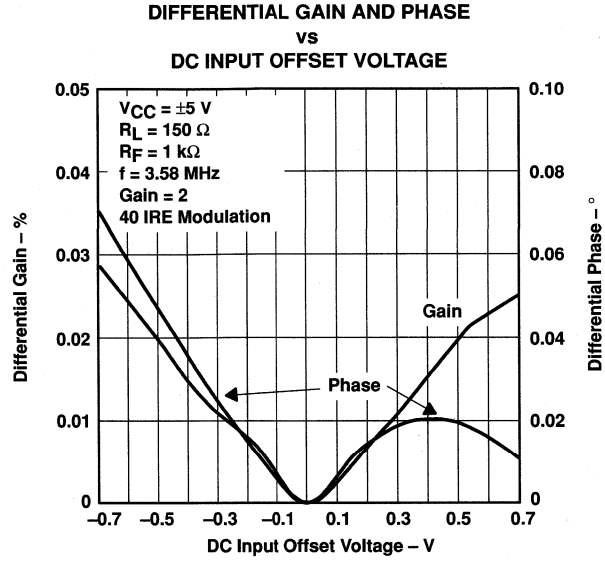


Figure 33

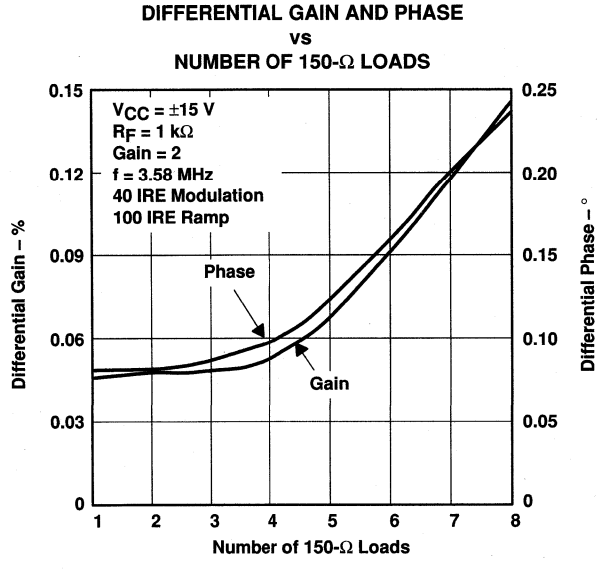


Figure 34

TYPICAL CHARACTERISTICS

DIFFERENTIAL GAIN AND PHASE vs NUMBER OF 150-Ω LOADS

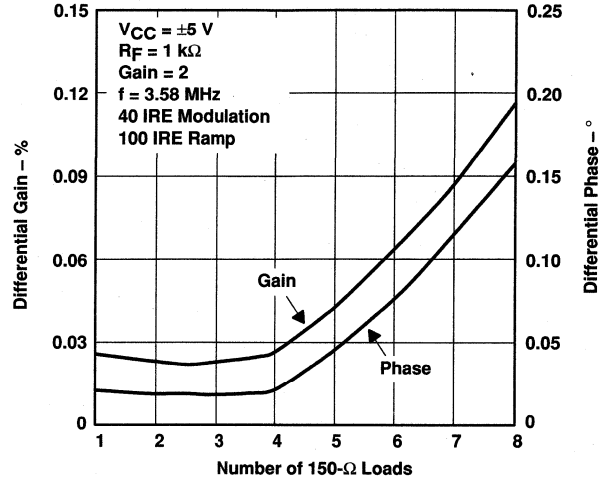


Figure 35

400-mV STEP RESPONSE

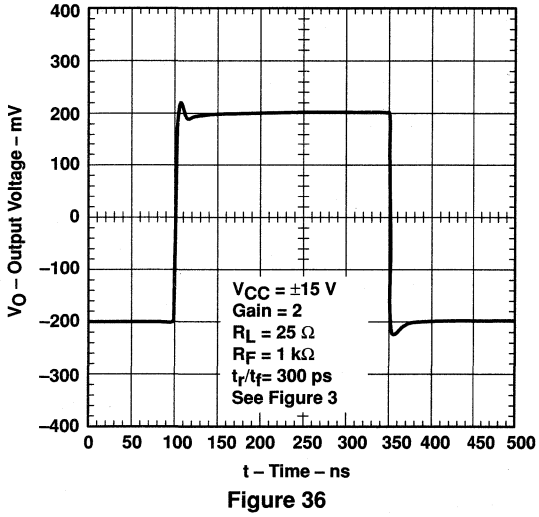


Figure 36

10-V STEP RESPONSE

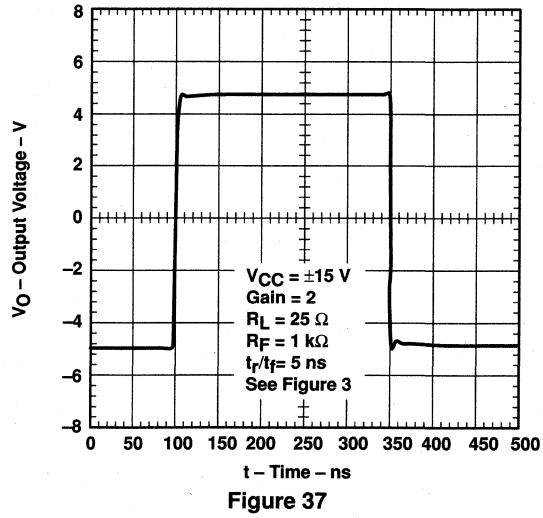


Figure 37

TYPICAL CHARACTERISTICS

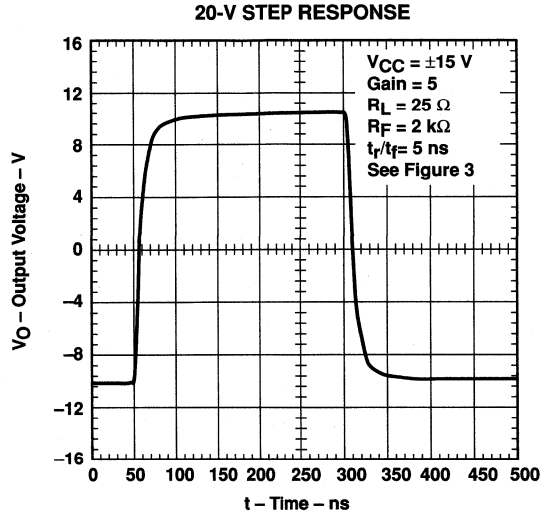


Figure 38

APPLICATION INFORMATION

The THS6012 contains two independent operational amplifiers. These amplifiers are current feedback topology amplifiers made for high-speed operation. They have been specifically designed to deliver the full power requirements of ADSL and therefore can deliver output currents of at least 400 mA at full output voltage.

The THS6012 is fabricated using Texas Instruments 30-V complementary bipolar process, HVBiCOM. This process provides excellent isolation and high slew rates that result in the device's excellent crosstalk and extremely low distortion.

independent power supplies

Each amplifier of the THS6012 has its own power supply pins. This was specifically done to solve a problem that often occurs when multiple devices in the same package share common power pins. This problem is crosstalk between the individual devices caused by currents flowing in common connections. Whenever the current required by one device flows through a common connection shared with another device, this current, in conjunction with the impedance in the shared line, produces an unwanted voltage on the power supply. Proper power supply decoupling and good device power supply rejection helps to reduce this unwanted signal. What is left is crosstalk.

However, with independent power supply pins for each device, the effects of crosstalk through common impedance in the power supplies is more easily managed. This is because it is much easier to achieve low common impedance on the PCB with copper etch than it is to achieve low impedance within the package with either bond wires or metal traces on silicon.

APPLICATION INFORMATION

power supply restrictions

Although the THS6012 is specified for operation from power supplies of ±5 V to ±15 V (or singled-ended power supply operation from 10 V to 30 V), and each amplifier has its own power supply pins, several precautions must be taken to assure proper operation.

1. The power supplies for each amplifier must be the same value. For example, if the driver 1 uses ±15 volts, then the driver 2 must also use ±15 volts. Using ±15 volts for one amplifier and ±5 volts for another amplifier is not allowed.
2. To save power by powering down one of the amplifiers in the package, the following rules must be followed.
   - The amplifier designated driver 1 must always receive power. This is because the internal startup circuitry uses the power from the driver 1 device.
   - The $-V_{CC}$ pins from both drivers must always be at the same potential.
   - Driver 2 is powered down by simply opening the $+V_{CC}$ connection.

The THS6012 incorporates a standard Class A-B output stage. This means that some of the quiescent current is directed to the load as the load current increases. So under heavy load conditions, accurate power dissipation calculations are best achieved through actual measurements. For small loads, however, internal power dissipation for each amplifier in the THS6012 can be approximated by the following formula:

$$P_D \cong \left(2\ V_{CC}\ I_{CC}\right) + \left(V_{CC} - V_O\right) \times \left(\frac{V_O}{R_L}\right)$$

Where:

P_D = Power dissipation for one amplifier
V_{CC} = Split supply voltage
I_{CC} = Supply current for that particular amplifier
V_O = Output voltage of amplifier
R_L = Load resistance

To find the total THS6012 power dissipation, we simply sum up both amplifier power dissipation results. Generally, the worst case power dissipation occurs when the output voltage is one-half the V_{CC} voltage. One last note, which is often overlooked: the feedback resistor (R_F) is also a load to the output of the amplifier and should be taken into account for low value feedback resistors.

device protection features

The THS6012 has two built-in protection features that protect the device against improper operation. The first protection mechanism is output current limiting. Should the output become shorted to ground the output current is automatically limited to the value given in the data sheet. While this protects the output against excessive current, the device internal power dissipation increases due to the high current and large voltage drop across the output transistors. Continuous output shorts are not recommended and could damage the device. Additionally, connection of the amplifier output to one of the supply rails ($\pm V_{CC}$) can cause failure of the device and is not recommended.

The second built-in protection feature is thermal shutdown. Should the internal junction temperature rise above approximately 180°C, the device automatically shuts down. Such a condition could exist with improper heat sinking or if the output is shorted to ground. When the abnormal condition is fixed, the internal thermal shutdown circuit automatically turns the device back on.

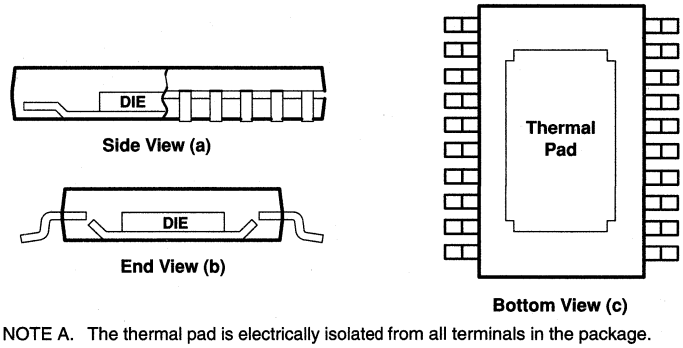
APPLICATION INFORMATION

thermal information

The THS6012 is packaged in a thermally-enhanced DWP package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 39(a) and Figure 39(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 39(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device. This is discussed in more detail in the *PCB design considerations* section of this document.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.



NOTE A. The thermal pad is electrically isolated from all terminals in the package.

Figure 39. Views of Thermally Enhanced DWP Package

APPLICATION INFORMATION

recommended feedback and gain resistor values

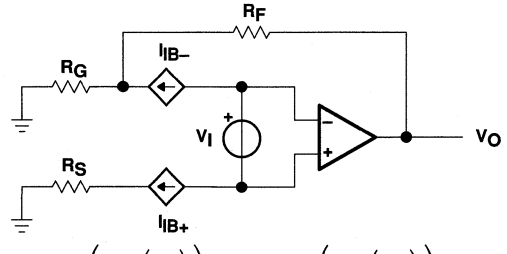
As with all current feedback amplifiers, the bandwidth of the THS6012 is an inversely proportional function of the value of the feedback resistor. This can be seen from Figures 17 – 20. The recommended resistors with a ±15 V power supply for the optimum frequency response with a 25-Ω load system are 680-Ω for a gain = 1 and 620-Ω for a gain = 2 or –1. Additionally, using a ±5 V power supply, it is recommended that a 1-kΩ feedback resistor be used for a gain of 1 and a 820-Ω feedback resistor be used for a gain of 2 or –1. These should be used as a starting point and once optimum values are found, 1% tolerance resistors should be used to maintain frequency response characteristics. Because there is a finite amount of output resistance of the operational amplifier, load resistance can play a major part in frequency response. This is especially true with these drivers, which tend to drive low-impedance loads. This can be seen in Figure 11, Figure 23, and Figure 24. As the load resistance increases, the output resistance of the amplifier becomes less dominant at high frequencies. To compensate for this, the feedback resistor should change. For 100-Ω loads, it is recommended that the feedback resistor be changed to 820 Ω for a gain of 1 and 560 Ω for a gain of 2 or –1. Although, for most applications, a feedback resistor value of 1 kΩ is recommended, which is a good compromise between bandwidth and phase margin that yields a very stable amplifier.

Consistent with current feedback amplifiers, increasing the gain is best accomplished by changing the gain resistor, not the feedback resistor. This is because the bandwidth of the amplifier is dominated by the feedback resistor value and internal dominant-pole capacitor. The ability to control the amplifier gain independently of the bandwidth constitutes a major advantage of current feedback amplifiers over conventional voltage feedback amplifiers. Therefore, once a frequency response is found suitable to a particular application, adjust the value of the gain resistor to increase or decrease the overall amplifier gain.

Finally, it is important to realize the effects of the feedback resistance on distortion. Increasing the resistance decreases the loop gain and increases the distortion. It is also important to know that decreasing load impedance increases total harmonic distortion (THD). Typically, the third order harmonic distortion increases more than the second order harmonic distortion.

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

Figure 40. Output Offset Voltage Model

APPLICATION INFORMATION

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true for the amplifying small signals. The noise model for current feedback amplifiers (CFB) is the same as voltage feedback amplifiers (VFB). The only difference between the two is that the CFB amplifiers generally specify different current noise parameters for each input while VFB amplifiers usually only specify one noise current parameter. The noise model is shown in Figure 42. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = Noninverting current noise (pA/$\sqrt{Hz}$)
- IN– = Inverting current noise (pA/$\sqrt{Hz}$)
- e_{Rx} = Thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR_x)

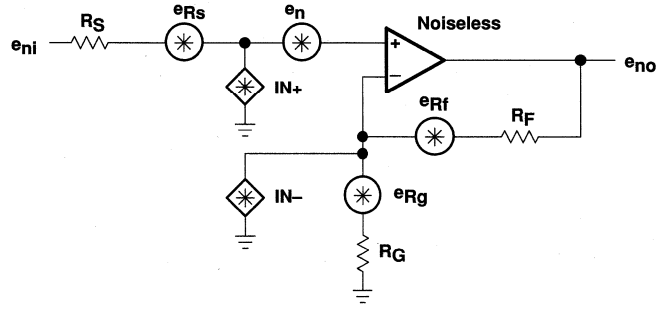


Figure 41. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + (IN+ \times R_S)^2 + (IN- \times (R_F \parallel R_G))^2 + 4\ kTR_S + 4\ kT(R_F \parallel R_G)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\ A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)}$$

APPLICATION INFORMATION

noise calculations and noise figure (continued)

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^2}{(e_{Rs})^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[(e_n)^2 + (IN + \times R_S)^2\right]}{4\ kTR_S}\right]$$

Figure 42 shows the noise figure graph for the THS6012.

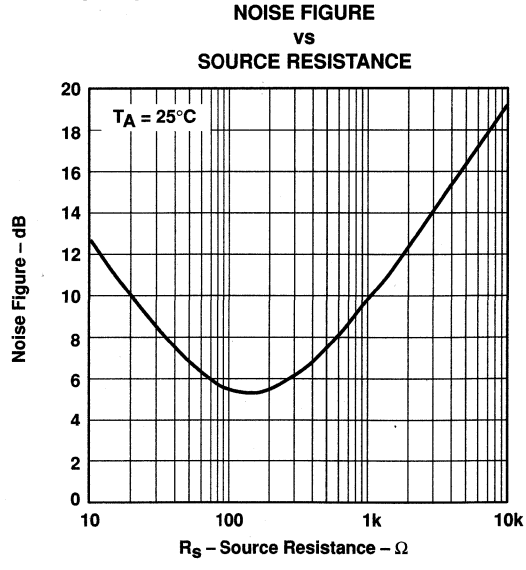


Figure 42. Noise Figure vs Source Resistance

APPLICATION INFORMATION

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS6012 has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 44. A minimum value of 10 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

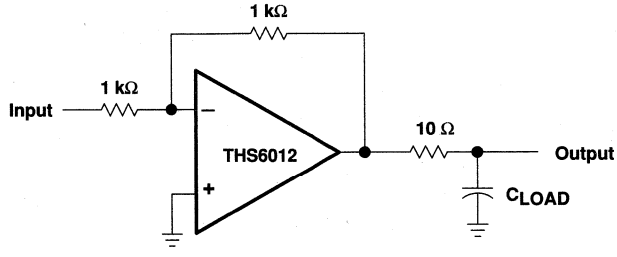


Figure 43. Driving a Capacitive Load

PCB design considerations

Proper PCB design techniques in two areas are important to assure proper operation of the THS6012. These areas are high-speed layout techniques and thermal-management techniques. Because the THS6012 is a high-speed part, the following guidelines are recommended.

- Ground plane – It is essential that a ground plane be used on the board to provide all components with a low inductive ground connection. Although a ground connection directly to a terminal of the THS6012 is not necessarily required, it is recommended that the thermal pad of the package be tied to ground. This serves two functions. It provides a low inductive ground to the device substrate to minimize internal crosstalk and it provides the path for heat removal.
- Input stray capacitance – To minimize potential problems with amplifier oscillation, the capacitance at the inverting input of the amplifiers must be kept to a minimum. To do this, PCB trace runs to the inverting input must be as short as possible, the ground plane must be removed under any etch runs connected to the inverting input, and external components should be placed as close as possible to the inverting input. This is especially true in the noninverting configuration. An example of this can be seen in Figure 44, which shows what happens when 1.8 pF is added to the inverting input terminal in the noninverting configuration. The bandwidth increases dramatically at the expense of peaking. This is because some of the error current is flowing through the stray capacitor instead of the inverting node of the amplifier. Although, in the inverting mode, stray capacitance at the inverting input has little effect. This is because the inverting node is at a *virtual ground* and the voltage does not fluctuate nearly as much as in the noninverting configuration.

APPLICATION INFORMATION

PCB design considerations (continued)

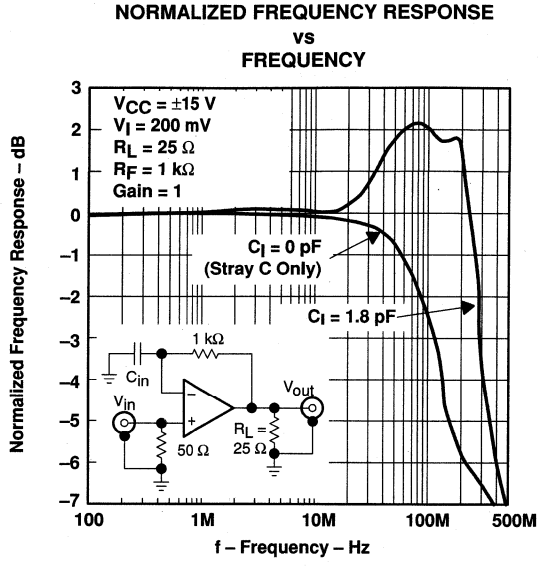


Figure 44. Driver Normalized Frequency Response vs Frequency

- Proper power supply decoupling – Use a minimum of a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting etch makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminal and the ceramic capacitors.

Because of its power dissipation, proper thermal management of the THS6012 is required. Although there are many ways to properly heatsink this device, the following steps illustrate one recommended approach for a multilayer PCB with an internal ground plane.

1. Prepare the PCB with a top side etch pattern as shown in Figure 45. There should be etch for the leads as well as etch for the thermal pad.
2. Place 18 holes in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
3. It is recommended, but not required, to place six more holes under the package, but outside the thermal pad area. These holes are 25 mils in diameter. They may be larger because they are not in the area to be soldered so that wicking is not a problem.
4. Connect all 24 holes, the 18 within the thermal pad area and the 6 outside the pad area, to the internal ground plane.

APPLICATION INFORMATION

PCB design considerations (continued)

5. When connecting these holes to the ground plane, do **not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS6012 package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated through hole.
6. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area with its five holes. The four larger holes outside the thermal pad area, but still under the package, should be covered with solder mask.
7. Apply solder paste to the exposed thermal pad area and all of the operational amplifier terminals.
8. With these preparatory steps in place, the THS6012 is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

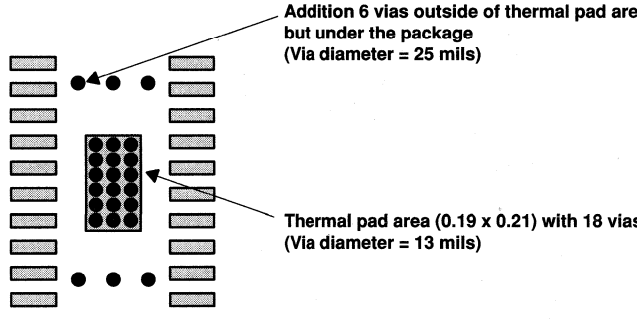


Figure 45. PowerPAD PCB Etch and Via Pattern

The actual thermal performance achieved with the THS6012 in its PowerPAD package depends on the application. In the previous example, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA}, is about 21.5°C/W. For a given θ_{JA}, the maximum power dissipation is shown in Figure 46 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS6012 (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case (0.37°C/W)
θ_{CA} = Thermal coefficient from case to ambient

APPLICATION INFORMATION

PCB design considerations (continued)

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

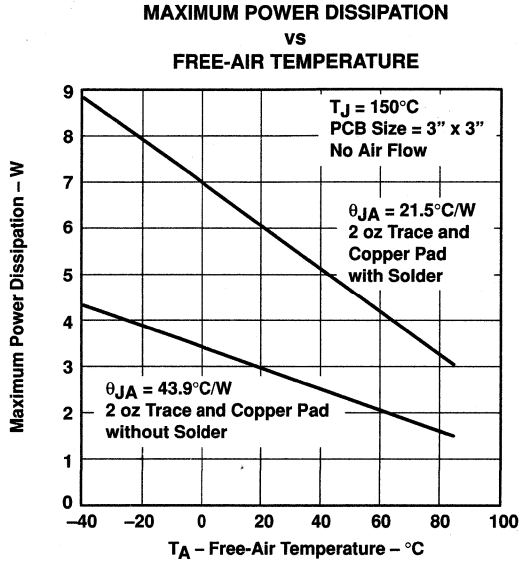


Figure 46. Maximum Power Dissipation vs Free-Air Temperature

APPLICATION INFORMATION

ADSL

The THS6012 was primarily designed as a line driver and line receiver for ADSL (asymmetrical digital subscriber line). The driver output stage has been sized to provide full ADSL power levels of 20 dBm onto the telephone lines. Although actual driver output peak voltages and currents vary with each particular ADSL application, the THS6012 is specified for a minimum full output current of 400 mA at its full output voltage of approximately 12 V. This performance meets the demanding needs of ADSL at the central office end of the telephone line. A typical ADSL schematic is shown in Figure 47.

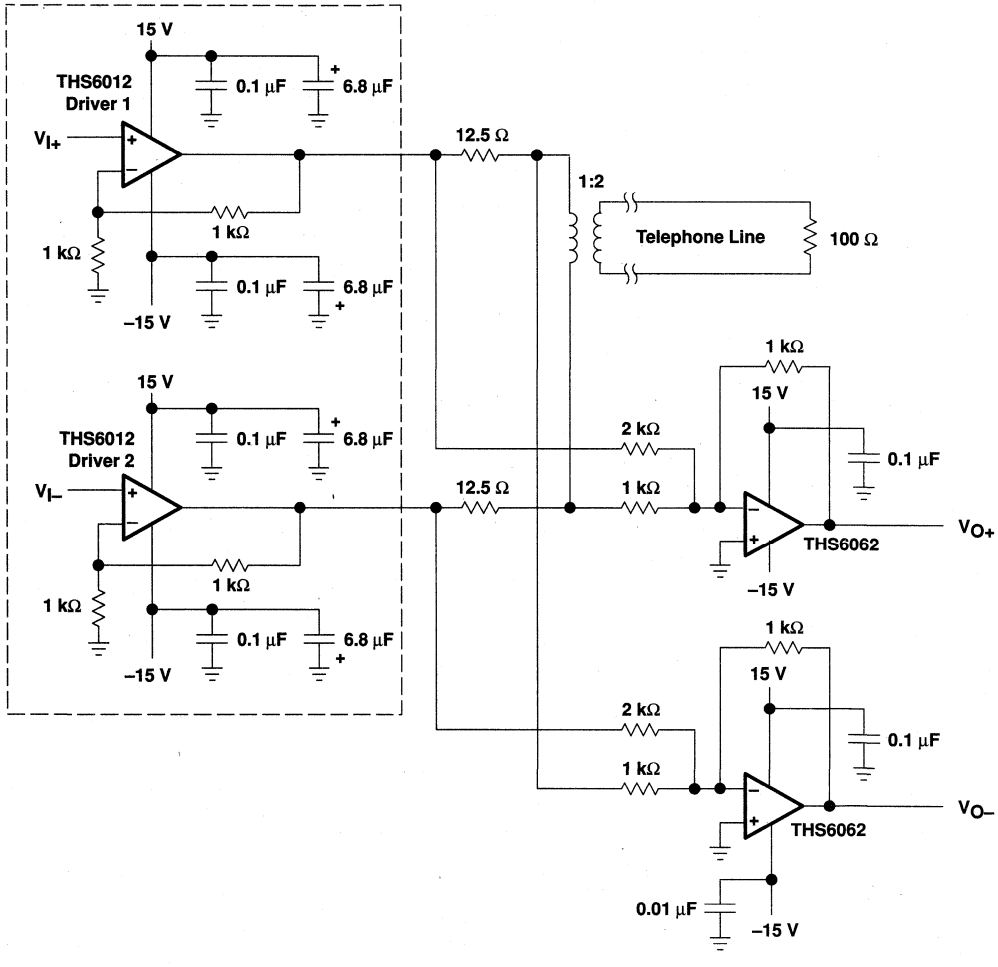


Figure 47. THS6012 ADSL Application

APPLICATION INFORMATION

ADSL (continued)

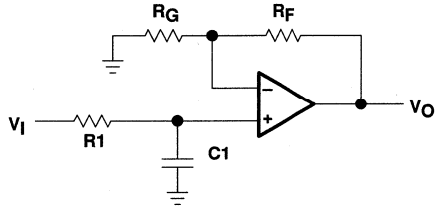
The ADSL transmit band consists of 255 separate carrier frequencies each with its own modulation and amplitude level. With such an implementation, it is imperative that signals put onto the telephone line have as low a distortion as possible. This is because any distortion either interferes directly with other ADSL carrier frequencies or it creates intermodulation products that interfere with ADSL carrier frequencies.

The THS6012 has been specifically designed for ultra low distortion by careful circuit implementation and by taking advantage of the superb characteristics of the complementary bipolar process. Driver single-ended distortion measurements are shown in Figures 29 – 32. It is commonly known that in the differential driver configuration, the second order harmonics tend to cancel out. Thus, the dominant total harmonic distortion (THD) will be primarily due to the third order harmonics. For these tests the load was 25 Ω. Additionally, distortion should be reduced as the feedback resistance drops. This is because the bandwidth of the amplifier increases, which allows the amplifier to react faster to any nonlinearities in the closed-loop system.

Another significant point is the fact that distortion decreases as the impedance load increases. This is because the output resistance of the amplifier becomes less significant as compared to the output load resistance.

general configurations

A common error for the first-time CFB user is to create a unity gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration oscillates and is **not** recommended. The THS6012, like all CFB amplifiers, **must** have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a very low impedance. This results in an unstable amplifier and should not be considered when using a current-feedback amplifier. Because of this, integrators and simple low-pass filters, which are easily implemented on a VFB amplifier, have to be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see Figure 49).



$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

Figure 48. Single-Pole Low-Pass Filter

If a multiple pole filter is required, the use of a Sallen-Key filter can work very well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew-rates and high bandwidths, CFB amplifiers can create very accurate signals and help minimize distortion. An example is shown in Figure 50.

APPLICATION INFORMATION

general configurations (continued)

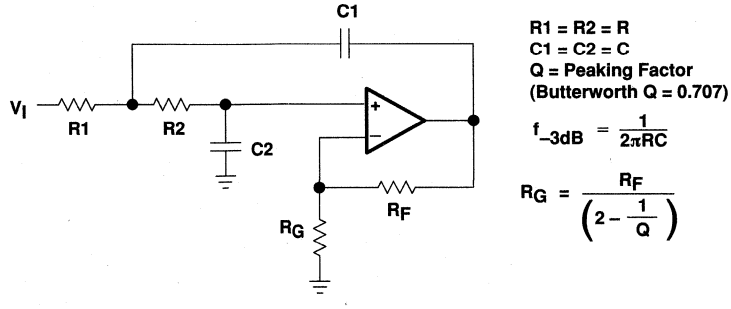


Figure 49. 2-Pole Low-Pass Sallen-Key Filter

There are two simple ways to create an integrator with a CFB amplifier. The first one shown in Figure 51 adds a resistor in series with the capacitor. This is acceptable because at high frequencies, the resistor is dominant and the feedback impedance never drops below the resistor value. The second one shown in Figure 52 uses positive feedback to create the integration. Caution is advised because oscillations can occur because of the positive feedback.

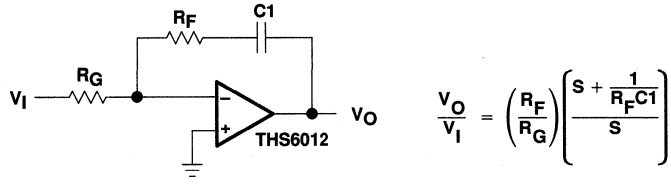


Figure 50. Inverting CFB Integrator

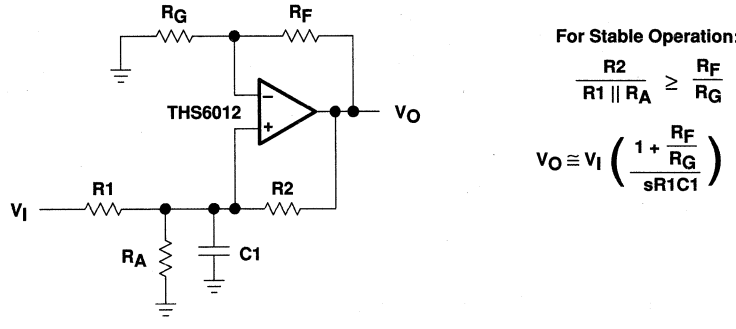


Figure 51. Non-Inverting CFB Integrator

APPLICATION INFORMATION

general configurations (continued)

Another good use for the THS6012 amplifiers is as very good video distribution amplifiers. One characteristic of distribution amplifiers is the fact that the differential phase (DP) and the differential gain (DG) are compromised as the number of lines increases and the closed-loop gain increases. Be sure to use termination resistors throughout the distribution system to minimize reflections and capacitive loading.

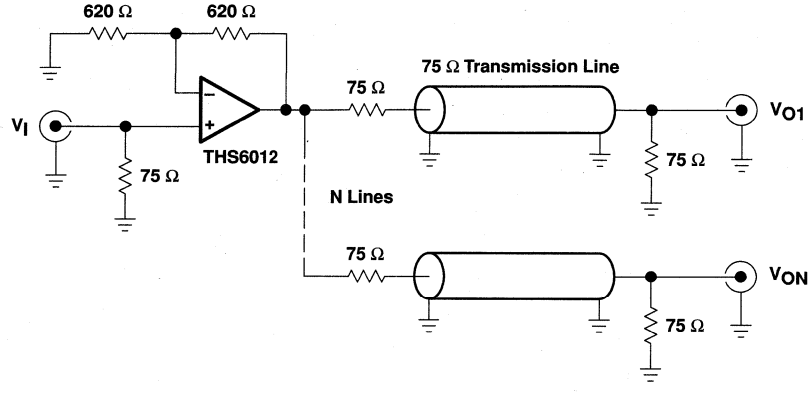


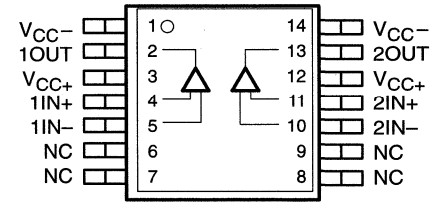
Figure 52. Video Distribution Amplifier Application

evaluation board

An evaluation board is available for the THS6012 (literature number SLOP132). This board has been configured for proper thermal management of the THS6012. The circuitry has been designed for a typical ADSL application as shown previously in this document. For more detailed information, refer to the *THS6012EVM User's Manual* (literature number SLOU034). To order the evaluation board contact your local TI sales office or distributor.

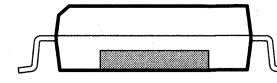
- **ADSL, HDSL and VDSL Diff. Line Driver**
- **200 mA Output Current Minimum Into 50-Ω Load**
- **High Speed**
  - **210 MHz Bandwidth (–3dB) at 50-Ω Load**
  - **300 MHz Bandwidth (–3dB) at 100-Ω Load**
  - **1900 V/μs Slew Rate, G = 5**
- **Low Distortion**
  - **–69 dB 3rd Order Harmonic Distortion at f = 1 MHz, 50-Ω Load, and $V_{O(PP)}$ = 20 V**
- **Independent Power Supplies for Low Crosstalk**
- **Wide Supply Range ±5 V to ±15 V**
- **Thermal Shutdown and Short Circuit Protection**
- **Evaluation Module Available**

Thermally Enhanced TSSOP (PWP)
PowerPAD™ Package
(TOP VIEW)



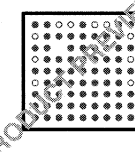
NC – No internal connection

(SIDE VIEW)

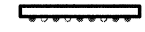


Cross Section View Showing PowerPAD
† This terminal is internally connected to the thermal pad.

MicroStar™ Junior (GQE) Package
(TOP VIEW)



(SIDE VIEW)



description

The THS6022 contains two high-speed drivers capable of providing 200 mA output current (min) into a 50-Ω load. These drivers can be configured differentially to drive a 50-V p-p output signal over low-impedance lines. The drivers are current feedback amplifiers, designed for the high slew rates necessary to support low total harmonic distortion (THD) in xDSL applications. The THS6022 is ideally suited for asymmetrical digital subscriber line (ADSL) at the remote terminal, high data rate digital suscriber line (HDSL), and very high data rate digital suscriber line (VDSL), where it supports the high-peak voltage and current requirements of these applications. Separate power supply connections for each driver are provided to minimize crosstalk.

HIGH-SPEED xDSL LINE DRIVER/RECEIVER FAMILY

DEVICE	DRIVER	RECEIVER	DESCRIPTION
THS6002	•	•	Dual differential line drivers and receivers
THS6012	•		500-mA dual differential line driver
THS6022	•		250-mA dual differential line driver
THS6032	•		Low-power ADSL central office line driver
THS6062		•	Low-noise ADSL receiver
THS7002		•	Low-noise programmable gain ADSL receiver

CAUTION: The THS6022 provides ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

PowerPAD is a trademark of Texas Instruments Incorporated.

description (continued)

The THS6022 is packaged in the patented PowerPAD package. This package provides outstanding thermal characteristics in a small footprint package, which is fully compatible with automated surface-mount assembly procedures. The exposed thermal pad on the underside of the package is in direct contact with the die. By simply soldering the pad to the PWB copper and using other thermal outlets, the heat is conducted away from the junction.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE		
	PowerPAD PLASTIC SMALL OUTLINE† (PWP)	MicroStar Junior (GQE)	EVALUATION MODULE
0°C to 70°C	THS6022CPWP	THS6022CGQE	THS6022EVM
–40°C to 85°C	THS6022IPWP	THS6022IGQE	—

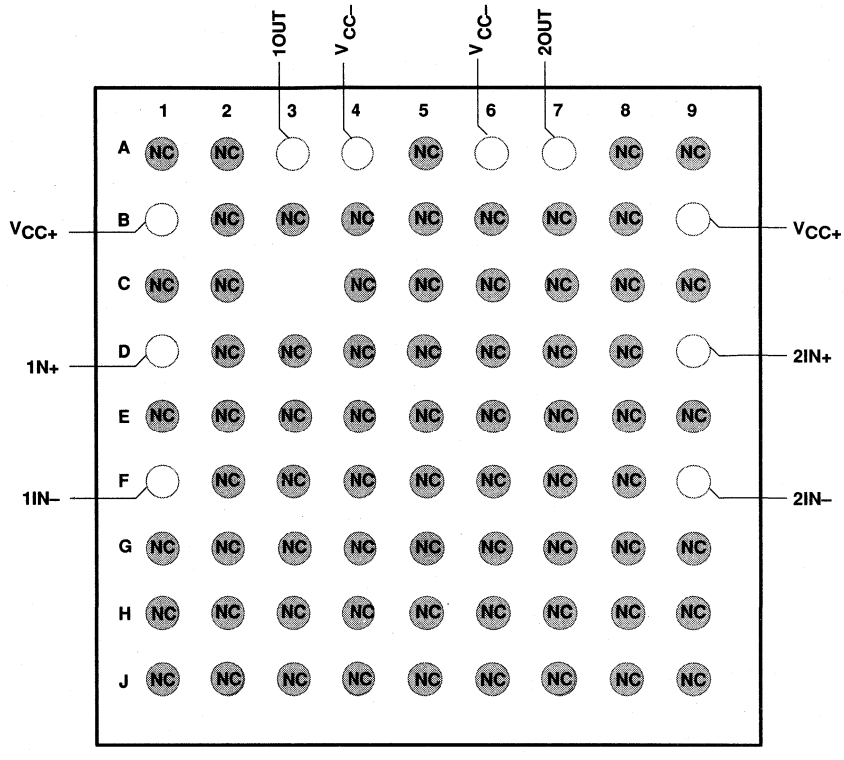
† The PWP packages are available taped and reeled. Add an R suffix to the device type (i.e., THS6022CPWPR)

Terminal Functions

TERMINAL		
NAME	PWP PACKAGE TERMINAL NO.	GQE PACKAGE TERMINAL NO.
1OUT	2	A3
1IN–	5	F1
1IN+	4	D1
2OUT	13	A7
2IN–	10	F9
2IN+	11	D9
V_{CC+}	3, 12	B1, B9
$V_{CC–}$	1, 14	A4, A6
NC	6, 7, 8 ,9	NA

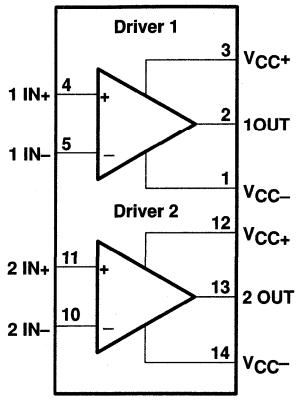
pin assignments

MicroStar™ Junior (GQE) Package
(TOP VIEW)



NOTE: Shaded terminals are used for thermal connection to the ground plane.

functional block diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC+} to V_{CC-} . . . . . 33 V
Input voltage, V_I . . . . . $\pm V_{CC}$
Output current, I_O (see Note 1) . . . . . 400 mA
Differential input voltage, V_{ID} . . . . . 6 V
Continuous total power dissipation at (or below) T_A = 25°C (see Note 1) . . . . . 3.3 W
Operating free air temperature, T_A . . . . . –40°C to 85°C
Storage temperature, T_{stg} . . . . . –65°C to 125°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The THS6022 incorporates a PowerPad on the underside of the chip. This acts as a heatsink and must be connected to a thermal dissipation plane for proper power dissipation. Failure to do so can result in exceeding the maximum junction temperature, which could permanently damage the device. See the *Thermal Information* section of this document for more information about PowerPad technology.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} and V_{CC-}	Split supply	±4.5		±16	V
	Single supply	9		32	
Operating free-air temperature, T_A	C Suffix	0		70	°C
	I Suffix	–40		85	

electrical characteristics, V_{CC} = ±15 V, R_L = 50 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
BW	Small-signal bandwidth (–3 dB)	V_O = 200 mV, G = 1	V_{CC} = ±15 V	R_F = 787 Ω		210		MHz
			V_{CC} = ±5 V	R_F = 910 Ω		150		
		V_O = 200 mV, G = 2	V_{CC} = ±15 V	R_F = 590 Ω		200		
			V_{CC} = ±5 V	R_F = 715 Ω		140		
		R_L = 100 Ω, G = 1	V_{CC} = ±15 V	R_F = 750 Ω		300		
			V_{CC} = ±5 V	R_F = 910 Ω		210		
		R_L = 100 Ω, G = 2	V_{CC} = ±15 V	R_F = 620 Ω		260		
			V_{CC} = ±5 V	R_F = 680 Ω		180		
	Bandwidth for 0.1 dB flatness	R_L = 50 Ω, G = 2,	V_{CC} = ±15 V	R_F = 590 Ω		115		MHz
			V_{CC} = ±5 V	R_F = 715 Ω		70		
		R_L = 100 Ω, G = 2,	V_{CC} = ±15 V	R_F = 620 Ω		140		
			V_{CC} = ±5 V	R_F = 680 Ω		80		
SR	Slew rate (see Note 2)	V_{CC} = ±15 V,	$V_{O(PP)}$ = 20 V,	G = 5		1900		V/µs
		V_{CC} = ±5 V,	$V_{O(PP)}$ = 5 V,	G = 2		950		
t_s	Settling time to 0.1%	0 V to 10 V Step,	G = 2,	R_L = 1 kΩ		70		ns
	Full power bandwidth (see Note 3)	V_{CC} = ±15 V,	V_O = 20 $V_{(PP)}$			30		MHz
		V_{CC} = ±5 V,	V_O = 4 $V_{(PP)}$			75		

NOTES: 2. Slew rate is measured from an output level range of 25% to 75%.
3. Full power bandwidth = slew rate/$2\pi V_{peak}$

noise/distortion performance

PARAMETER			TEST CONDITIONS			MIN	TYP	MAX	UNIT
THD	Total harmonic distortion		V_{CC} = ±15 V, G = 2	f = 500 kHz	$V_{O(PP)}$ = 20 V		–69		dBc
					$V_{O(PP)}$ = 2 V		–80		
				f = 1 MHz	$V_{O(PP)}$ = 20 V		–66		
					$V_{O(PP)}$ = 2 V		–75		
			V_{CC} = ±5 V, $V_{O(PP)}$ = 2 V, G = 2	R_L = 25 Ω	f = 500 kHz		–71		
					f = 1 MHz		–65		
				R_L = 50 Ω	f = 500 kHz		–78		
					f = 1 MHz		–72		
I_n	Input noise current	Positive (IN+)	V_{CC} = ±5 V or ±15 V,	G = 2,	f = 10 kHz,		11.5		pA/√Hz
		Negative (IN–)					16		
A_D	Differential gain error		R_L = 150 Ω, G = 2	NTSC, 40 IRE Mod.	V_{CC} = ±5 V		0.03%		
					V_{CC} = ±15 V		0.04%		
ϕ_D	Differential phase error		R_L = 150 Ω, G = 2	NTSC, 40 IRE Mod.	V_{CC} = ±5 V		0.08°		
					V_{CC} = ±15 V		0.06°		
	Crosstalk		V_I = 200 mV,	f = 1 MHz			–64		dB
V_n	Input voltage noise		V_{CC} = ±5 V or ±15 V, Single-ended	f = 10 kHz,	G = 2,		1.7		nV/√Hz

electrical characteristics, V_{CC} = ±15 V, R_L = 50 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted) (continued)

dc performance

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage		V_{CC} = ±5 V or ±15 V	T_A = 25°C		1	5	mV
				T_A = full range			7	
	Input offset voltage drift		V_{CC} = ±5 V or ±15 V,	T_A = full range			20	µV/°C
	Differential input offset voltage		V_{CC} = ±5 V or ±15 V	T_A = 25°C		0.5	4	mV
				T_A = full range			5	
	Differential input offset voltage drift		V_{CC} = ±5 V or ±15 V,	T_A = full range			10	µV/°C
I_{IB}	Input bias current	Negative	V_{CC} = ±5 V or ±15 V	T_A = 25°C		1	9	µA
				T_A = full range			12	
		Positive		T_A = 25°C		5	10	µA
				T_A = full range			12	
		Differential		T_A = 25°C		1.5	8	µA
				T_A = full range			11	
	Open loop transresistance		V_{CC} = ±5 V			1		MΩ
			V_{CC} = ±15 V			4		

† Full range is 0°C to 70°C for the THS6022C and –40°C to 85°C for the THS6022I.

input characteristics

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{ICR}	Common-mode input voltage range		V_{CC} = ±5 V		±3.5	±3.6		V
			V_{CC} = ±15 V		±13.3	±13.4		
CMRR	Common-mode rejection ratio		V_{CC} = ±5 V or ±15 V,	T_A = full range	62	73		dB
	Differential common-mode rejection ratio					100		
r_i	Input resistance	+ Input				1.5		MΩ
		– Input				15		Ω
C_i	Input capacitance					1.4		pF

† Full range is 0°C to 70°C for the THS6022C and –40°C to 85°C for the THS6022I.

output characteristics

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_O	Output voltage swing	Single ended	R_L = 50 Ω	V_{CC} = ±5 V	±3.1	±3.2		V
				V_{CC} = ±15 V	±12.3	±12.6		
		Differential	R_L = 100 Ω	V_{CC} = ±5 V	±6.2	±6.6		V
				V_{CC} = ±15 V	±24.6	±25.2		
I_O	Output current (see Note 2)		V_{CC} = ±5 V,	R_L = 5 Ω		250		mA
			V_{CC} = ±15 V,	R_L = 50 Ω	200	250		
I_{OS}	Short-circuit output current (see Note 4)					400		mA
R_O	Output resistance		Open loop			13		Ω

† Full range is 0°C to 70°C for the THS6022C and –40°C to 85°C for the THS6022I.

NOTES: 2. Slew rate is measured from an output level range of 25% to 75%.

4. A heat sink is required to keep the junction temperature below absolute maximum when an output is heavily loaded or shorted. See absolute maximum ratings and Thermal Information section.

electrical characteristics, V_{CC} = ±15 V, R_L = 50 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted) (continued)

power supply

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{CC}	Power supply operating range	Split supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Quiescent current (each driver)	V_{CC} = ±5 V	T_A = 25°C		6	8	mA
			T_A = full range			10	
		V_{CC} = ±15 V	T_A = 25°C		7.2	9	
			T_A = full range			11	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V	T_A = 25°C	−68	−76		dB
			T_A = full range	−65			
		V_{CC} = ±15 V	T_A = 25°C	−64	−75		dB
			T_A = full range	−62			

† Full range is 0°C to 70°C for the THS6022C and −40°C to 85°C for the THS6022I.

PARAMETER MEASUREMENT INFORMATION

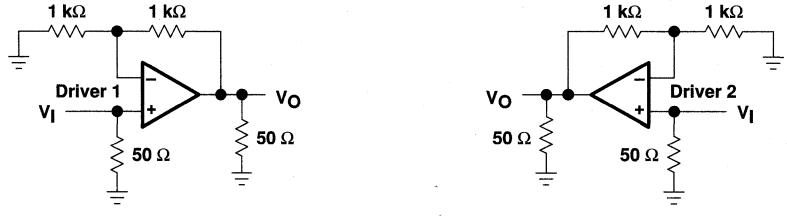


Figure 1. Input-to-Output Crosstalk Test Circuit

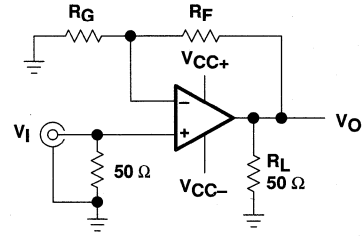


Figure 2. Test Circuit, Gain = 1 + (R_F/R_G)

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$V_{O(PP)}$	Peak-to-peak output voltage	vs Load resistance	3
	Maximum peak-to-peak output voltage swing	vs Free-air temperature	4
V_{IO}	Input offset voltage	vs Free-air temperature	5
I_{IB}	Input bias current	vs Free-air temperature	6
	Positive input bias current	vs Common-mode input votlage	7
CMMR	Common-mode rejection ratio	vs Free-air temperature	8
	Input-to-output crosstalk	vs Frequency	9
PSSR	Power supply rejection ratio	vs Free-air temperature	10
	Closed-loop output impedance	vs Frequency	11
I_{CC}	Supply current	vs Free-air temperature	12
SR	Slew rate	vs Output step	13, 14
V_n	Input voltage noise	vs Frequency	15
I_n	Input current noise	vs Frequency	15
	Output amplitude	vs Frequency	16, 17, 19 – 32
	Closed-loop output phase	vs Frequency	18
	Small and large frequency response		33 – 36
	Single-ended output distortion	vs Output voltage	37, 38
	Harmonic distortion	vs Frequency	39, 40
	Differential gain	Number of 150-Ω loads	41, 42
	Differential phase	Number of 150-Ω loads	43, 44
	400-mV output step response		45, 47
	20-V step response		46
	4-V step response		48

TYPICAL CHARACTERISTICS

PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

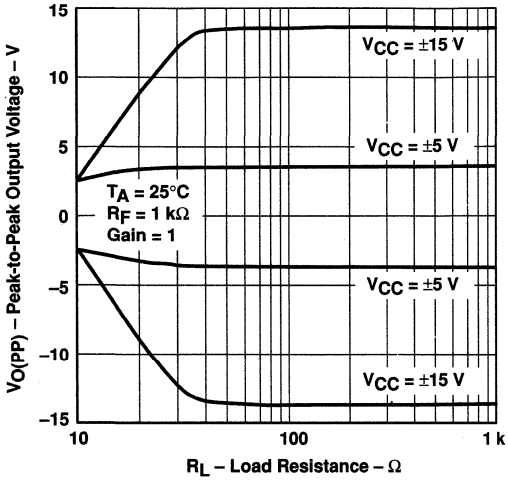


Figure 3

MAXIMUM PEAK–TO-PEAK OUTPUT VOLTAGE SWING vs FREE-AIR TEMPERATURE

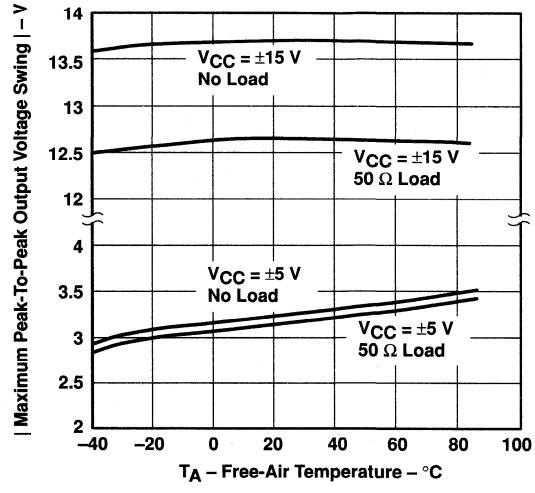


Figure 4

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

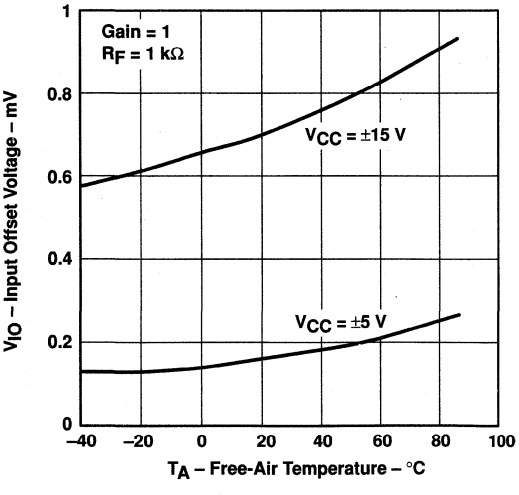


Figure 5

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

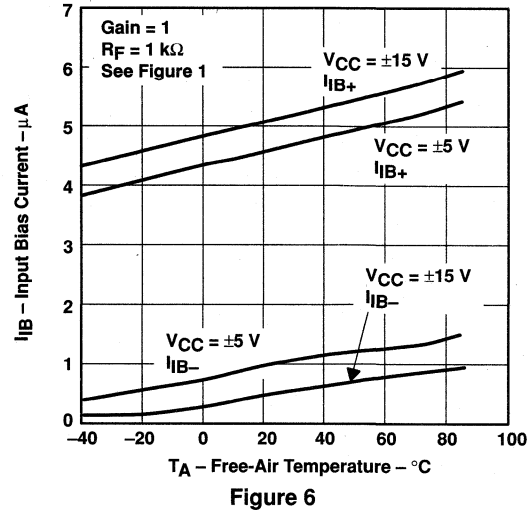


Figure 6

TYPICAL CHARACTERISTICS

POSITIVE INPUT BIAS CURRENT
vs
COMMON-MODE INPUT VOLTAGE

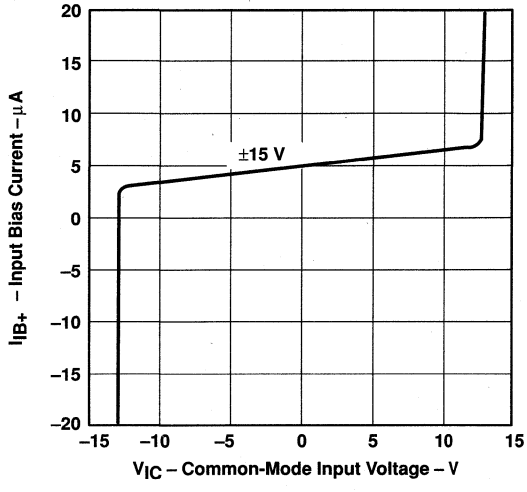


Figure 7

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

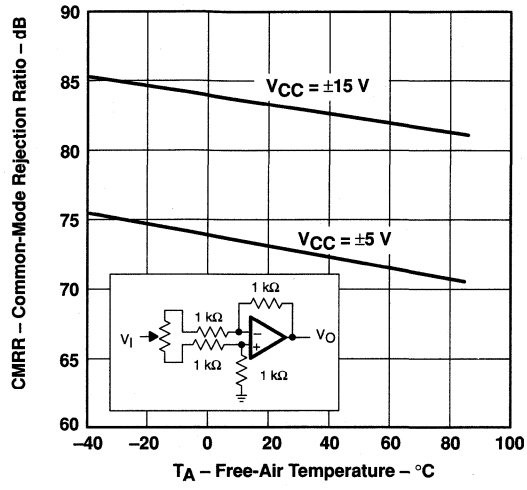


Figure 8

INPUT-TO-OUTPUT CROSSTALK
vs
FREQUENCY

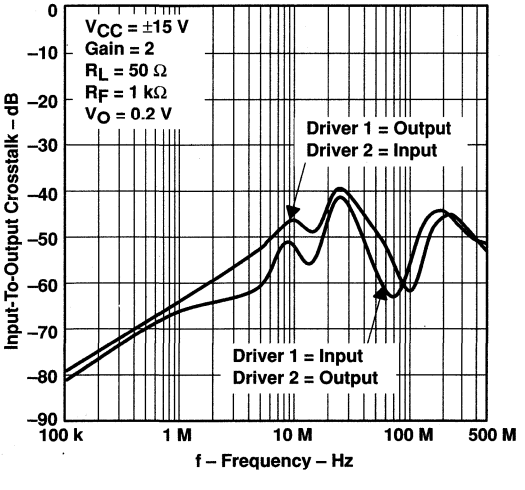


Figure 9

POWER SUPPLY REJECTION RATIO
vs
FREE-AIR TEMPERATURE

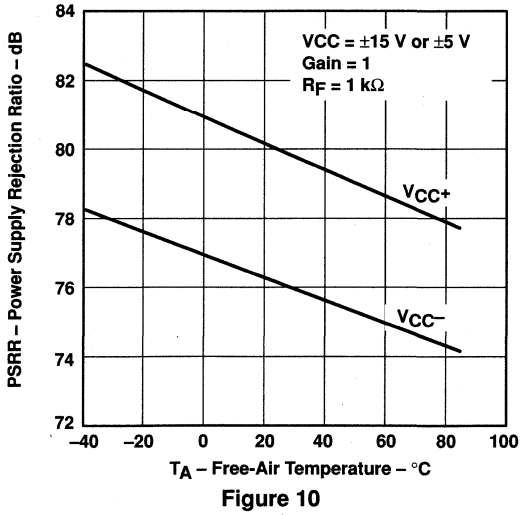


Figure 10

TYPICAL CHARACTERISTICS

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

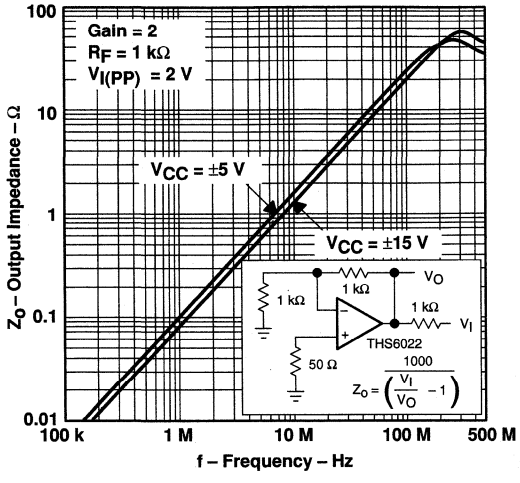


Figure 11

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

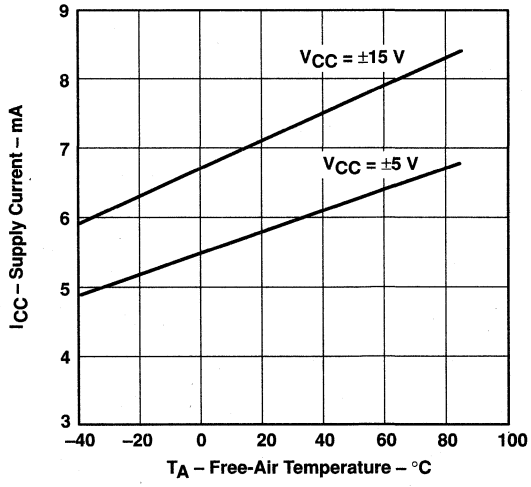


Figure 12

SLEW RATE vs OUTPUT STEP

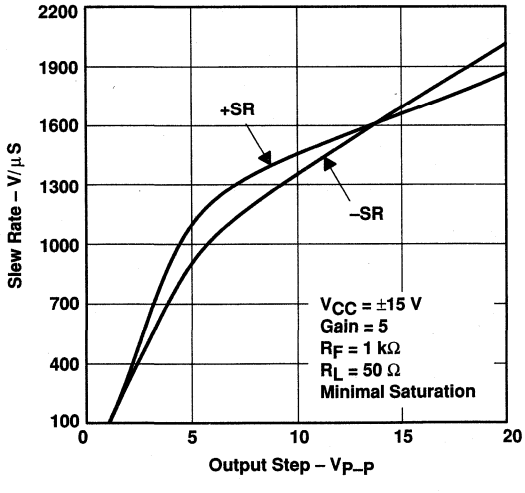


Figure 13

SLEW RATE vs OUTPUT STEP

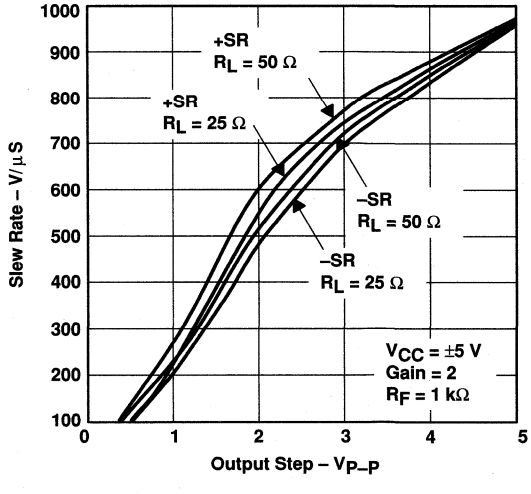


Figure 14

TYPICAL CHARACTERISTICS

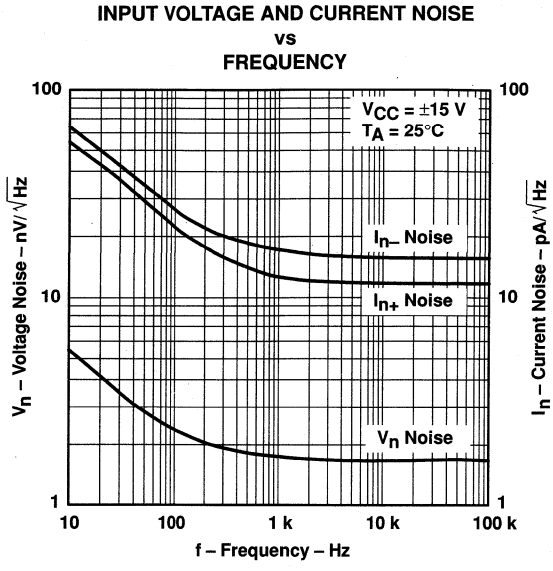


Figure 15

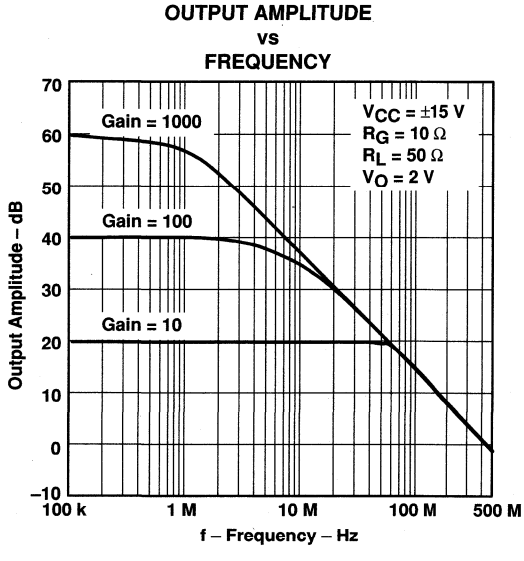


Figure 16

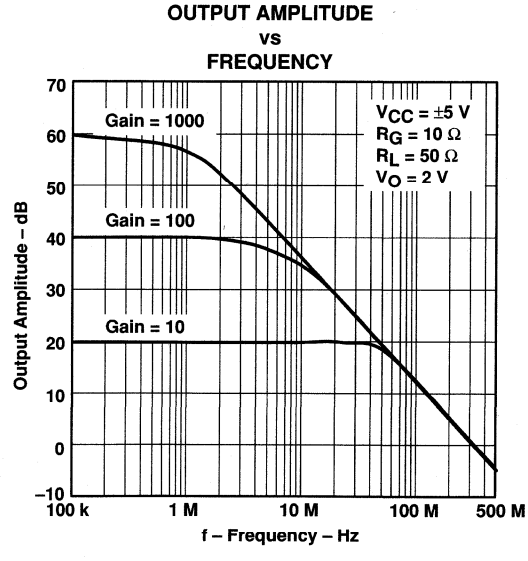


Figure 17

TYPICAL CHARACTERISTICS

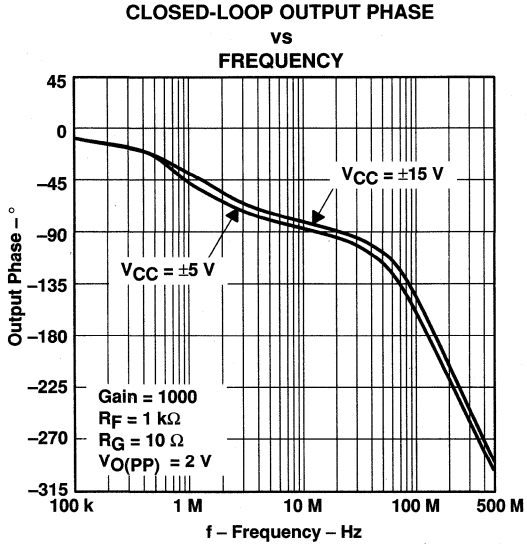


Figure 18

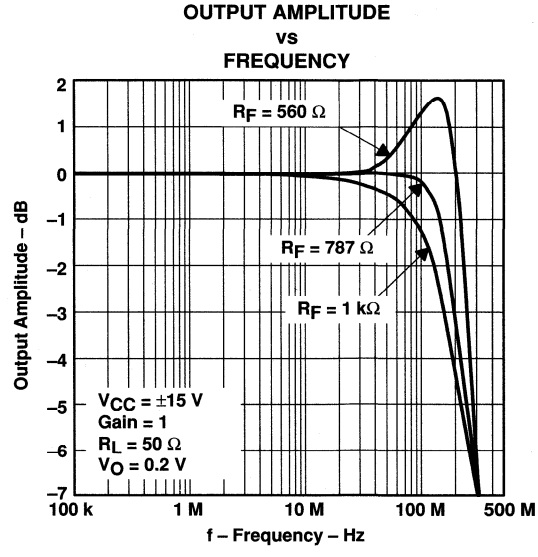


Figure 19

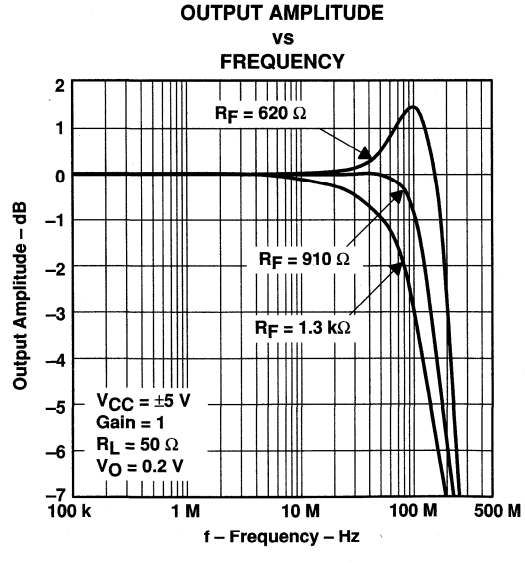


Figure 20

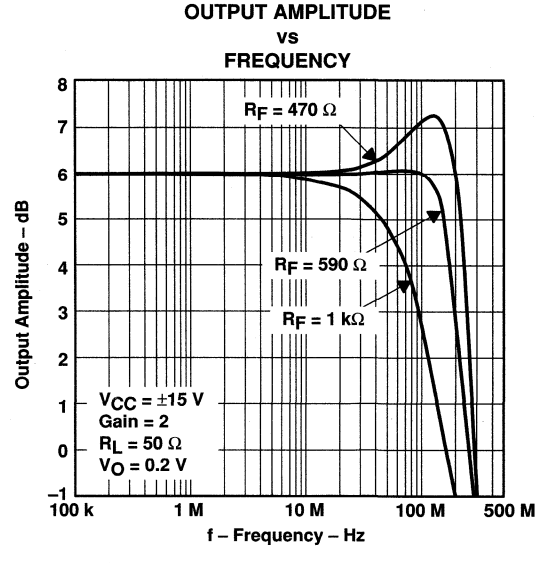


Figure 21

TYPICAL CHARACTERISTICS

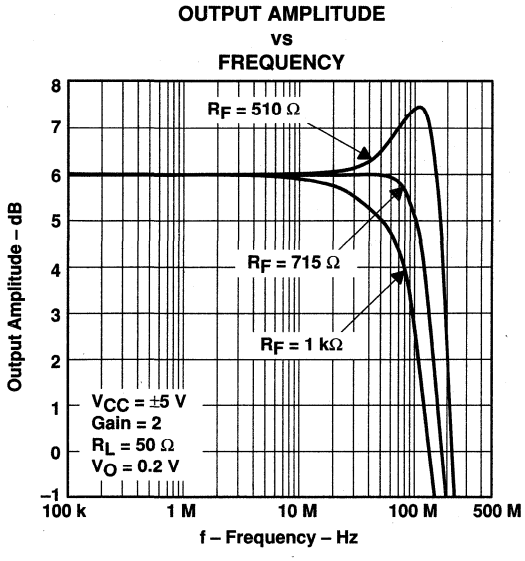


Figure 22

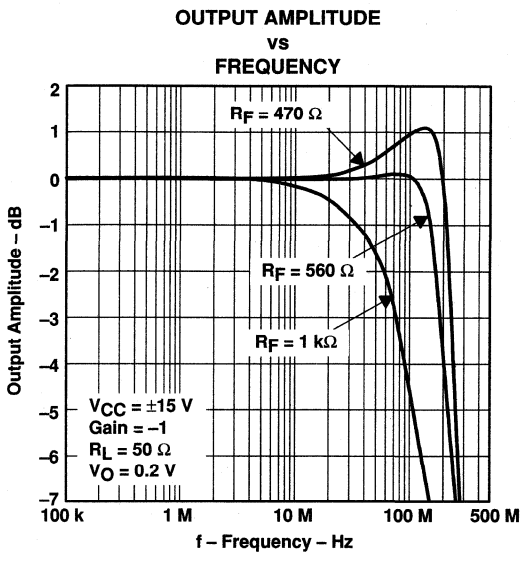


Figure 23

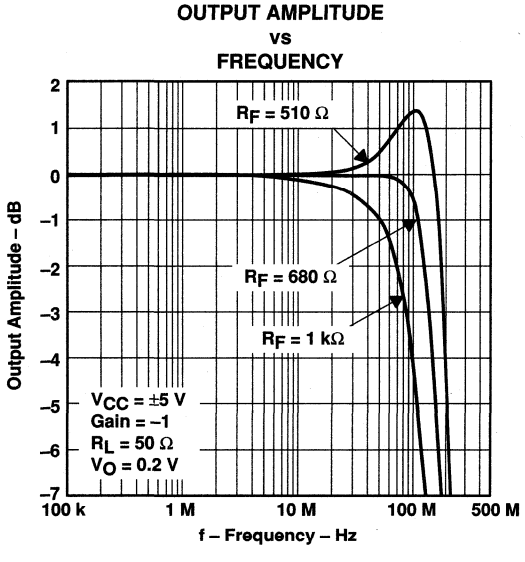


Figure 24

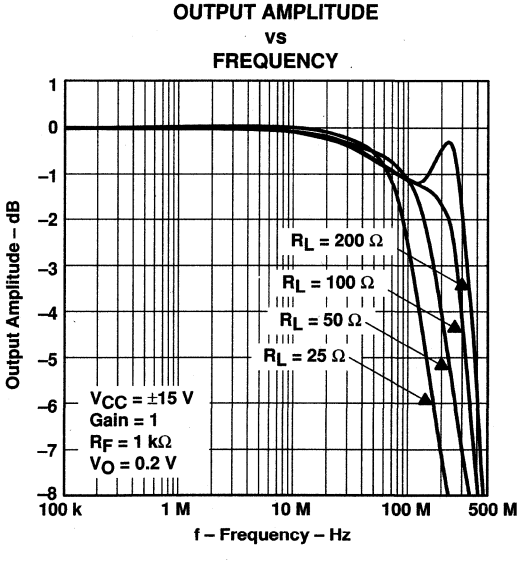


Figure 25

TYPICAL CHARACTERISTICS

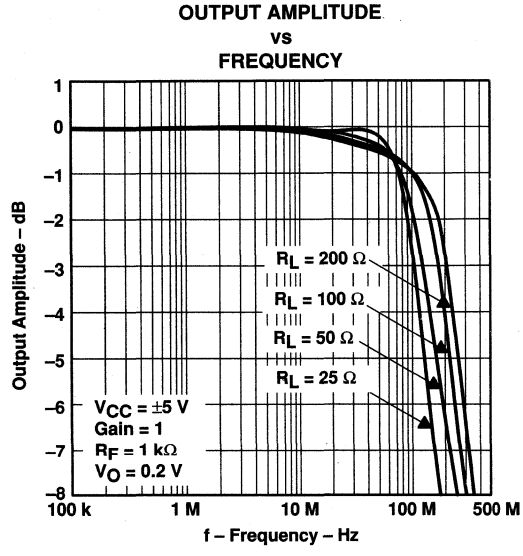


Figure 26

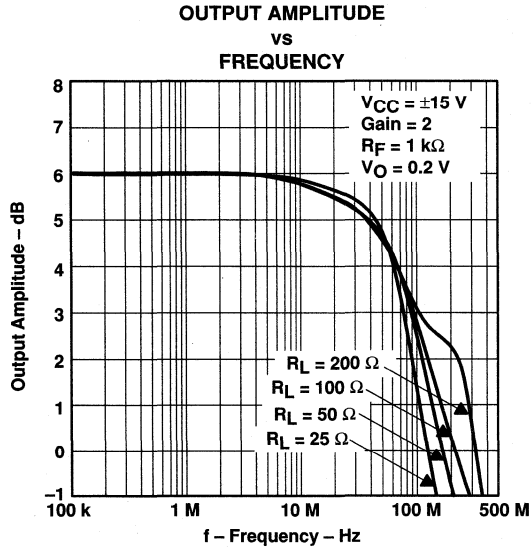


Figure 27

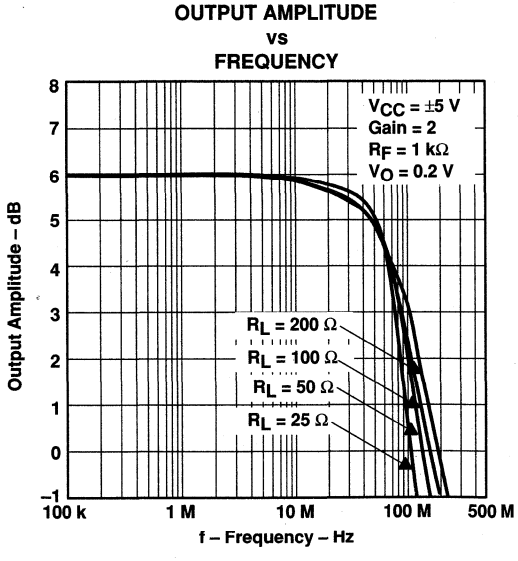


Figure 28

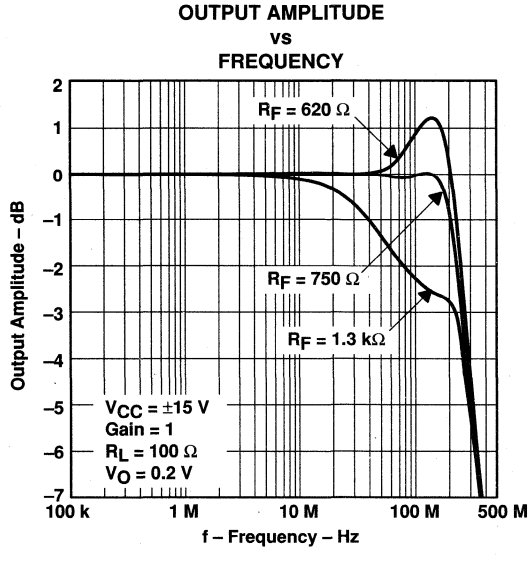


Figure 29

TYPICAL CHARACTERISTICS

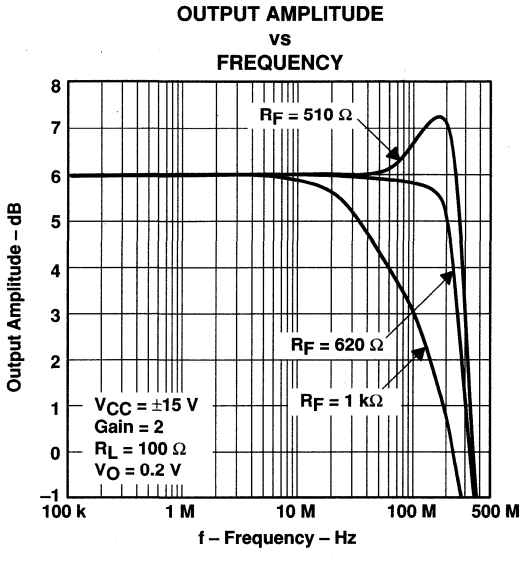


Figure 30

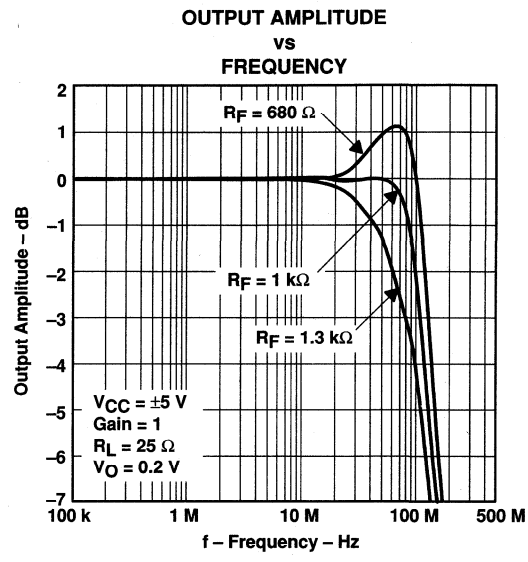


Figure 31

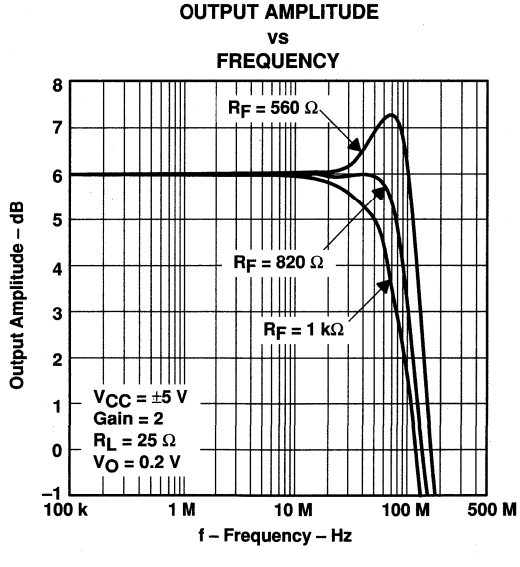


Figure 32

TYPICAL CHARACTERISTICS

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

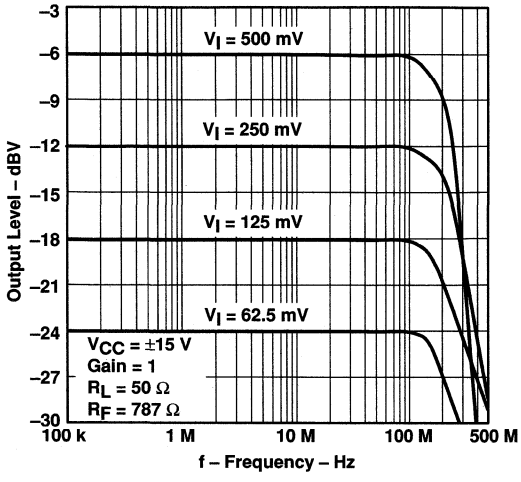


Figure 33

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

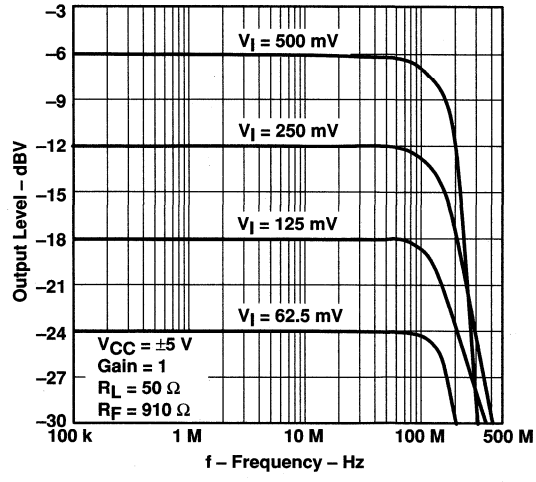


Figure 34

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

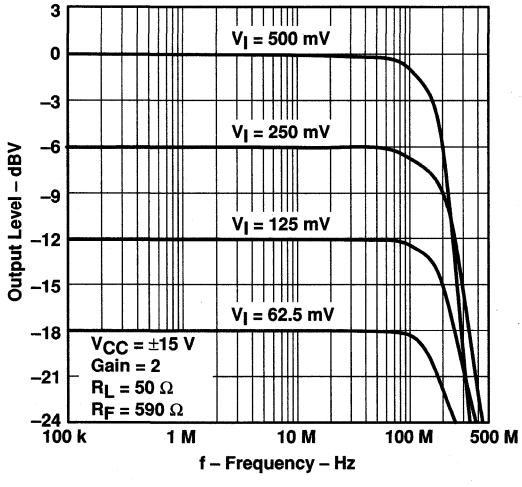


Figure 35

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

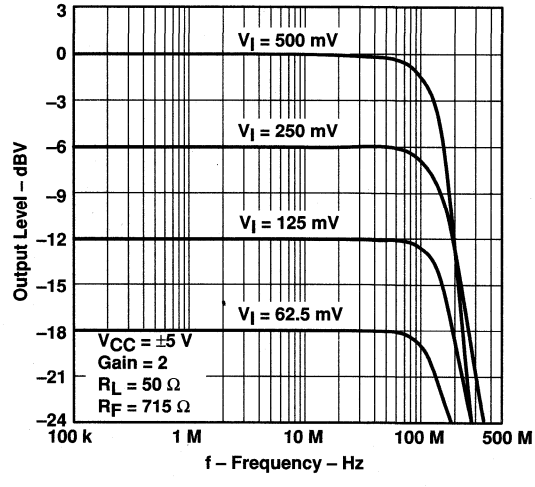


Figure 36

TYPICAL CHARACTERISTICS

SINGLE-ENDED OUTPUT DISTORTION
vs
OUTPUT VOLTAGE

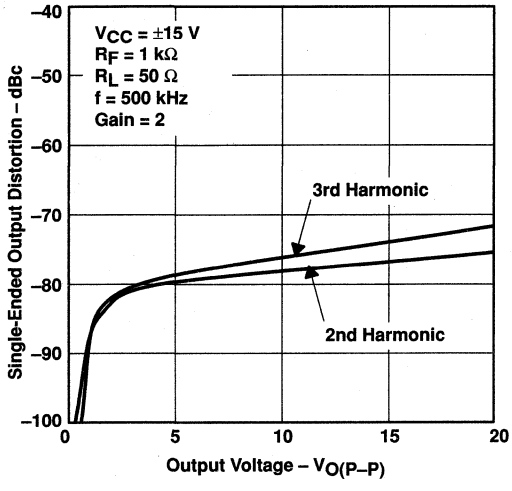


Figure 37

SINGLE-ENDED OUTPUT DISTORTION
vs
OUTPUT VOLTAGE

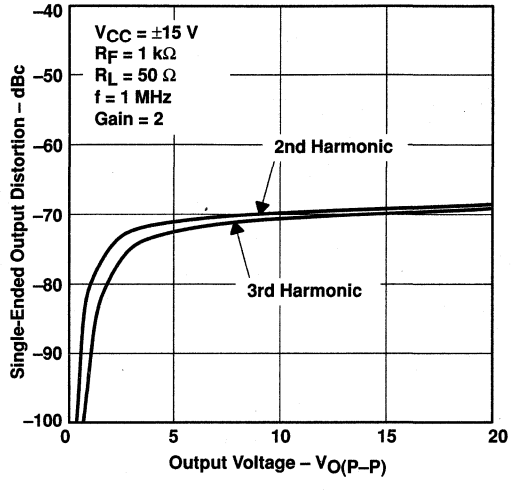


Figure 38

HARMONIC DISTORTION
vs
FREQUENCY

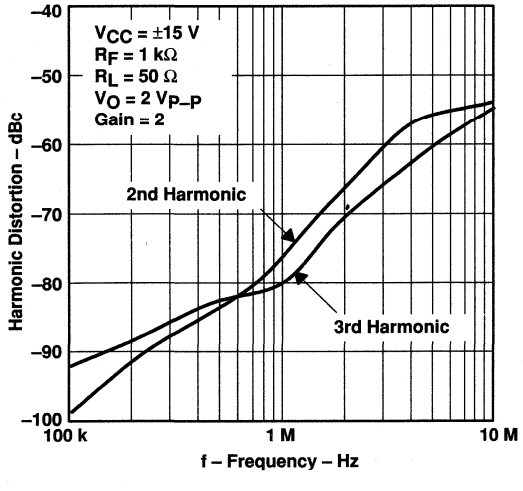


Figure 39

HARMONIC DISTORTION
vs
FREQUENCY

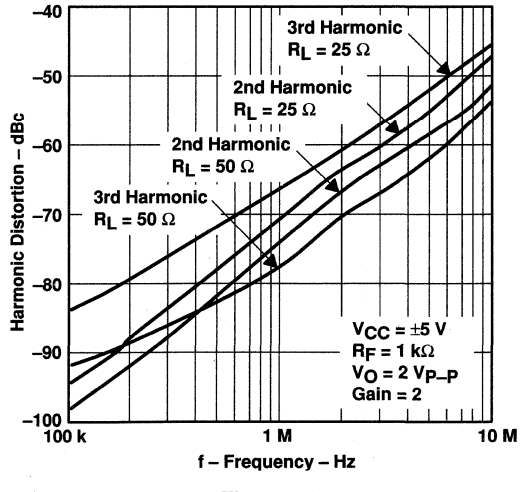


Figure 40

TYPICAL CHARACTERISTICS

DIFFERENTIAL GAIN
vs
LOADING

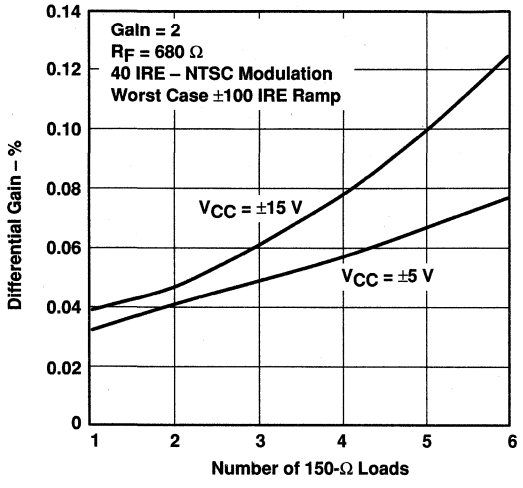


Figure 41

DIFFERENTIAL GAIN
vs
LOADING

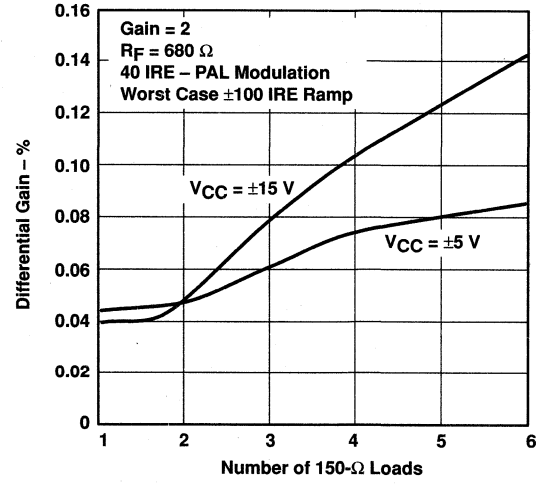


Figure 42

DIFFERENTIAL PHASE
vs
LOADING

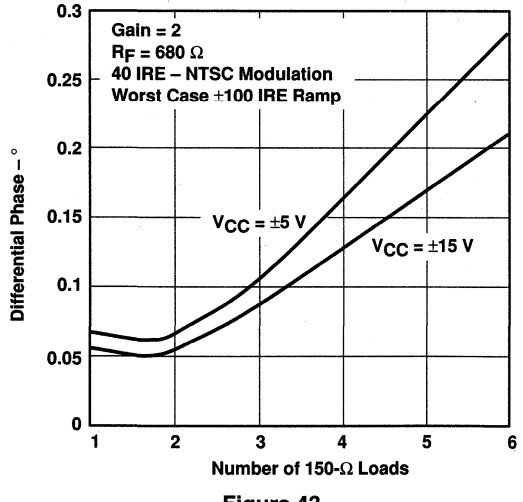


Figure 43

DIFFERENTIAL PHASE
vs
LOADING

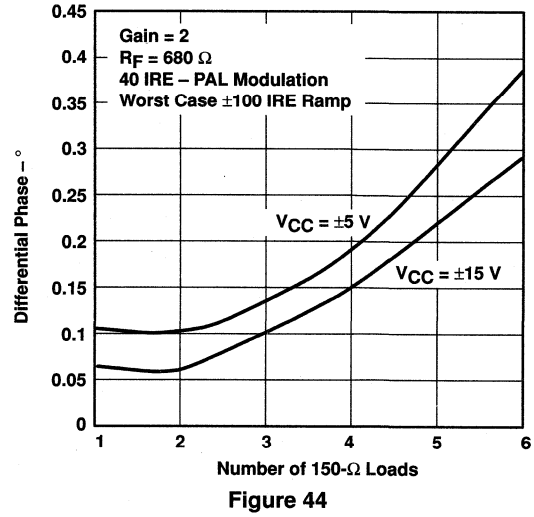


Figure 44

TYPICAL CHARACTERISTICS

400-mV STEP RESPONSE

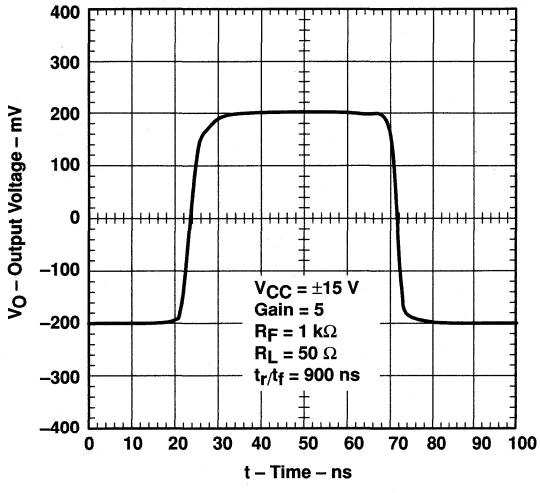


Figure 45

20-V STEP RESPONSE

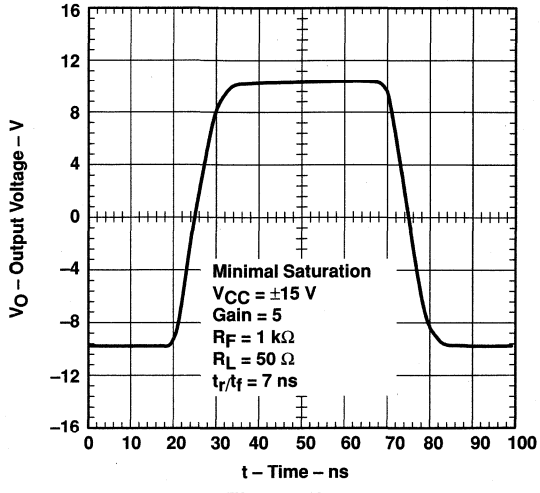


Figure 46

400-mV STEP RESPONSE

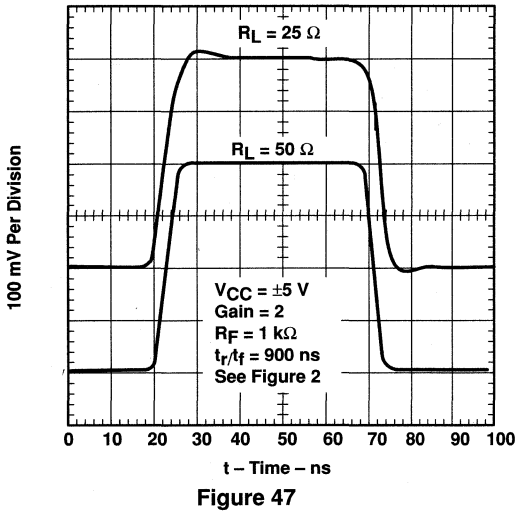


Figure 47

4-V STEP RESPONSE

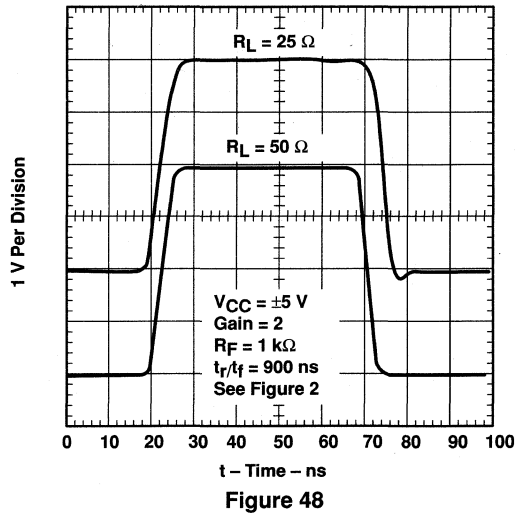
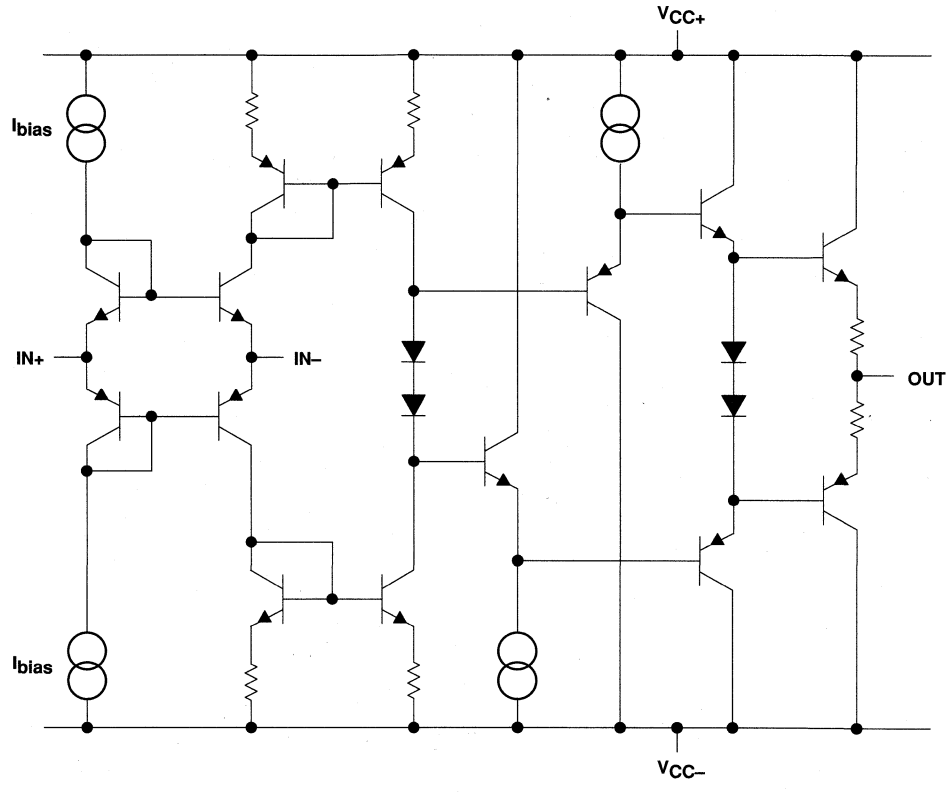


Figure 48

APPLICATION INFORMATION

simplified schematic



The THS6022 contains two independent operational amplifiers. These amplifiers are current feedback topology amplifiers made for high-speed operation. They have been specifically designed to deliver the full power requirements of ADSL and therefore can deliver output currents of at least 200 mA at full output voltage.

The THS6022 is fabricated using Texas Instruments 30-V complementary bipolar process, HVBiCOM. This process provides excellent isolation and high slew rates that result in the device's excellent crosstalk and extremely low distortion.

independent power supplies

Each amplifier of the THS6022 has its own power supply pins. This was specifically done to solve a problem that often occurs when multiple devices in the same package share common power pins. This problem is crosstalk between the individual devices caused by currents flowing in common connections. Whenever the current required by one device flows through a common connection shared with another device, this current, in conjunction with the impedance in the shared line, produces an unwanted voltage on the power supply. Proper power supply decoupling and good device power supply rejection helps to reduce this unwanted signal. What is left is crosstalk.

independent power supplies (continued)

However, with independent power supply pins for each device, the effects of crosstalk through common impedance in the power supplies are more easily managed. This is because it is much easier to achieve low common impedance on the PCB with copper etch than it is to achieve low impedance within the package with either bond wires or metal traces on silicon.

power supply restrictions

Although the THS6022 is specified for operation from power supplies of ±5 V to ±15 V (or singled-ended power supply operation from 10 V to 30 V), and each amplifier has its own power supply pins, several precautions must be taken to assure proper operation.

1. The power supplies for each amplifier must be the same value. For example, if the driver 1 uses ±15 volts, then the driver 2 must also use ±15 volts. Using ±15 volts for one amplifier and ±5 volts for another amplifier is not allowed.
2. To save power by powering down one of the amplifiers in the package, the following rules must be followed.
   - The amplifier designated driver 1 must always receive power. This is because the internal startup circuitry uses the power from the driver 1 device.
   - The $-V_{CC}$ pins from both drivers must always be at the same potential.
   - Individual amplifiers are powered down by simply opening the $+V_{CC}$ connection.

The THS6022 incorporates a standard Class A-B output stage. This means that some of the quiescent current is directed to the load as the load current increases. So under heavy load conditions, accurate power dissipation calculations are best achieved through actual measurements. For small loads, however, internal power dissipation for each amplifier in the THS6022 can be approximated by the following formula:

$$P_D \cong \left(2\ V_{CC}\ I_{CC}\right) + \left(V_{CC} - V_O\right) \times \left(\frac{V_O}{R_L}\right)$$

Where:

P_D = Power dissipation for one amplifier
V_{CC} = Split supply voltage
I_{CC} = Supply current for that particular amplifier
V_O = RMS output voltage of amplifier
R_L = Load resistance

To find the total THS6022 power dissipation, we simply sum up both amplifier power dissipation results. Generally, the worst case power dissipation occurs when the output voltage is one-half the V_{CC} voltage. One last note, which is often overlooked: the feedback resistor (R_F) is also a load to the output of the amplifier and should be taken into account for low value feedback resistors.

device protection features

The THS6022 has two built-in features that protect the device against improper operation. The first protection mechanism is output current limiting. Should the output become shorted to ground the output current is automatically limited to the value given in the data sheet. While this protects the output against excessive current, the device internal power dissipation increases due to the high current and large voltage drop across the output transistors. Continuous output shorts are not recommended and could damage the device. Additionally, connection of the amplifier output to one of the supply rails ($\pm V_{CC}$) can cause failure of the device and is not recommended.

APPLICATION INFORMATION

device protection features (continued)

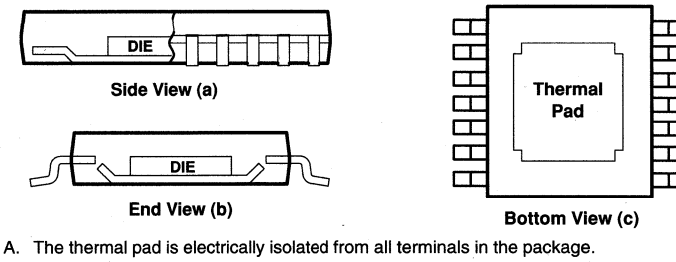
The second built-in protection feature is thermal shutdown. Should the internal junction temperature rise above approximately 180°C, the device automatically shuts down. Such a condition could exist with improper heat sinking or if the output is shorted to ground. When the abnormal condition is fixed, the internal thermal shutdown circuit automatically turns the device back on.

thermal information

The THS6022 is packaged in a thermally-enhanced PWP package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 50(a) and Figure 50(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 50(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device. This is discussed in more detail in the *PCB design considerations* section of this document.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.



NOTE A. The thermal pad is electrically isolated from all terminals in the package.

Figure 49. Views of Thermally Enhanced PWP Package

APPLICATION INFORMATION

recommended feedback and gain resistor values

As with all current feedback amplifiers, the bandwidth of the THS6022 is an inversely proportional function of the value of the feedback resistor. This can be seen from Figures 19 to 32. The recommended resistors for the optimum frequency response are shown in Table 1. These should be used as a starting point and once optimum values are found, 1% tolerance resistors should be used to maintain frequency response characteristics. Because there is a finite amount of output resistance of the operational amplifier, load resistance can play a major part in frequency response. This is especially true with these drivers, which tend to drive low-impedance loads. This can be seen in Figure 10 and Figures 25 – 28. As the load resistance increases, the output resistance of the amplifier becomes less dominant at high frequencies. To compensate for this, the feedback resistor should change. Although, for most applications, a feedback resistor value of 1 kΩ is recommended, which is a good compromise between bandwidth and phase margin that yields a very stable amplifier.

Table 1. Recommended Feedback (R_F) Values for Optium Frequency Response

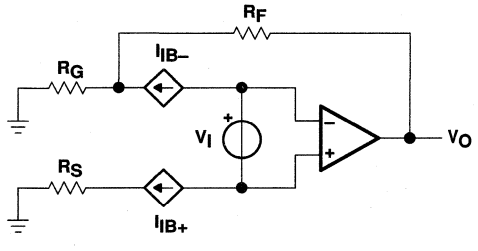
GAIN	V_{CC} = ±15 V		V_{CC} = ±15 V		
	R_L = 50 Ω	R_L = 100 Ω	R_L = 25 Ω	R_L = 50 Ω	R_L = 100 Ω
1	787 Ω	750 Ω	1 kΩ	910 Ω	820 Ω
2	590 Ω	590 Ω	820 Ω	715 Ω	680 Ω
–1	560 Ω	—	—	680 Ω	—

Consistent with current feedback amplifiers, increasing the gain is best accomplished by changing the gain resistor, not the feedback resistor. This is because the bandwidth of the amplifier is dominated by the feedback resistor value and internal dominant-pole capacitor. The ability to control the amplifier gain independently of the bandwidth constitutes a major advantage of current feedback amplifiers over conventional voltage feedback amplifiers. Therefore, once a frequency response is found suitable to a particular application, adjust the value of the gain resistor to increase or decrease the overall amplifier gain.

Finally, it is important to realize the effects of the feedback resistance on distortion. Increasing the resistance decreases the loop gain and increases the distortion. It is also important to know that decreasing load impedance increases total harmonic distortion (THD). Typically, the third order harmonic distortion increases more than the second order harmonic distortion. This is illustrated in Figure 40.

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

Figure 50. Output Offset Voltage Model

APPLICATION INFORMATION

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true for the amplifying small signals. The noise model for current feedback amplifiers (CFB) is the same as voltage feedback amplifiers (VFB). The only difference between the two is that the CFB amplifiers generally specify different current noise parameters for each input, while VFB amplifiers usually only specify one noise current parameter. The noise model is shown in Figure 52. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise ($nV/\sqrt{Hz}$)
- IN+ = Noninverting current noise ($pA/\sqrt{Hz}$)
- IN– = Inverting current noise ($pA/\sqrt{Hz}$)
- e_{Rx} = Thermal voltage noise associated with each resistor ($e_{Rx} = 4\ kTR_x$)

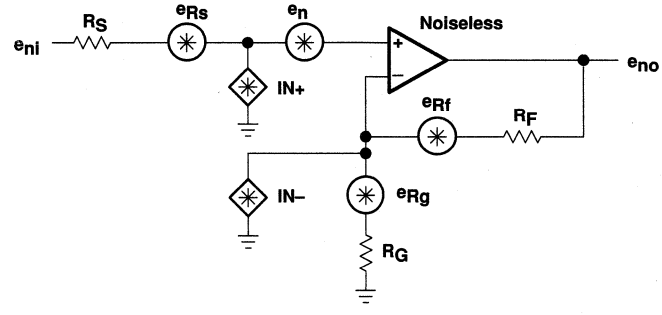


Figure 51. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN + \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\ kTR_s + 4\ kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\ A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

APPLICATION INFORMATION

noise calculations and noise figure (continued)

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^{\ 2}}{(e_{Rs})^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[(e_n)^2 + (IN + \times R_S)^2\right]}{4\ kTR_S}\right]$$

Figure 52 shows the noise figure graph for the THS6022.

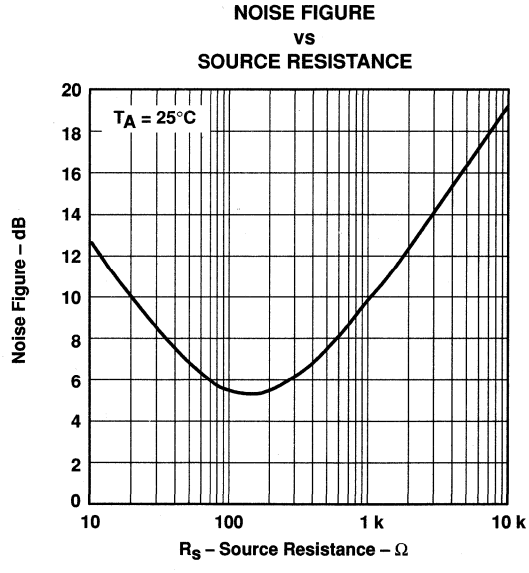


Figure 52. Noise Figure vs Source Resistance

APPLICATION INFORMATION

slew rate

The slew rate performance of a current feedback amplifier, like the THS6022, is affected by many different factors. Some of these factors are external to the device, such as amplifier configuration and PCB parasitics, and others are internal to the device, such as available currents and node capacitance. Understanding some of these factors should help the PCB designer arrive at a more optimum circuit with fewer problems.

Whether the THS6022 is used in an inverting amplifier configuration or a noninverting configuration can impact the output slew rate. Slew rate performance in the inverting configuration is generally faster than the noninverting configuration. This is because in the inverting configuration the input terminals of the amplifier are at a virtual ground and do not significantly change voltage as the input changes. Consequently, the time to charge any capacitance on these input nodes is less than for the noninverting configuration, where the input nodes actually do change in voltage an amount equal to the size of the input step. In addition, any PCB parasitic capacitance on the input nodes degrades the slew rate further simply because there is more capacitance to charge. If the supply voltage (V_{CC}) to the amplifier is reduced, slew rate decreases because there is less current available within the amplifier to charge the capacitance on the input nodes as well as other internal nodes. Also, as the load resistance decreases, the slew rate typically decreases due to the increasing internal currents, which slow down the transitions (see Figures 13 and 14)

Internally, the THS6022 has other factors that impact the slew rate. The amplifier's behavior during the slew rate transition varies slightly depending upon the rise time of the input. This is because of the way the input stage handles faster and faster input edges. Slew rates (as measured at the amplifier output) of less than about 1300 V/µs are processed by the input stage in a very linear fashion. Consequently, the output waveform smoothly transitions between initial and final voltage levels. This is shown in Figure 53. For slew rates greater than 1300 V/µs, additional slew-enhancing transistors present in the input stage begin to turn on to support these faster signals. The result is an amplifier with extremely fast slew rate capabilities. Figure 54 shows waveforms for these faster slew rates. The additional aberrations present in the output waveform with these faster slewing input signals are due to the brief saturation of the internal current mirrors. This phenomenon, which typically lasts less than 20 ns, is considered normal operation and is not detrimental to the device in any way. If for any reason this type of response is not desired, then increasing the feedback resistor or slowing down the input signal slew rate reduces the effect.

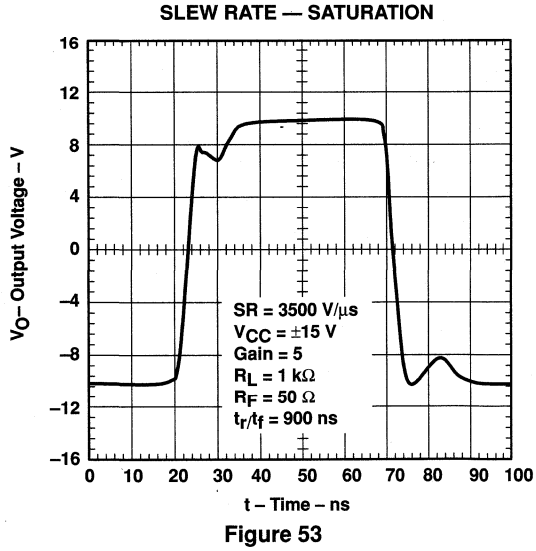


Figure 53

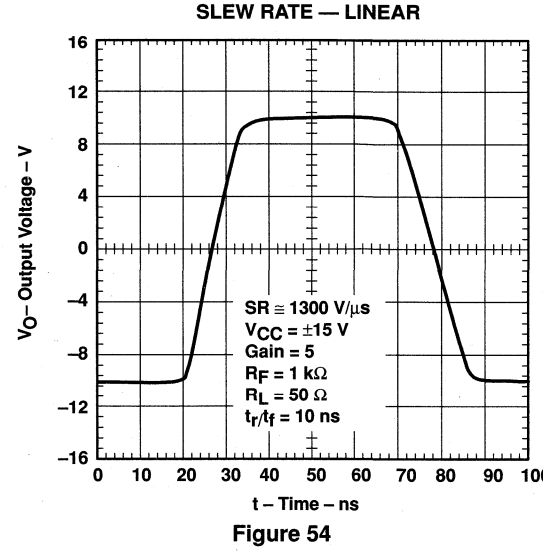


Figure 54

APPLICATION INFORMATION

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS6022 has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 55. A minimum value of 15 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

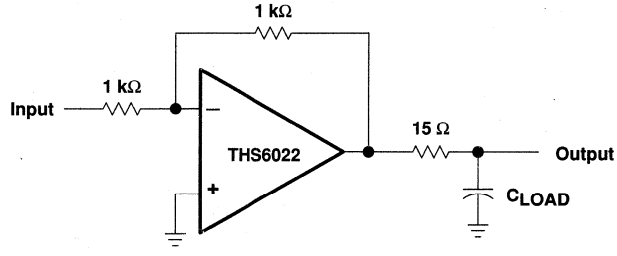


Figure 55. Driving a Capacitive Load

PCB design considerations

Proper PCB design techniques in two areas are important to assure proper operation of the THS6022. These areas are high-speed layout techniques and thermal-management techniques. Because the THS6022 is a high-speed part, the following guidelines are recommended.

- Ground plane – It is essential that a ground plane be used on the board to provide all components with a low inductive ground connection. Although a ground connection directly to a terminal of the THS6022 is not necessarily required, it is recommended that the thermal pad of the package be tied to ground. This serves two functions. It provides a low inductive ground to the device substrate to minimize internal crosstalk and it provides the path for heat removal.
- Input stray capacitance – To minimize potential problems with amplifier oscillation, the capacitance at the inverting input of the amplifiers must be kept to a minimum. To do this, PCB trace runs to the inverting input must be as short as possible, the ground plane must be removed under any etch runs connected to the inverting input, and external components should be placed as close as possible to the inverting input. This is especially true in the noninverting configuration. An example of this can be seen in Figure 56, which shows what happens when a 1.0 pF capacitor is added to the inverting input terminal in the noninverting configuration. The bandwidth increases dramatically at the expense of peaking. This is because some of the error current is flowing through the stray capacitor instead of the inverting node of the amplifier. While the device is in the inverting mode, stray capacitance at the inverting input has a minimal effect. This is because the inverting node is at a virtual ground and the voltage does not fluctuate nearly as much as in the noninverting configuration. This can be seen in Figure 57, where a 27-pF capacitor adds only 0.5 dB of peaking. In general, as the gain of the system increases, the output peaking due to this capacitor decreases. While this can initally appear to be a faster and better system, overshoot and ringing are more likely to occur under fast transient conditions. So, proper analysis of adding a capacitor to the inverting input node should always be performed for stable operation.

APPLICATION INFORMATION

PCB design considerations (continued)

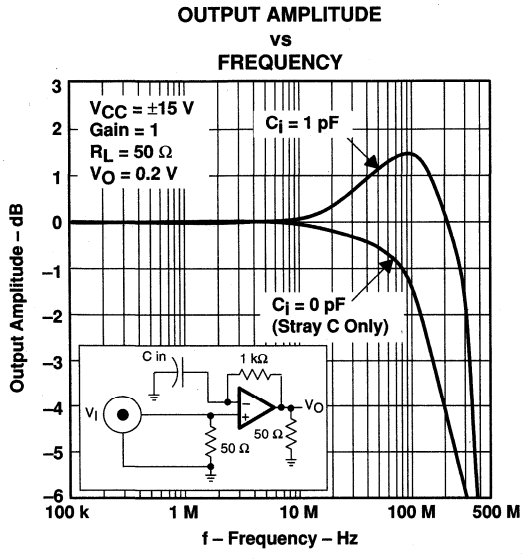


Figure 56

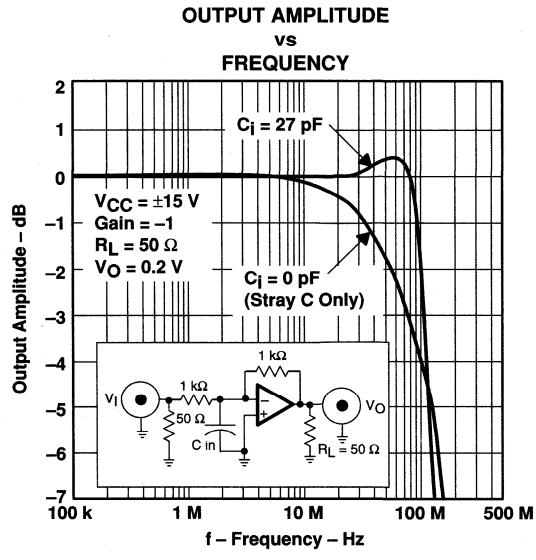


Figure 57

- Proper power supply decoupling – Use a minimum of a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting etch makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminal and the ceramic capacitors.

Because of its power dissipation, proper thermal management of the THS6022 is required. Although there are many ways to properly heatsink this device, the following steps illustrate one recommended approach for a multilayer PCB with an internal ground plane. Refer to Figure 58 for the following steps.

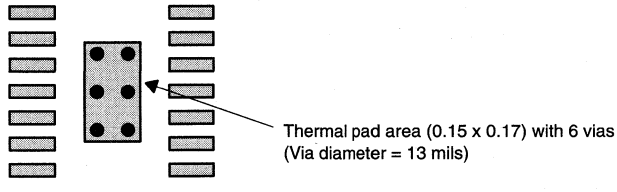


Figure 58. PowerPAD PCB Etch and Via Pattern – Minimum Requirements

APPLICATION INFORMATION

PCB design considerations (continued)

1. Place 6 holes in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
2. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This will help dissipate the heat generated from the THS6022. These additional vias may be larger than the 13 mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal-pad area to be soldered, therefore, wicking is generally not a problem.
3. Connect all holes to the internal ground plane.
4. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS6022 package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated through hole.
5. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area with its 6 holes. The bottom-side solder mask should cover the 6 holes of the thermal pad area. This eliminates the solder from being pulled away from the thermal pad area during the reflow process.
6. Apply solder paste to the exposed thermal pad area and all of the operational amplifier terminals.
7. With these preparatory steps in place, the THS6022 is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

The actual thermal performance achieved with the THS6022 in its PowerPAD package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches $\times$ 3 inches, then the expected thermal coefficient, θ_{JA}, is about 37.5°C/W. For a given θ_{JA}, the maximum power dissipation is shown in Figure 60 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS6022 (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case (2.07°C/W)
θ_{CA} = Thermal coefficient from case to ambient air

APPLICATION INFORMATION

PCB design considerations (continued)

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments technical brief, *PowerPAD Thermally Enhanced Package*. This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

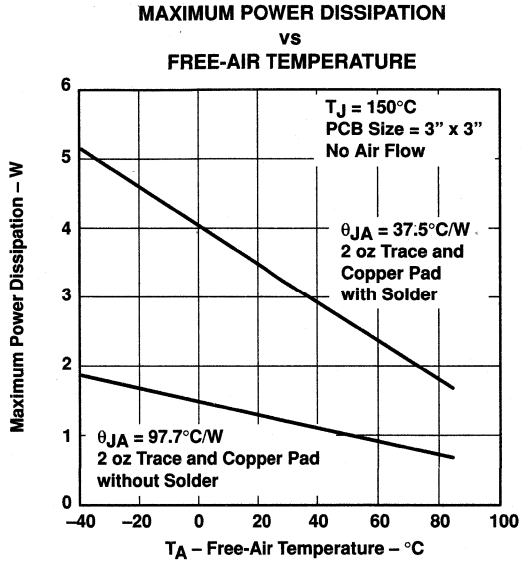


Figure 59. Maximum Power Dissipation vs Free-Air Temperature

APPLICATION INFORMATION

ADSL

The THS6022 was primarily designed as a line driver and line receiver for ADSL (asymmetrical digital subscriber line). The driver output stage has been sized to provide full ADSL power levels of 13 dBm onto the telephone lines. Although actual driver output peak voltages and currents vary with each particular ADSL application, the THS6022 is specified for a minimum full output current of 200 mA at its full output voltage of approximately 12 V. This performance meets the demanding needs of ADSL at the client side end of the telephone line. A typical ADSL schematic is shown in Figure 60.

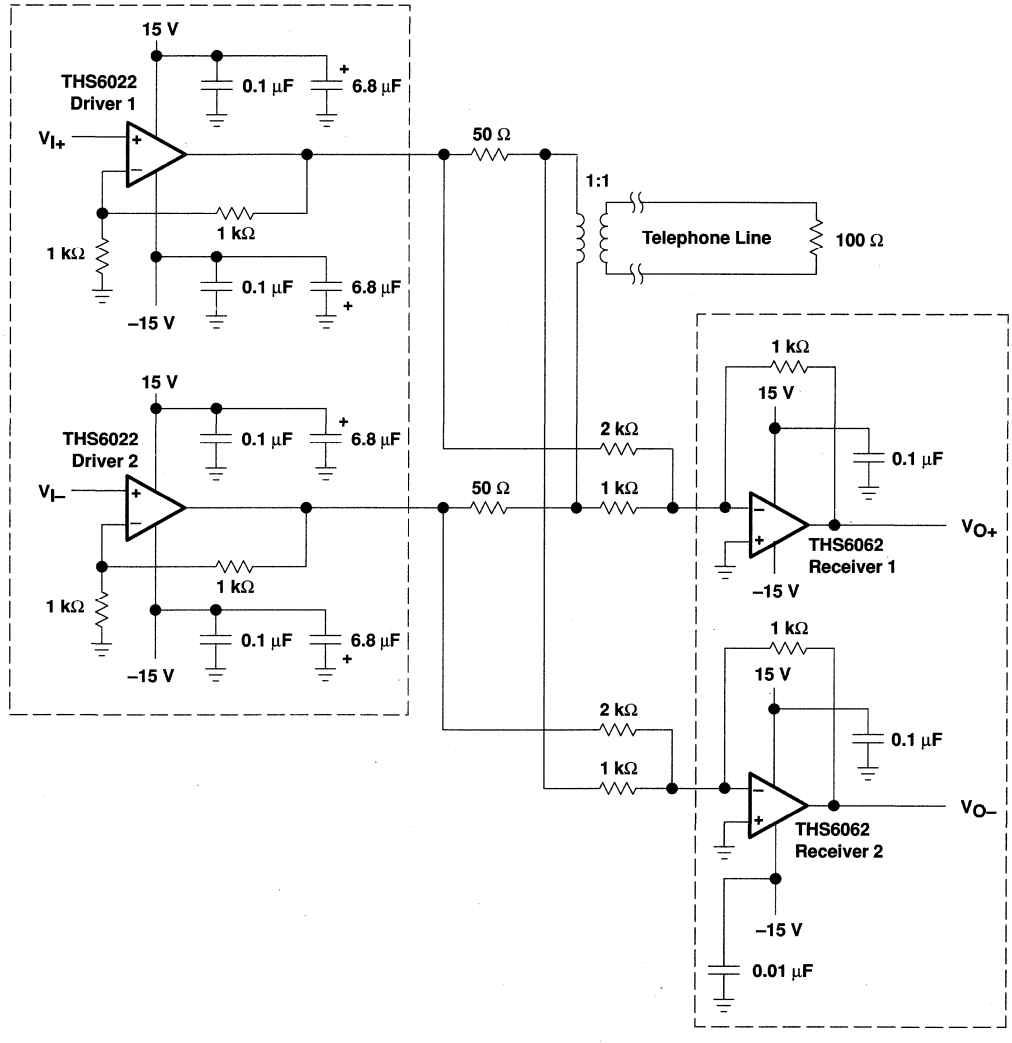


Figure 60. THS6022 ADSL Application

APPLICATION INFORMATION

ADSL (continued)

The ADSL transmit band consists of 255 separate carrier frequencies each with its own modulation and amplitude level. With such an implementation, it is imperative that signals put onto the telephone line have as low a distortion as possible. This is because any distortion either interferes directly with other ADSL carrier frequencies or it creates intermodulation products that interfere with ADSL carrier frequencies.

The THS6022 has been specifically designed for ultra low distortion by careful circuit implementation and by taking advantage of the superb characteristics of the complementary bipolar process. Driver single-ended distortion measurements are shown in Figures 37 – 40. It is commonly known that in the differential driver configuration, the second order harmonics tend to cancel out. Thus, the dominant total harmonic distortion (THD) will be primarily due to the third order harmonics. Additionally, distortion should be reduced as the feedback resistance drops. This is because the bandwidth of the amplifier increases, which allows the amplifier to react faster to any nonlinearities in the closed-loop system.

Another significant point is the fact that distortion decreases as the impedance load increases. This is because the output resistance of the amplifier becomes less significant as compared to the output load resistance. This is illustrated by Figure 40.

One problem that has been receiving a lot of attention in the ADSL area is power dissipation. One way to substantially reduce power dissipation is to lower the power supply voltages. This is because the RMS voltage of an ADSL remote terminal signal is 1.35-V RMS. But, to meet ADSL requirements, the drivers must have a voltage RMS-to-peak crest factor of 5.6 in order to keep the bit-error probability rate below 10^{-7}. Hence, the power supply voltages must be high enough to accomplish the peak output voltage of $1.35\,V \times 5.6 = 7.6\,V_{(PEAK)}$. If ±15-V power supplies are used for the THS6022 drivers in the circuit shown in Figure 61, the power dissipation of the THS6022 is approximately 600 mW. This is assuming that part of the quiescent current is diverted back to the load, which typically happens in a class-AB amplifier. But, if the power supplies are dropped down to ±12 V, then the power dissipation drops to appriximately 460 mW. This is a 23% reduction of power, which ultimately lowers the temperature of the drivers and increases efficiency.

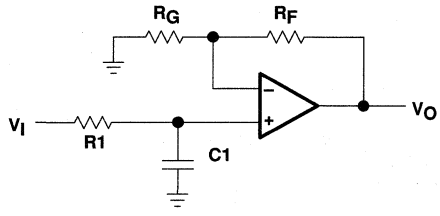
Another way to reduce power dissipation in the drivers is to increase the transformer ratio. The drawback in doing this is that it increases the loading on the drivers and reduces the signals being received from the central office. If this can be overcome, then a power reduction in the drivers will result. By going to a 1:2 transformer ratio, the power supply voltages can drop to ±6 V. The driver output voltage has now been reduced to 675-mV RMS. But, the loading on the output of the drivers drops to 25 Ω. The power dissipated is now approximately 360 mW, a reduction of 22% over the previous example. But, the received signal is now 1/2 of the previous example. This must be dealt with by requiring low-noise receivers. There are always trade offs when it comes to dealing with power, so proper analysis of the system should always be considered.

general configurations

A common error for the first-time CFB user is to create a unity gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration oscillates and is **not** recommended. The THS6022, like all CFB amplifiers, **must** have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a very low impedance. This results in an unstable amplifier and should not be considered when using a current-feedback amplifier. Because of this, integrators and simple low-pass filters, which are easily implemented on a VFB amplifier, have to be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see Figure 62).

APPLICATION INFORMATION

general configurations (continued)

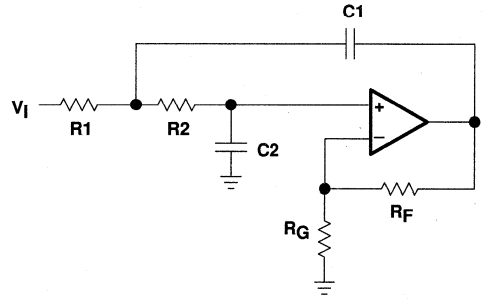


$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

Figure 61. Single-Pole Low-Pass Filter

If a multiple pole filter is required, the use of a Sallen-Key filter can work very well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew-rates and high bandwidths, CFB amplifiers can create very accurate signals and help minimize distortion. An example is shown in Figure 63.



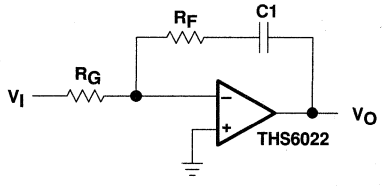
R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 62. 2-Pole Low-Pass Sallen-Key Filter

There are two simple ways to create an integrator with a CFB amplifier. The first one, shown in Figure 64, adds a resistor in series with the capacitor. This is acceptable because at high frequencies, the resistor is dominant and the feedback impedance never drops below the resistor value. The second one, shown in Figure 65, uses positive feedback to create the integration. Caution is advised because oscillations can occur because of the positive feedback.

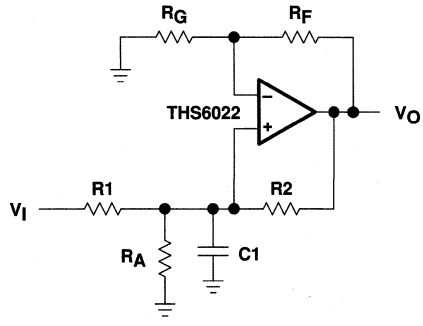


$$\frac{V_O}{V_I} = \left(\frac{R_F}{R_G}\right)\left[\frac{S + \frac{1}{R_F C1}}{S}\right]$$

Figure 63. Inverting CFB Integrator

APPLICATION INFORMATION

general configurations (continued)



For Stable Operation:

$$\frac{R2}{R1 \parallel R_A} \geq \frac{R_F}{R_G}$$

$$V_O \cong V_I \left(\frac{1 + \frac{R_F}{R_G}}{sR1C1} \right)$$

Figure 64. Noninverting CFB Integrator

Another good use for the THS6022 amplifiers is as very good video distribution amplifiers. One characteristic of distribution amplifiers is the fact that the differential phase (DP) and the differential gain (DG) are compromised as the number of lines increases and the closed-loop gain increases. Be sure to use termination resistors throughout the distribution system to minimize reflections and capacitive loading.

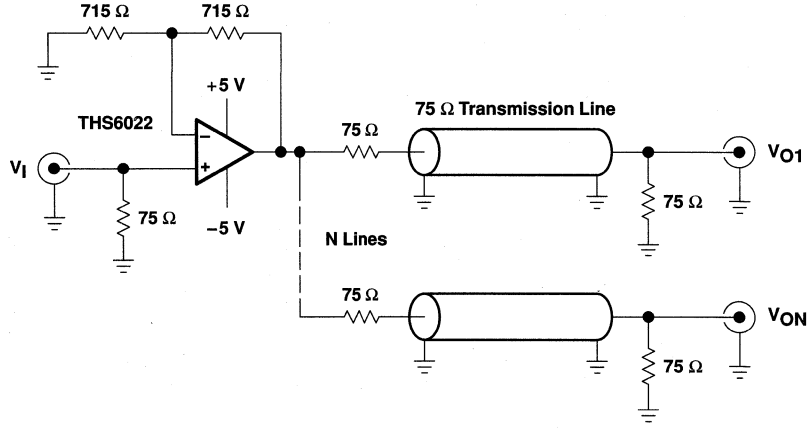


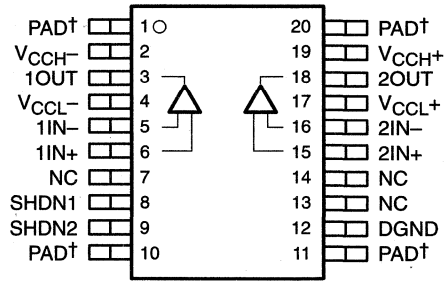
Figure 65. Video Distribution Amplifier Application

evaluation board

An evaluation board is available for the THS6022 (literature number SLOP133). This board has been configured for proper thermal management of the THS6022. The circuitry has been designed for a typical ADSL application as shown previously in this document. For more detailed information, refer to the *THS6022EVM User's Manual* (literature number SLOV035) To order the evaluation board, contact your local TI sales office or distributor.

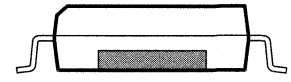
- **Low Power ADSL Line Driver Ideal for Central Office**
  - **1.35-W Total Power Dissipation for Full-Rate ADSL Into a 25-Ω Load**
- **Low-Impedance Shutdown Mode**
  - **Allows Reception of Incoming Signal During Standby**
- **Two Modes of Operation**
  - **Class-G Mode: 4 Power Supplies, 1.35 W Power Dissipation**
  - **Class-AB Mode: 2 Power Supplies, 2 W Power Dissipation**
- **Low Distortion**
  - **THD = –62 dBc at f = 1 MHz, $V_{O(PP)}$ = 20 V, 25-Ω Load**
  - **THD = –69 dBc at f = 1 MHz, $V_{O(PP)}$ = 2 V, 25-Ω Load**
- **400-mA Minimum Output Current Into a 25-Ω Load**
- **High Speed**
  - **65-MHz Bandwidth (–3dB) , 25-Ω Load**
  - **100-MHz Bandwidth (–3dB) , 100-Ω Load**
  - **1200 V/μs Slew Rate**
- **Thermal Shutdown and Short Circuit Protection**
- **Evaluation Module Available**

THERMALLY ENHANCED SOIC (DWP)
PowerPAD™ PACKAGE
(TOP VIEW)



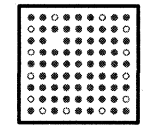
NC – Not Connected

(SIDE VIEW)



Cross section view showing PowerPAD
† This terminal is internally connected to the thermal pad.

MicroStar Junior™ (GQE) PACKAGE
(TOP VIEW)



description

The THS6032 is a low-power line driver ideal for asymmetrical digital subscriber line (ADSL) applications. This device contains two high-current, high-speed current-feedback drivers, which can be configured differentially for driving ADSL signals at the central office. The THS6032 features a unique class-G architecture to lower power consumption to 1.35 W. The THS6032 can also be operated in a traditional class-AB mode to reduce the number of power supplies to two.

HIGH-SPEED xDSL LINE DRIVER/RECEIVER FAMILY

DEVICE	DRIVER	RECEIVER	5 V	±5 V	±15 V	DESCRIPTION
THS6002	•	•		•	•	500-mA differential line driver and receiver
THS6012	•			•	•	500-mA differential line driver
THS6022	•			•	•	250-mA differential line driver
THS6032	•			•	•	500-mA low-power ADSL central-office line driver
THS6062		•	•	•	•	Low-noise ADSL receiver
THS6072		•		•	•	Low-power ADSL receiver
THS7002		•		•	•	Low-noise programmable-gain ADSL receiver

CAUTION: The THS6032 provides ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

PowerPAD and MicroStar Junior are trademarks of Texas Instruments.

description

The class-G architecture supplies current to the load from four supplies. For low output voltages (typically $-2.5 < V_O < +2.5$), some of the output current is supplied from the $+V_{CC(L)}$ and $-V_{CC(L)}$ supplies (typically ±5 V). For large output voltages (typically $V_O < -2.5$ and $V_O > +2.5$), the output current is supplied from $+V_{CC(H)}$ and $-V_{CC(H)}$ (typically ±15 V). This current sharing between $V_{CC(L)}$ and $V_{CC(H)}$ minimizes power dissipation within the THS6032 output stages for high crest factor ADSL signals.

The THS6032 features a low-impedance shutdown mode, which allows the central office to receive incoming calls even after the device has been shut down. The THS6032 is available packaged in the patented PowerPAD package. This package provides outstanding thermal characteristics in a small-footprint surface-mount package, which is fully compatible with automated surface-mount assembly procedures. It is also available in the new MicoStar Junior BGA package. This package is only 25 mm^2 in area, allowing for high density PCB designs.

Shutdown (SHDN1 and SHDN2) allows for powering down the internal circuitry for power conservation or for multiplexing. Separate shutdown controls are available for each channel on the THS6032. The control levels are TTL compatible. When turned off, each driver output is placed in a low impedance state which is determined by the voltage at DGND. This virtual ground at the outputs allows proper termination of a transmission line.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	PACKAGED DEVICES	EVALUATION MODULES
	PowerPAD PLASTIC SMALL OUTLINE (DWP)	MicroStar Junior (BGA) (GQE)	
0°C to 70°C	THS6032CDWP	THS6032CGQE	THS6032EVM THS6032GQE EVM‡
–40°C to 85°C	THS6032IDWP	THS6032IGQE	—

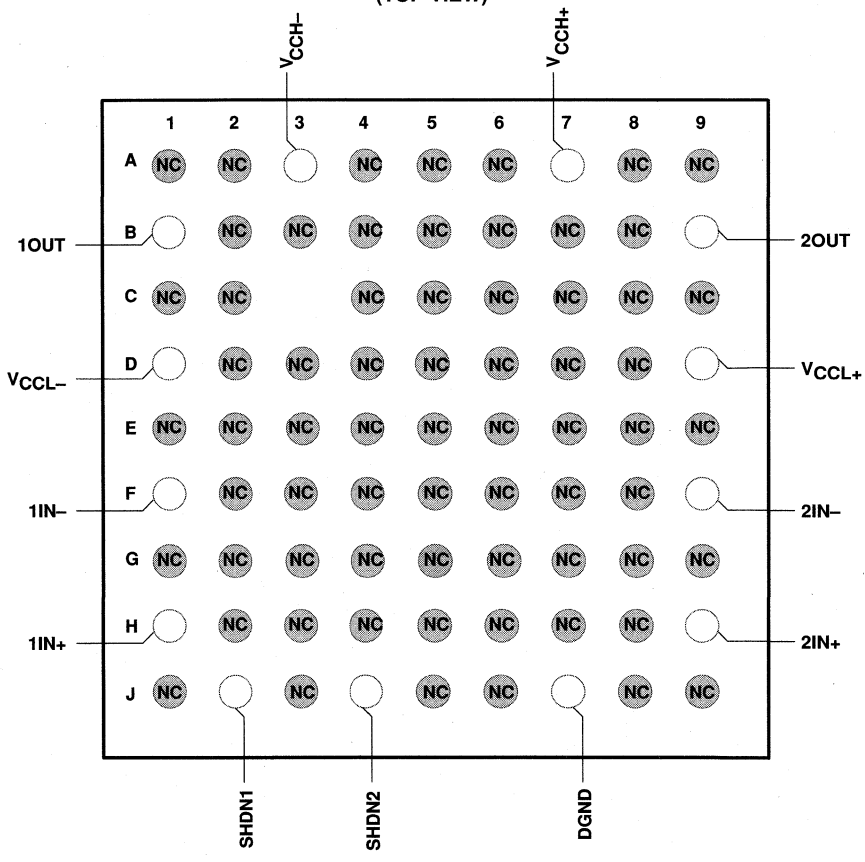
† The THS6032 is available taped and reeled. Add an R suffix to the device type (i.e.,THS6032CDWPR)
‡ Uses the THS6032CGQE packaging option.

Terminal Functions

TERMINAL		
NAME	DWP PACKAGE TERMINAL NO.	GQE PACKAGE TERMINAL NO.
1OUT	3	B1
1IN–	5	F1
1IN+	6	H1
2OUT	18	B9
2IN–	16	F9
2IN+	15	H9
V_{CCH-}	2	A3
V_{CCH+}	19	A7
V_{CCL-}	4	D1
V_{CCL+}	17	D9
SHDN1	8	J2
SHDN2	9	J4
DGND	12	J7
PAD	1, 10, 11, 20	N/A
NC	7, 13, 14	N/A

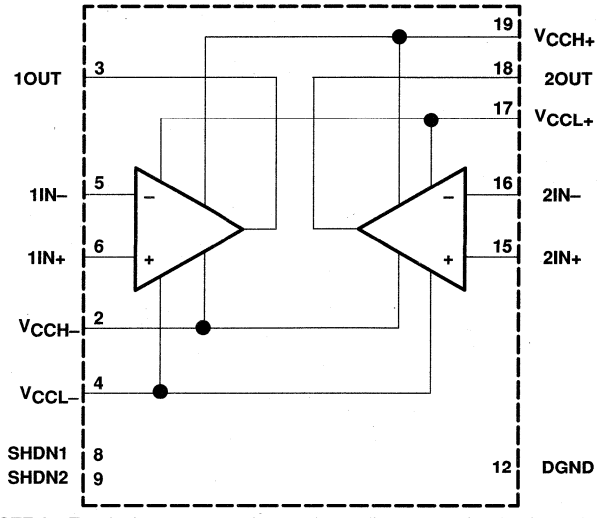
pin assignments

MicroStar Junior™ (GQE) PACKAGE
(TOP VIEW)



NOTE: Shaded terminals are used for thermal connection to the ground plane.

functional block diagram (SOIC package)



NOTE A. Terminals 1, 10, 11, and 20 are internally connected to the thermal pad.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, $V_{CC(L)}$ and $V_{CC(H)}$ (see Note 1) ..... 33 V
Input voltage, V_I ..... $\pm V_{CCH}$
Output current, I_O (see Note 2) ..... 800 mA
Differential input voltage, V_{ID} ..... ±4 V
Total power dissipation at (or below) 25°C free-air temperature
(see Note 2) ..... See Dissipation Rating Table
Maximum junction temperature, T_J ..... 150°C
Operating free-air temperature, T_A, C-suffix ..... 0°C to 70°C
I-suffix ..... −40°C to 85°C
Storage temperature, T_{stg} ..... −65°C to 125°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. $V_{CC(L)}$ must always be less than or equal to $V_{CC(H)}$
2. The THS6032 incorporates a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See the Thermal Information section for more information about utilizing the PowerPAD thermally enhanced packages.

DISSIPATION RATING TABLE‡

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING
DWP	21.5	0.37	5.8 W
GQE	37.8	4.56	3.3 W

‡ This data was taken using 2 oz. trace and copper pad that is soldered directly to a JEDEC standard 4 layer 3 in × 3 in PCB.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage	$V_{CC(L)}$ – Class G mode	±3	±5	$\pm V_{CCH}$	V
	$V_{CC(L)}$ – Class AB mode	0	0	0	V
	$V_{CC(H)}$	±5	±15	±16	V
Operating free-air temperatures, T_A	C-suffix	0		70	°C
	I-suffix	−40		85	

electrical characteristics, $V_{CC(L)} = \pm 5$ V, $V_{CC(H)} = \pm 15$ V, $R_L = 25\,\Omega$, $T_A = 25$°C (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BW	Small signal bandwidth (–3 dB)	Gain = 1, R_F = 1.3 kΩ	R_L = 25 Ω		65		MHz
			R_L = 100 Ω		100		
		Gain = 2, R_F = 1.1 kΩ	R_L = 25 Ω		60		MHz
			R_L = 100 Ω		70		
	Bandwidth for 0.1 dB flatness	Gain = 1			30		MHz
		Gain = 2			25		
	Full power bandwidth†	V_{OPP} = 20 V			19		MHz
SR	Slew rate‡	Gain = 5,	$V_{O(PP)}$ = 20 V		1200		V/µs
t_s	Settling time to 0.1%	Gain = 1, R_L = 25 Ω,	5 V Step		120		ns

† Full power bandwidth = slew rate/2π V_{PEAK}
‡ Slew rate is defined from the 25% to the 75% output levels.

noise/distortion performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	V_O = 20 $V_{(pp)}$, Gain = 5,	f = 1 MHz		−62		dBc
		V_O = 2 $V_{(pp)}$, Gain = 2,	f = 1 MHz		−69		
V_n	Input voltage noise	f = 10 kHz			2.4		nV/√Hz
I_n	Input current noise	f = 10 kHz	I_{n+}		11		nV/√Hz
			I_{n-}		15		
	Differential gain error	Gain = 2, NTSC	R_L = 150 Ω		0.016%		
			R_L = 25 Ω		0.020%		
	Differential phase error	Gain = 2, NTSC	R_L = 150 Ω		0.04°		
			R_L = 25 Ω		0.30°		
	Crosstalk	f = 1 MHz, Gain = 2,	R_F = 1.1 kΩ		−62		dB

electrical characteristics, $V_{CC(L)} = \pm 5$ V, $V_{CC(H)} = \pm 15$ V, $R_L = 25\,\Omega$, $T_A = 25$°C (unless otherwise noted) (continued)

dc performance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Z_{(t)}$	Open loop transimpedance	R_L = 1 kΩ		2		MΩ
V_{IO}	Input offset voltage	T_A = 25°C		1.5	5	mV
		T_A = full range			7	
	Offset voltage drift				10	µV/°C
	Differential offset voltage	T_A = 25°C		0.5	3	mV
		T_A = full range			6	

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IB}	Negative input bias current	T_A = 25°C		1.5	9	µA
		T_A = full range			12	
	Positive input bias current	T_A = 25°C		1.5	9	
		T_A = full range			12	

input characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ICR}	Input common-mode voltage range		±13.2	±13.4		V
CMRR	Common-mode rejection ratio	T_A = full range	64	72		dB
r_i	Input resistance	Inverting terminal		15		Ω
		Non inverting terminal		400		kΩ
	Differential input capacitance			1.4		pF

output characteristics

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	Single-ended	R_L = 25 Ω	±10.5	±11		V
		Differential	R_L = 50 Ω	±21	±22		
I_O	Output current†		R_L = 25 Ω	400	440		mA
I_{SC}	Short-circuit current†				800		mA

† A heat sink is required to keep junction temperature below absolute maximum when an output is heavily loaded or shorted. See "absolute maximum ratings."

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Operating range	V_{CCL}		0	±5	±V_{CCH}	V
		V_{CCH}		±5	±15	±16.5	
I_{CC}	Quiescent current (per amplifier)	V_{CCL}	T_A = 25°C		4.3	5.8	mA
			T_A = full range			6.2	
		V_{CCH}	TA = 25°C		4	5	mA
			T_A = full range			5.5	
PSRR	Power supply rejection ratio	V_{CCL}	TA = 25°C	90	100		dB
			T_A = full range	80			
		V_{CCH}	TA = 25°C	69	80		dB
			T_A = full range	66			

electrical characteristics, $V_{CC(L)}$ = ±5 V, $V_{CC(H)}$ = ±15 V, R_L = 25 Ω, T_A = 25 °C (unless otherwise noted) (continued)

shutdown characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Shutdown voltage for power up	Relative to DGND terminal			0.8	V
V_{IH}	Shutdown voltage for power down	Relative to DGND terminal	2			V
I_{IH}	Shutdown input current-high	$V_{(SHDN)}$ = 5 V		200	300	µA
I_{IL}	Shutdown input current-low	$V_{(SHDN)}$ = 0.5 V		20	40	µA
Z_o	Output impedance (while in shutdown state)	$V_{(SHDN)}$ = 2.5 V, f = 1 MHz		0.5		Ω
I_{CCL}	Supply current (per amplifier) (while in shutdown state)	$V_{(SHDN)}$ = 2.5 V, V_O = 0 V		0.05	0.2	mA
I_{CCH}				2.4	3	

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{dis}	Disable time†			1.1		µS
t_{en}	Enable time†			1.5		µS

† Disable/enable time begins when the logic signal is applied to the shutdown terminal and ends when the supply current has reached half of its final value.

TYPICAL CHARACTERISTICS

OUTPUT AMPLITUDE vs FREQUENCY

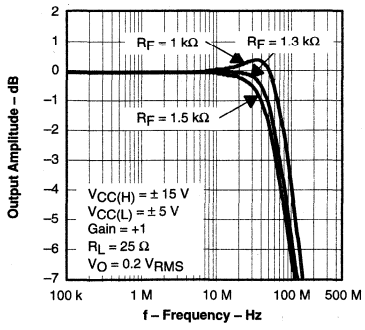


Figure 1

OUTPUT AMPLITUDE vs FREQUENCY

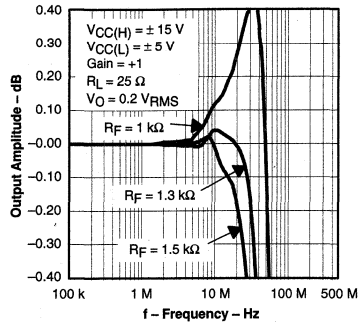


Figure 2

OUTPUT AMPLITUDE vs FREQUENCY

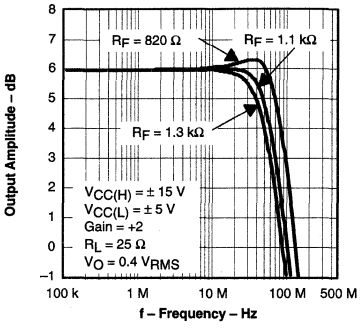


Figure 3

OUTPUT AMPLITUDE vs FREQUENCY

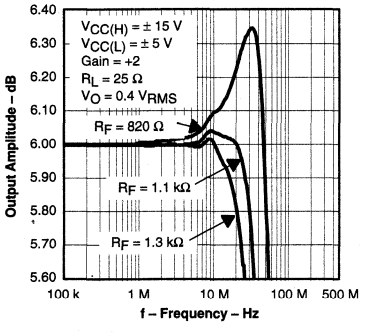


Figure 4

OUTPUT AMPLITUDE vs FREQUENCY

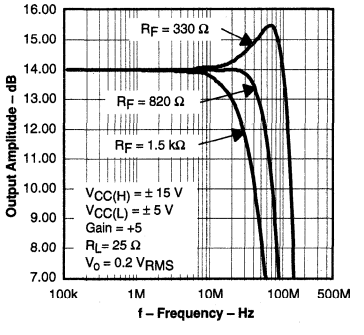


Figure 5

OUTPUT AMPLITUDE vs FREQUENCY

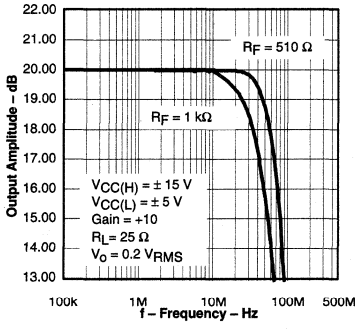


Figure 6

CLASS-AB MODE OUTPUT AMPLITUDE vs FREQUENCY

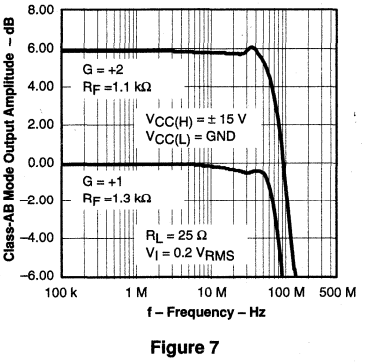


Figure 7

OUTPUT AMPLITUDE vs FREQUENCY

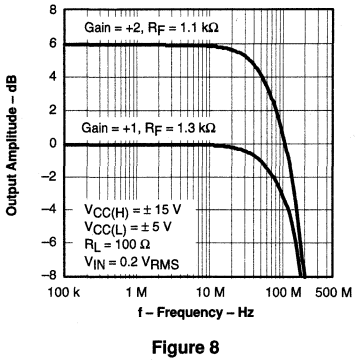


Figure 8

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

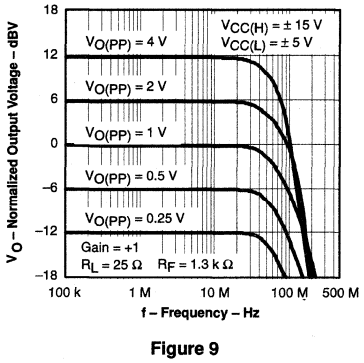


Figure 9

TYPICAL CHARACTERISTICS

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

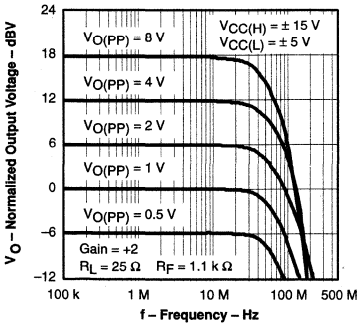


Figure 10

CLASS-G MODE DISTORTION vs FREQUENCY

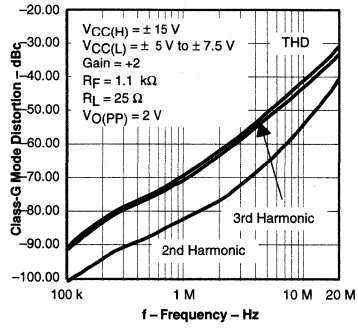


Figure 11

CLASS-AB MODE DISTORTION vs FREQUENCY

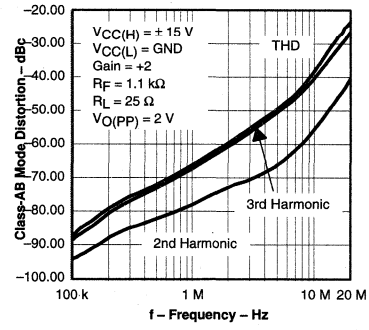


Figure 12

2ND ORDER DISTORTION vs OUTPUT VOLTAGE

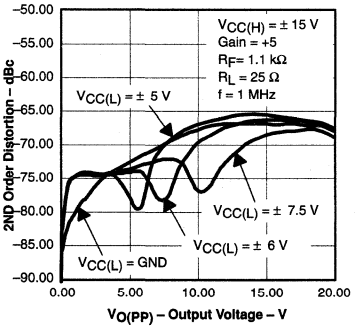


Figure 13

3RD ORDER DISTORTION vs OUTPUT VOLTAGE

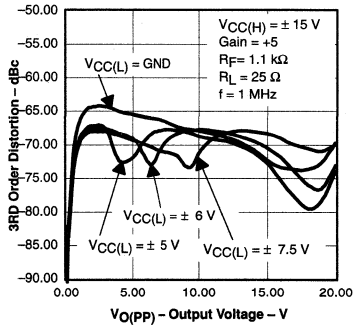


Figure 14

THD vs OUTPUT VOLTAGE

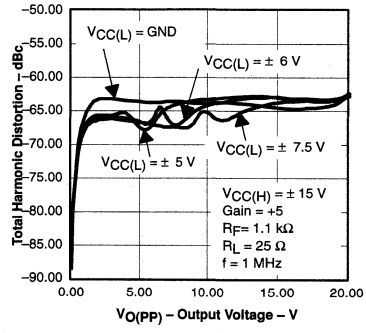


Figure 15

CROSSTALK vs FREQUENCY

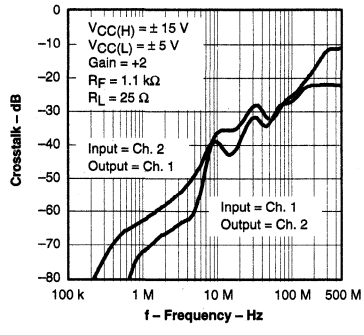


Figure 16

SLEW RATE vs OUTPUT STEP

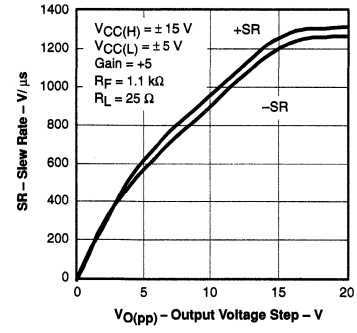


Figure 17

VOLTAGE AND CURRENT NOISE vs FREQUENCY

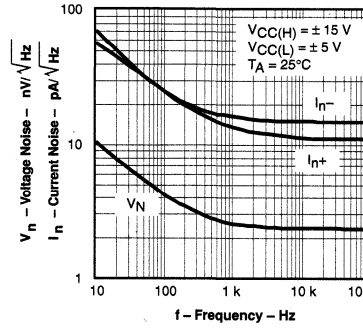


Figure 18

TYPICAL CHARACTERISTICS

TRANSIMPEDANCE vs FREQUENCY

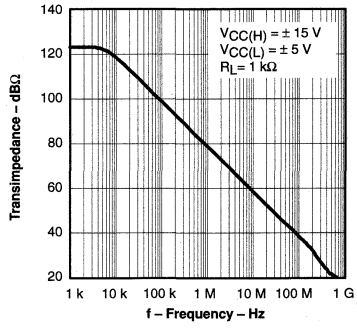


Figure 19

POWER SUPPLY REJECTION RATIO vs FREQUENCY

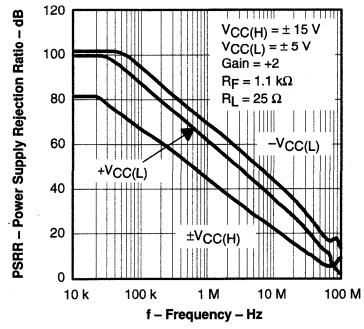


Figure 20

COMMON-MODE REJECTION RATIO vs FREQUENCY

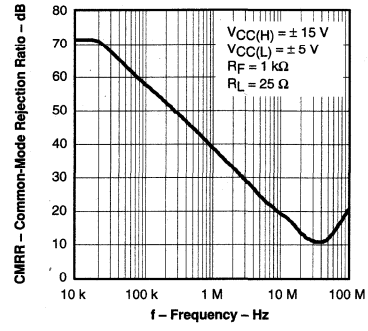


Figure 21

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

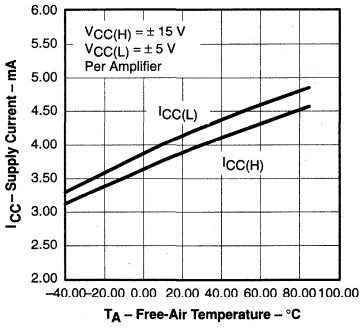


Figure 22

MAXIMUM OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

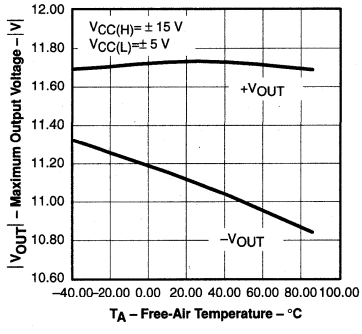


Figure 23

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

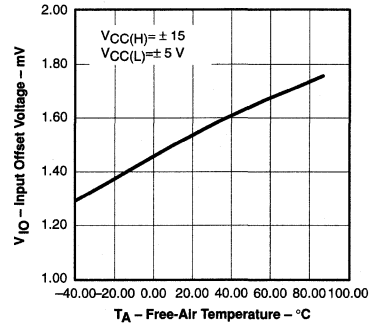


Figure 24

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

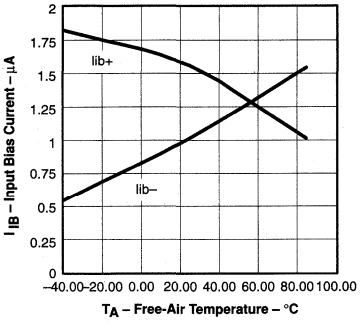


Figure 25

DIFFERENTIAL GAIN vs LOADING

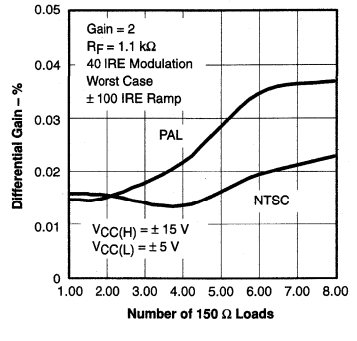


Figure 26

DIFFERENTIAL PHASE vs LOADING

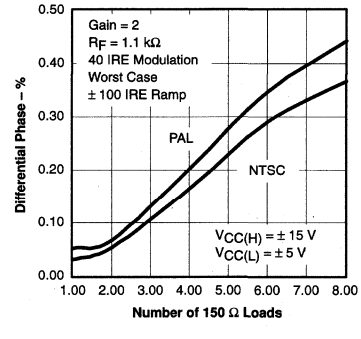


Figure 27

TYPICAL CHARACTERISTICS

CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY

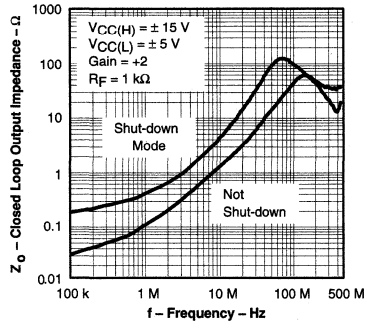


Figure 28

STANDBY SUPPLY CURRENT vs FREE-AIR TEMPERATURE

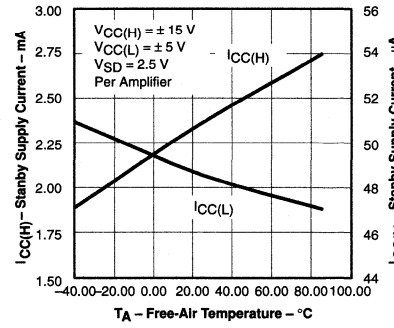


Figure 29

SHUTDOWN ISOLATION vs FREQUENCY

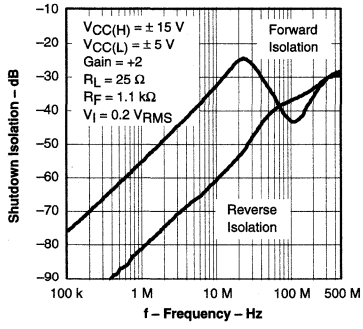


Figure 30

SHUTDOWN ISOLATION vs FREQUENCY

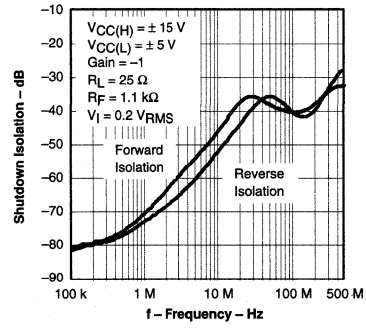


Figure 31

SHUTDOWN RESPONSE

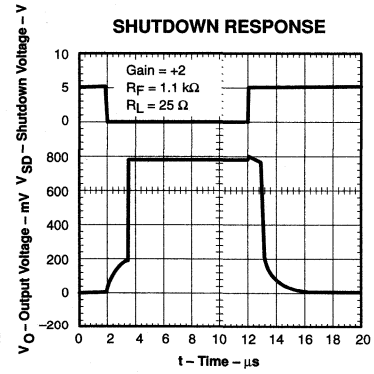


Figure 32

1 VOLT STEP RESPONSE

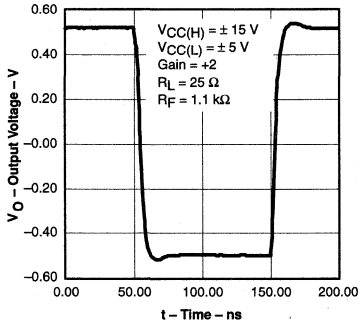


Figure 33

5 VOLT STEP RESPONSE

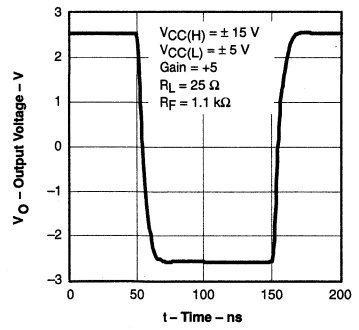


Figure 34

10 V PULSE RESPONSE

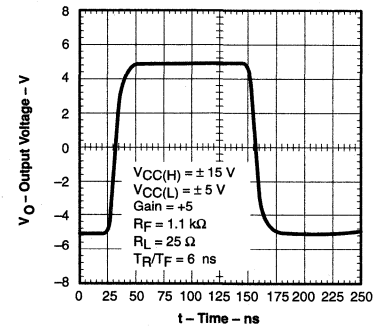


Figure 35

APPLICATION INFORMATION

ADSL

The THS6032 was primarily designed as a low-power line driver for ADSL (asymmetrical digital subscriber line). The driver output stage has been sized to provide full ADSL power levels of 20 dBm onto the telephone lines. Although actual driver output peak voltages and currents vary with each particular ADSL application, the THS6032 is specified for a minimum full output current of 400 mA at its full output voltage of approximately 11 V. This performance meets the demanding needs of ADSL at the central office end of the telephone line. A typical ADSL schematic is shown in Figure 36.

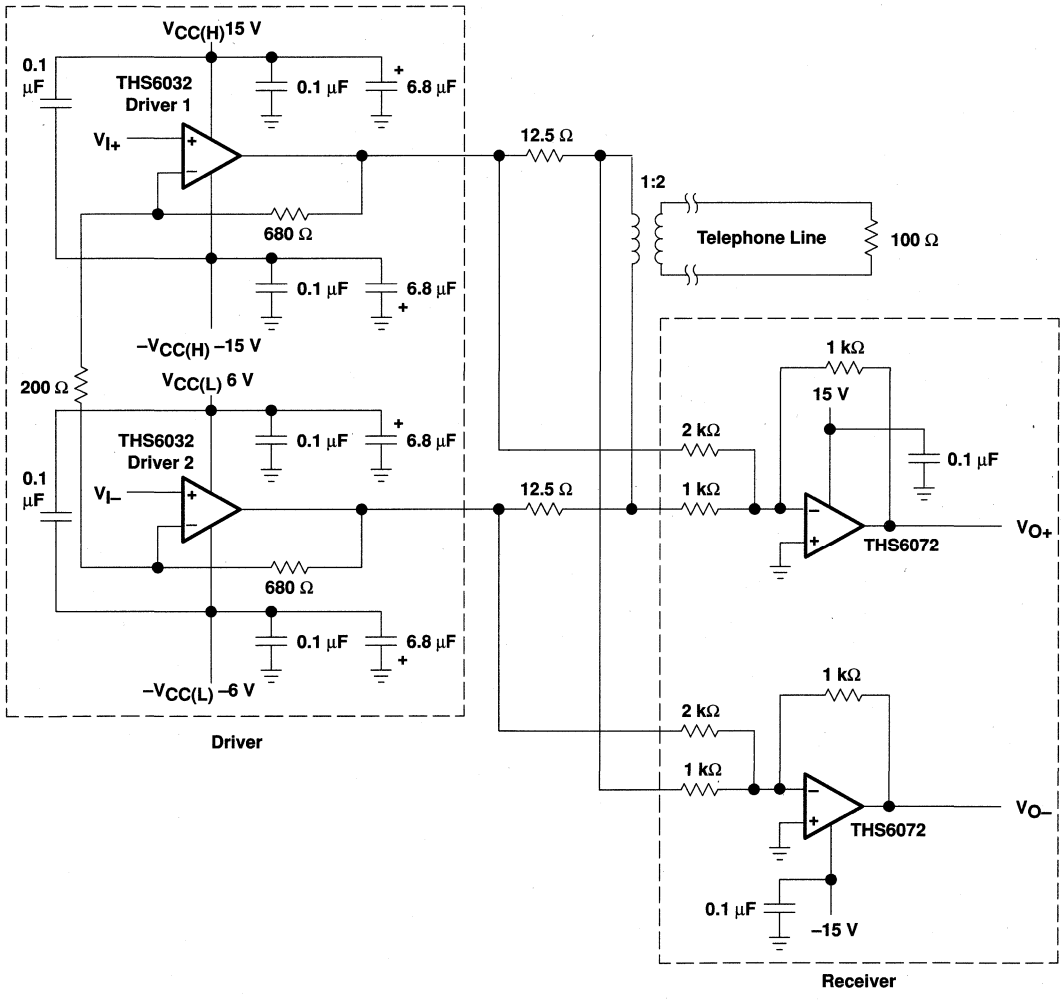


Figure 36. THS6032 ADSL Application

APPLICATION INFORMATION

ADSL (continued)

The ADSL transmit band consists of 255 separate carrier frequencies, each with its own modulation and amplitude level. With such an implementation, it is imperative that signals put onto the telephone line have as low a distortion as possible. This is because any distortion either interferes directly with other ADSL carrier frequencies or it creates intermodulation products that interfere with ADSL carrier frequencies.

The THS6032 has been specifically designed for ultralow distortion by careful circuit implementation and by taking advantage of the superb characteristics of the complementary bipolar process. Driver single-ended distortion measurements are shown in Figures 11 – 15. It is commonly known that in the differential driver configuration, the second order harmonics tend to cancel out. Thus, the dominant total harmonic distortion (THD) will be primarily due to the third order harmonics. Additionally, distortion should be reduced as the feedback resistance drops. This is because the bandwidth of the amplifier increases, which allows the amplifier to react faster to any nonlinearities in the closed-loop system.

Another significant point is the fact that distortion decreases as the impedance load increases. This is because the output resistance of the amplifier becomes less significant as compared to the output load resistance.

One problem that has been receiving a lot of attention in the ADSL area is power dissipation. One way to substantially reduce power dissipation is to lower the power supply voltages. This is because the RMS voltage of an ADSL central office signal is 1.65-V RMS at each driver's output with a 1:2 transformer. But, to meet ADSL requirements, the drivers must have a voltage peak-to-RMS crest factor of 5.6 in order to keep the bit-error probability rate below 10^{-7}. Hence, the power supply voltages must be high enough to accomplish the driver's peak output voltage of $1.65\ V \times 5.6 = 9.25\ V_{(PEAK)}$.

This high peak output voltage requirement, coupled with a low RMS voltage requirement, does not lend itself to conventional high efficiency designs. One way to save power is to decrease the bias currents internal to the amplifier. The drawback of doing this is an increase in distortion and a lower frequency response bandwidth.

This is where the THS6032 class-G architecture is useful. The class-G output stage utilizes both a high supply voltage [$V_{CC(H)}$ typically ±15 V] and a low supply voltage [($V_{CC(L)}$ typically ±6 V]. As long as the output voltage is less than [$V_{CC(L)}$ −2.5 V], then part of the output current will be drawn from the $V_{CC(L)}$ supplies. If the output signal goes above this cutoff point [for example, $V_O > V_{CC(L)} - 2.5$ V], then all of the output current will be supplied by $V_{CC(H)}$.

APPLICATION INFORMATION

ADSL (continued)

To ensure that the cutoff point does not introduce distortion into the system, the entire output stage is always biased on. This constant biasing scheme will cause a decrease in the efficiency over hard switching class-G circuits, but the very low distortion results tend to outweigh the efficiency loss. The biasing scheme used in the THS6032 can be shown by the currents being supplied by the $V_{CC(L)}$ power supplies in Figure 37. This graph shows there is no discrete current transfer point between the $V_{CC(L)}$ supplies and the $V_{CC(H)}$ supplies. This was done to ensure low distortion throughout the entire output range. By changing the $V_{CC(L)}$ supply voltage, the system efficiency can be tailored to suit almost any system with high crest factor requirements.

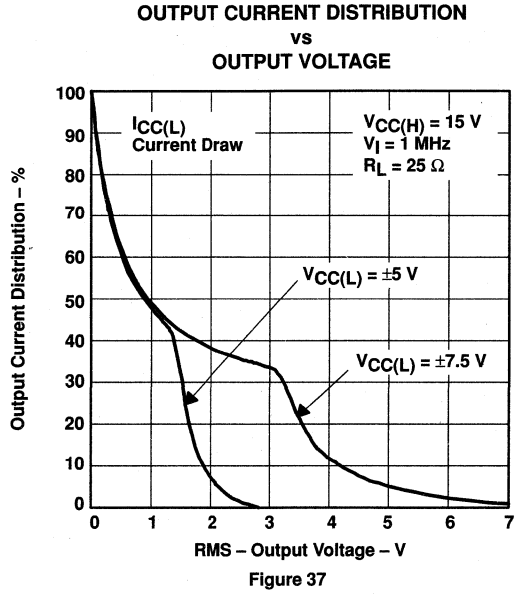


Figure 37

class-AB mode operation

The class-G architecture produces sizable power dissipation savings over traditional class-AB designs while maintaining low distortion requirements. The only drawback to the class-G design is the requirement of 4 power supply voltages, 2 more than a typical line driver requires. In certain instances, the addition of two separate power supplies may be cost prohibitive or PCB space prohibitive. There are two options in this case, use a traditional amplifier, such as a THS6012, or use the THS6032 in class-AB mode.

Using the THS6032 in class-AB mode will give several functional benefits over the THS6012. This includes shutdown capability, low-impedance output while in shutdown state, and a slight reduction in quiescent current. One important thing to remember is that the THS6032 running in class-AB mode, will be only about as efficient as the THS6012. This means that the power dissipation of the THS6032 will increase dramatically and must be accounted for. Failure to do so will result in a part which continuously overheats and may lead to failure.

APPLICATION INFORMATION

class-AB mode operation (continued)

To use the THS6032 in class-AB mode, the user should always connect the $V_{CC(L)}$ power supply pins to GND. The internal $V_{CC(L)}$ paths were not designed for continuous full output current and could possibly fail. The $V_{CC(H)}$ paths were designed for the full output currents and thus, should be used for class-AB mode operation.

The performance of the THS6032 while in class-AB mode is very similar to the class-G mode. Figure 7 and Figures 12 to15 show the THS6032 while in class-AB mode.

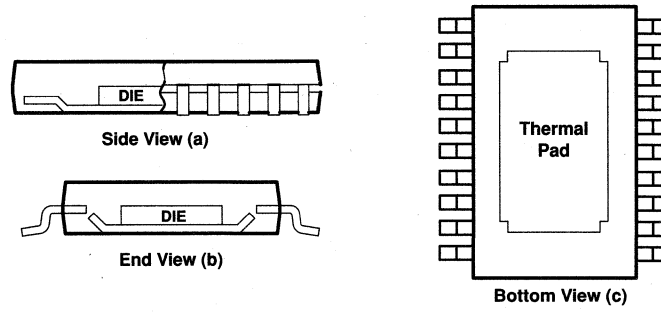
device protection features

The THS6032 has two built-in features that protect the device against improper operation. The first protection mechanism is output current limiting. Should the output become shorted to ground the output current is automatically limited to the value given in the data sheet. While this protects the output against excessive current, the device internal power dissipation increases due to the high current and large voltage drop across the output transistors. Continuous output shorts are not recommended and could damage the device. Additionally, connection of the amplifier output to one of the high supply rails [$\pm V_{CC(H)}$] can cause failure of the device and is not recommended.

The second built-in protection feature is thermal shutdown. Should the internal junction temperature rise above approximately 180°C, the device automatically shuts down. Such a condition could exist with improper heat sinking or if the output is shorted to ground. When the junction temperature drops below 150°C, the internal thermal shutdown circuit automatically turns the device back on.

thermal information

The THS6032 is available in a thermally-enhanced DWP package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 38(a) and Figure 38(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 38(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.



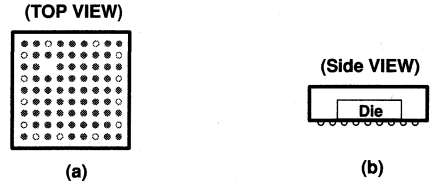
NOTE A. The thermal pad is electrically isolated from all terminals in the package.

Figure 38. Views of Thermally Enhanced DWP Package

APPLICATION INFORMATION

thermal information (continued)

The THS6032 is also available in the MicroStar Junior GQE package. Just like the DWP package, the GQE package utilizes the PowerPAD functionality to improve thermal performance. The GQE package is part of the new ball-grid array (BGA) family developed by Texas Instruments (TI™). This package allows for even higher density layouts with virtually no loss in thermal performance. Its construction is similar to the DWP construction (see Figure 39 (a) and (b)), but utilizes the BGA's to transfer the heat away from the die.



NOTE: Shaded areas are part of the thermally conductive path.

Figure 39. Views of Thermally Enhanced GQE Package

The PowerPAD packages allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads or balls are being soldered), the thermal areas can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device. This is discussed in more detail in the *PCB design considerations* section of this document.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.

Because of its power dissipation, proper thermal management of the THS6032 is required. There are several ways to properly heatsink both the DWP and GQE packages. There are several TI application notes on how to best accomplish the thermal mounting scheme required for each package. For the DWP package, refer to the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package*, literature number SLMA002. There is also a more compact technical paper entitled *PowerPad Made Easy*, literature number SLMA004. For the GQE – MicroStar Junior package, refer to the *MicroStar BGA Packaging Reference Guide*, literature number SSYZ015A and the compact version entitled *MicroStar Junior Made Easy*, literature number SSYA009. This literature is available on TI's web site at http://www.ti.com.

APPLICATION INFORMATION

thermal information (continued)

The actual thermal performance achieved with the THS6032 in its PowerPAD package depends on the application. In the previous example, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA}, is about 21.5°C/W for the DWP package and 37.8°C/W for the GQE package. For a given θ_{JA}, the maximum power dissipation is shown in Figure 40 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS6032 (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case (DWP =0.37°C/W; GQE = 4.56°C/W)
θ_{CA} = Thermal coefficient from case to ambient

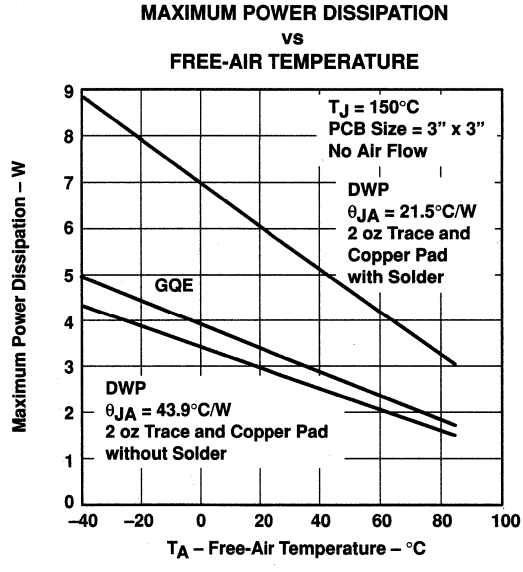


Figure 40. Maximum Power Dissipation vs Free-Air Temperature

APPLICATION INFORMATION

PCB design considerations

Proper PCB design techniques in two areas are important to assure proper operation of the THS6032. These areas are high-speed layout techniques and thermal-management techniques. Because the THS6032 is a high-speed part, the following guidelines are recommended.

- Ground plane – It is essential that a ground plane be used on the board to provide all components with a low inductive ground connection. Although a ground connection directly to a terminal of the THS6032 is not necessarily required, it is recommended that the thermal pad of the package be tied to ground. This serves two functions. It provides a low inductive ground to the device substrate to minimize internal crosstalk and it provides the path for heat removal.
- Input stray capacitance – To minimize potential problems with amplifier oscillation, the capacitance at the inverting input of the amplifiers must be kept to a minimum. To do this, PCB trace runs to the inverting input must be as short as possible, the ground plane must be removed under any etch runs connected to the inverting input, and external components should be placed as close as possible to the inverting input. This is especially true in the noninverting configuration. An example of this can be seen in Figure 41, which shows what happens when a 2.2 pF capacitor is added to the inverting input terminal in the noninverting configuration. The bandwidth increases dramatically at the expense of peaking. This is because some of the error current is flowing through the stray capacitor instead of the inverting node of the amplifier. While the device is in the inverting mode, stray capacitance at the inverting input has a minimal effect. This is because the inverting node is at a virtual ground and the voltage does not fluctuate nearly as much as in the noninverting configuration. This can be seen in Figure 42, where a 27-pF capacitor adds only 2.5 dB of peaking. In general, as the gain of the system increases, the output peaking due to this capacitor decreases. While this can initially appear to be a faster and better system, overshoot and ringing are more likely to occur under fast transient conditions. So, proper analysis of adding a capacitor to the inverting input node should always be performed for stable operation.

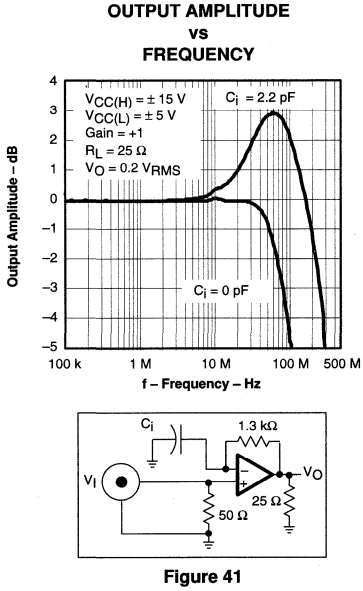


Figure 41

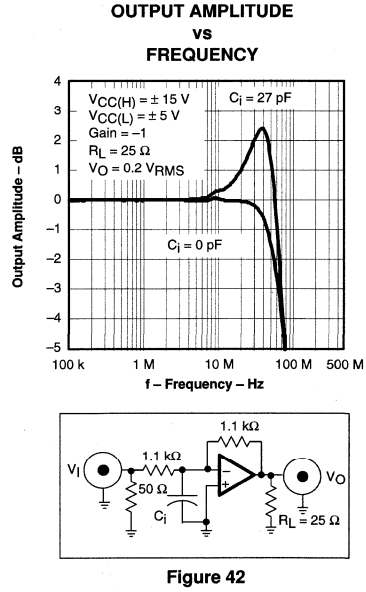


Figure 42

APPLICATION INFORMATION

PCB design considerations (continued)

- Proper power supply decoupling – Use a minimum of a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting etch makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminal and the ceramic capacitors.
- Differential power supply decoupling – The THS6032 was designed for driving low-impedance differential signals. The 25 Ω load which each amplifier drives causes large amounts of currents to flow from amplifier to amplifier. Power supply decoupling for differential current signals must be accounted for to ensure low distortion of the THS6032. By simply connecting a 0.1-μF ceramic capacitor from the $+V_{CC(H)}$ pin to the $-V_{CC(H)}$ pin, along with another 0.1-μF ceramic capacitor from the $+V_{CC(L)}$ pin to the $-V_{CC(L)}$ pin, differential current loops will be minimized (see Figure 36). This will help keep the THS6032 operating at peak performance.

recommended feedback and gain resistor values

As with all current feedback amplifiers, the bandwidth of the THS6032 is an inversely proportional function of the value of the feedback resistor. This can be seen from Figures 1 to 6. The recommended resistors for the optimum frequency response with a 25-Ω load system can be seen in Table 1. These should be used as a starting point and once optimum values are found, 1% tolerance resistors should be used to maintain frequency response characteristics. For most applications, a feedback resistor value of 1.3 kΩ is recommended, which is a good compromise between bandwidth and phase margin that yields a very stable amplifier.

Consistent with current feedback amplifiers, increasing the gain is best accomplished by changing the gain resistor, not the feedback resistor. This is because the bandwidth of the amplifier is dominated by the feedback resistor value and the internal dominant-pole capacitor. The ability to control the amplifier gain independently of the bandwidth constitutes a major advantage of current feedback amplifiers over conventional voltage feedback amplifiers. Therefore, once a frequency response is found suitable to a particular application, adjust the value of the gain resistor to increase or decrease the overall amplifier gain.

Finally, it is important to realize the effects of the feedback resistance on distortion. Increasing the resistance decreases the loop gain and increases the distortion. It is also important to know that decreasing load impedance increases total harmonic distortion (THD). Typically, the third order harmonic distortion increases more than the second order harmonic distortion.

Table 1. Recommended Feedback Resistor Values for 25 Ω Loads

GAIN	R_f
1	1.3 kΩ
2, –1	1.1 kΩ
5	820 Ω
7.8	680 Ω
10	510 Ω

APPLICATION INFORMATION

shutdown control

There are two shutdown pins which control the shutdown for each amplifier of the THS6032. When the shutdown pin signals are low, the THS6032 is active. But, when a shutdown pin is high (≥2 V), the corresponding amplifier is turned off. The shutdown logic is not latched and should always have a signal applied to it. To help ensure a fixed logic state, an internal 50 kΩ resistor to DGND is utilized. An external resistor, such as a 3.3 kΩ, to DGND may be added to help improve noise immunity within harsh environments. If no external resistor is utilized and $SHDN_X$ pins are left unconnected, the THS6032 will default to a power-on state. A simplified circuit can be seen in Figure 43.

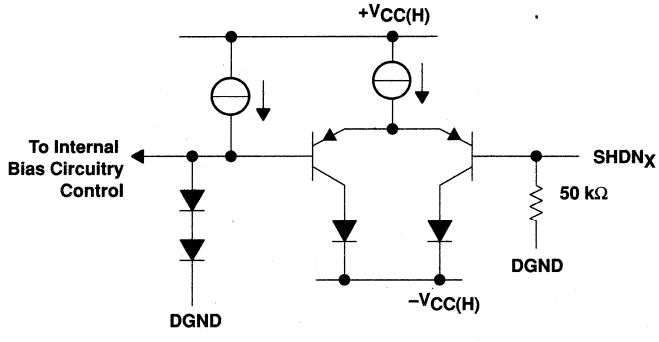


Figure 43. Simplified THS6032 Shutdown Control Circuit

shutdown function

The THS6032 incorporates a shutdown circuit to conserve power. Traditionally when an amplifier is placed into shutdown mode, the input and output circuitry are turned off. This conserves a large amount of power, but the output impedance will be a very high, typically greater than several kΩ. This situation does not allow for proper line termination resulting in a severe reduction of the receive signal coming through the transmission line (see Figure 36).

The THS6032 eliminates this problem. When the $SHDN_X$ pin voltage is greater than 2 V, the THS6032 enters shutdown mode to conserve power. Unlike the traditional amplifier, the THS6032's output impedance is typically 0.5 Ω at 1 MHz (see Figure 28). The shutdown mode function results in the proper termination of the line without degradation in performance of the receive signal coming through the transmission line.

There are a few design considerations in order to fully achieve this type of functionality. To better understand these design considerations, it is helpful to examine what is happening inside the THS6032. Figure 44 shows the simplified shutdown components. Notice that there are two similar input stages; the normal input stage consisting of transistors Q_1 through Q_4 and the shutdown input stage consisting of transistors Q_{S1} through Q_{S4}. When in shutdown mode, the $I_{(BIAS-1)}$ and $I_{(BIAS-2)}$ current sources are turned off. This turns off the normal input stage of the amplifier. The $I_{(BIAS-S1)}$ and $I_{(BIAS-S2)}$ current sources are then turned on. The shutdown input stage signals are then fed through the same internal circuitry which the normal input stage drove. This allows for sinking and sourcing large amounts of current at the output of the THS6032 during shutdown operation. The Q_{S1} through Q_{S4} transistors are not designed for the performance like the Q_1 through Q_4 transistors because their only function is to amplify the DC ground reference, DGND. A 1-kΩ resistor connects internally to the output node of the amplifier, which provides a feedback loop in shutdown mode. This forces the output impedance to become very small, making for proper transmission line termination.

APPLICATION INFORMATION

shutdown function (continued)

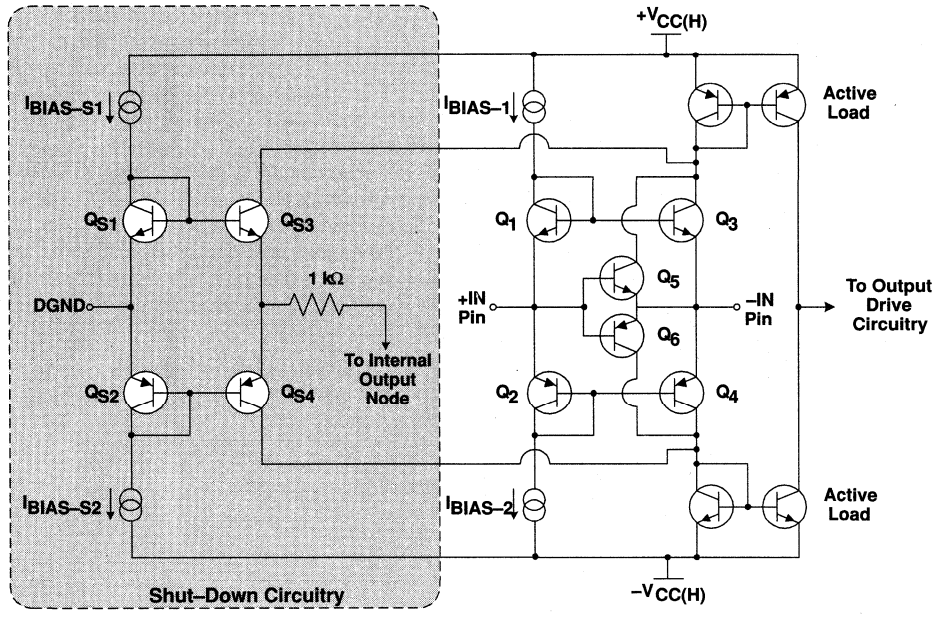


Figure 44. Simplified THS6032 Input Stages

Because the DGND pin voltage is effectively at a noninverting terminal, any signal or voltage fluctuation at this node is amplified by the THS6032. This could possibly cause a noisy output to appear during shutdown operation. Figure 45 shows the frequency response of the THS6032 due to an input signal at the DGND terminal. The maximum DGND voltage signal which the THS6032 will follow linearly during shutdown operation is less than ±4 V. With this dynamic range capability, it is recommended that the DGND pin be as noise-free as possible to ensure proper transmission line termination.

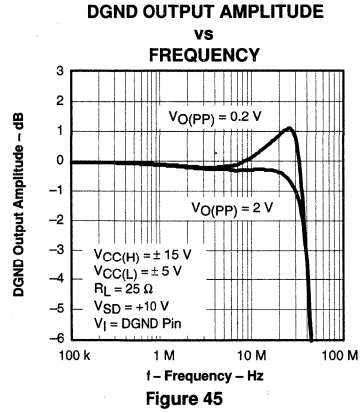


Figure 45

APPLICATION INFORMATION

shutdown function (continued)

The second design consideration is due to transistors Q_5 and Q_6. These transistors ensure the +IN to –IN voltage separation is less than a V_{BE} drop (about 0.7 V). This protects the other transistors, Q_1 to Q_4, from saturating during fast transients. Transistors Q_5 and Q_6 also enhance the slew rate capabilities of the THS6032. When a fast transient is applied to the input, these transistors will quickly apply the currents to the active load stages. A design issue with this setup is that while in shutdown mode, a large enough signal being applied to the input pins may turn on these transistors. Once the input voltage differential between the +IN and –IN pins reaches ±0.7-V, transistors Q_5 and Q_6 turn on applying the difference signal to the rest of the amplifier circuitry. Because these two transistors are designed for much higher performance levels than the shutdown circuitry transistors (Q_{S3} and Q_{S4}), they will become dominant and the difference input signal will be utilized instead of the DGND signal. Because the external negative feedback resistor path is still connected around the amplifier, this difference input signal will be amplified just like a normal amplifier is designed to do (see Figure 46). As long as the +IN and –IN input signals are kept below ±0.7 V, the isolation from input-to-output is very high as shown in the Shutdown Isolation vs Frequency graphs (see Figures 30 and 31).

To ensure proper shutdown functionality of the THS6032, it is important to keep the DGND voltage noise-free. Additionally, the +IN and –IN signals should be limited to less than ±0.7 V during shutdown mode. This will ensure proper line termination functionality while conserving power.

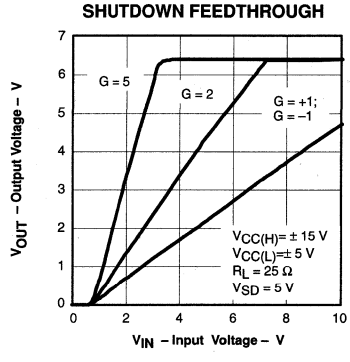


Figure 46

slew rate

The slew rate performance of a current feedback amplifier, like the THS6032, is affected by many different factors. Some of these factors are external to the device, such as amplifier configuration and PCB parasitics, and others are internal to the device, such as available currents and node capacitance. Understanding some of these factors should help the PCB designer arrive at a more optimum circuit with fewer problems.

APPLICATION INFORMATION

slew rate (continued)

Whether the THS6032 is used in an inverting amplifier configuration or a noninverting configuration can impact the output slew rate. Slew rate performance in the inverting configuration is generally faster than the noninverting configuration. This is because in the inverting configuration the input terminals of the amplifier are at a virtual ground and do not significantly change voltage as the input changes. Consequently, the time to charge any capacitance on these input nodes is less than for the noninverting configuration, where the input nodes actually do change in voltage an amount equal to the size of the input step. In addition, any PCB parasitic capacitance on the input nodes degrades the slew rate further simply because there is more capacitance to charge. If the main supply voltage $V_{CC(H)}$ to the amplifier is reduced, slew rate decreases because there is less current available within the amplifier to charge the capacitance on the input nodes as well as other internal nodes. Also, as the load resistance decreases, the slew rate typically decreases due to the increasing internal currents, which slow down the transitions.

Internally, the THS6032 has other factors that impact the slew rate. The amplifier's behavior during the slew rate transition varies slightly depending upon the rise time of the input. This is because of the way the input stage handles faster and faster input edges. Slew rates (as measured at the amplifier output) of less than about 1200 V/µs are processed by the input stage in a very linear fashion. Consequently, the output waveform smoothly transitions between initial and final voltage levels. For slew rates greater than 1200 V/µs, additional slew-enhancing transistors present in the input stage (transistors Q5 and Q6 in Figure 44) begin to turn on to support these faster signals. The result is an amplifier with extremely fast slew rate capabilities. The additional aberrations present in the output waveform with these faster slewing input signals are due to the brief saturation of the internal current mirrors. This phenomenon, which typically lasts less than 20 ns, is considered normal operation and is not detrimental to the device in any way. If for any reason this type of response is not desired, then increasing the feedback resistor or slowing down the input signal slew rate reduces the effect.

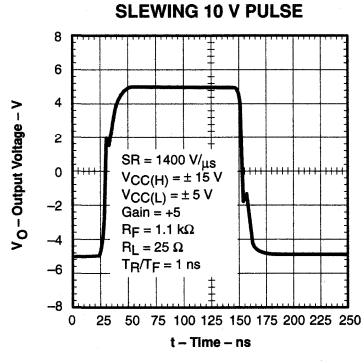


Figure 47

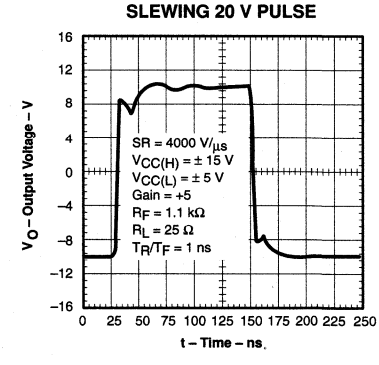


Figure 48

APPLICATION INFORMATION

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true for the amplifying small signals. The noise model for current feedback amplifiers (CFB) is the same as voltage feedback amplifiers (VFB). The only difference between the two is that the CFB amplifiers generally specify different current noise parameters for each input, while VFB amplifiers usually only specify one noise current parameter. The noise model is shown in Figure 49. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = Noninverting current noise (pA/$\sqrt{Hz}$)
- IN– = Inverting current noise (pA/$\sqrt{Hz}$)
- e_{Rx} = Thermal voltage noise associated with each resistor ($e_{Rx} = 4\ kTR_x$)

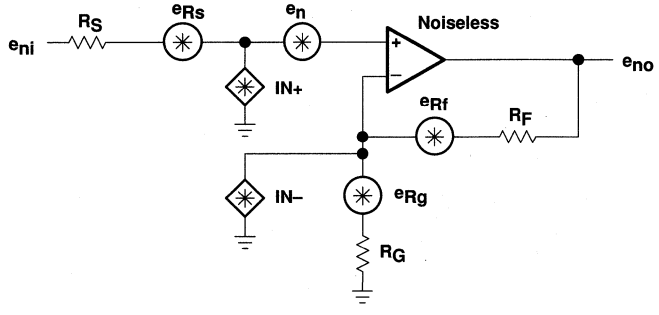


Figure 49. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN + \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\ kTR_S + 4\ kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\ A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)}$$

APPLICATION INFORMATION

noise calculations and noise figure (continued)

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

For more information on noise analysis, please refer to *Noise Analysis in Operational Amplifier Circuits*, literature number SLVA043A

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^{\ 2}}{(e_{Rs})^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\ kTR_S}\right]$$

APPLICATION INFORMATION

noise calculations and noise figure (continued)

Figure 50 shows the noise figure graph for the THS6032.

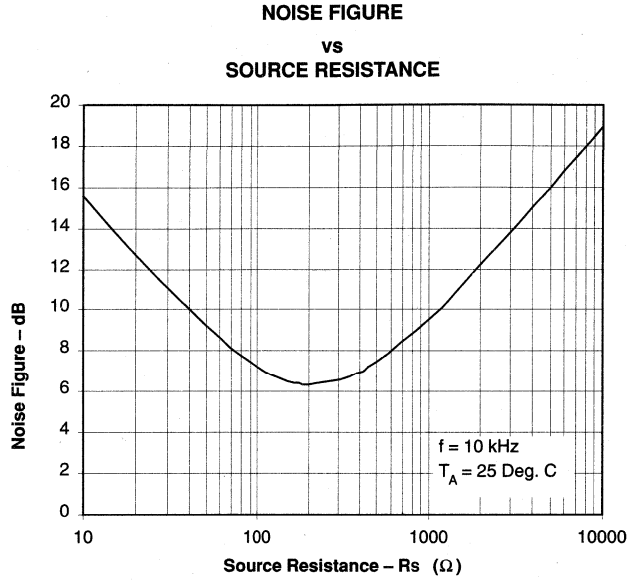
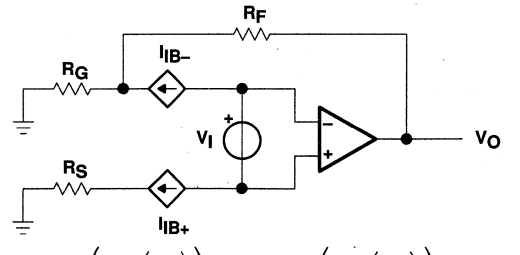


Figure 50. Noise Figure vs Source Resistance

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. Figure 51 can be used to calculate the output offset voltage.



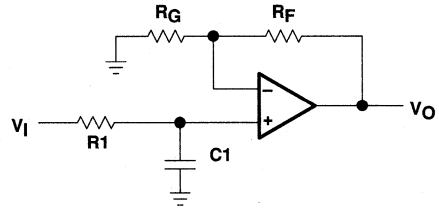
$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\ R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\ R_F$$

Figure 51. Output Offset Voltage Model

APPLICATION INFORMATION

general configurations

A common error for the first-time CFB user is to create a unity gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration oscillates and is not recommended. The THS6032, like all CFB amplifiers, must have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a very low impedance. This results in an unstable amplifier and should not be considered when using a current-feedback amplifier. Because of this, simple low-pass filters, which are easily implemented on a VFB amplifier, have to be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see Figure 52).

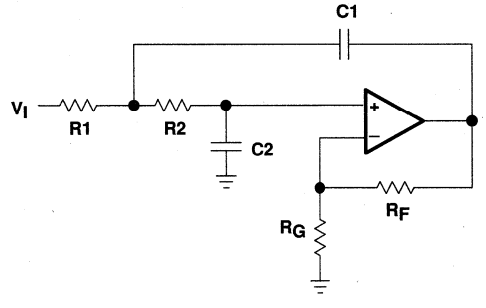


$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

Figure 52. Single-Pole Low-Pass Filter

If a multiple pole filter is required, the use of a Sallen-Key filter can work very well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew-rates and high bandwidths, CFB amplifiers can create very accurate signals and help minimize distortion. One implementation of the Sallen-Key filter is shown in Figure 53. For more information on Sallen-Key filters, refer to the *Analysis of the Sallen-Key Architecture*, literature number SLOA024A.



R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 53. 2-Pole Low-Pass Sallen-Key Filter

Another good use for the THS6032 amplifiers is as video distribution amplifiers. One characteristic of distribution amplifiers is the fact that the differential phase (DP) and the differential gain (DG) are compromised as the number of lines increases and the closed-loop gain increases. Be sure to use termination resistors throughout the distribution system to minimize reflections and capacitive loading.

APPLICATION INFORMATION

general configurations (continued)

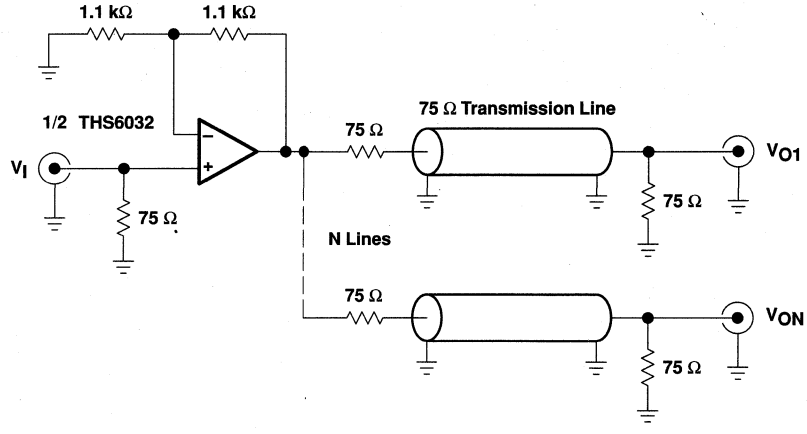


Figure 54. Video Distribution Amplifier Application

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS6032 has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 55. A minimum value of 10 Ω should work well for most applications. For example, in ADSL systems, setting the series resistor value to 12.5 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

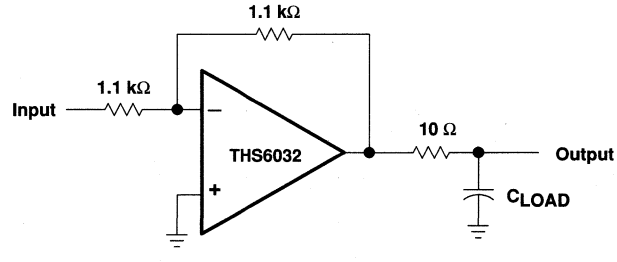


Figure 55. Driving a Capacitive Load

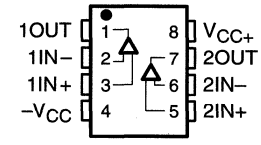
evaluation board

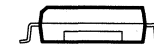
Evaluation boards are available for the THS6032. Each board has been configured for proper thermal management of the THS6032 depending on package selection. The circuitry has been designed for a typical ADSL application as shown previously in this document. To order the evaluation board, contact your local TI sales office or distributor.

SLOS228B – JANUARY 1999 – REVISED JUNE 1999

- **ADSL Differential Receiver**
- **Low 1.6 nV/√Hz Voltage Noise**
- **High Speed**
  - **100 MHz Bandwidth [–3 dB, G = 2 (–1)]**
  - **100 V/μs Slew Rate**
- **90 mA Output Drive (Typ)**
- **Very Low Distortion**
  - **THD = –72 dBc (f = 1 MHz, R_L = 150 Ω)**
  - **THD = –90 dBc (f = 1 MHz, R_L = 1 kΩ)**
- **5 V, ±5 V to ±15 V Typical Operation**
- **Available in Standard SOIC or MSOP PowerPAD™ Package**

D AND DGN PACKAGE
(TOP VIEW)





Cross Section View Showing PowerPAD

description

The THS6062 is a high-speed differential receiver designed for ADSL data communication systems. Its very low 1.6 nV/√Hz voltage noise provides the high signal-to-noise ratios necessary for the long transmission lengths of ADSL systems over copper telephone lines. In addition, this receiver operates with a very low distortion of –90 dBc (f = 1 MHz, R_L = 1 kΩ), exceeding the distortion requirements of ADSL CODECs. The THS6062 is a voltage feedback amplifier offering a high 100-MHz bandwidth and 100-V/μs slew rate and is stable at gains of 2(–1) or greater. It operates over a wide range of power supply voltages including 5 V and ±5 V to ±15 V. This device is available in standard SOIC or MSOP PowerPAD package. The small, surface-mount, thermally-enhanced MSOP PowerPAD package is fully compatible with automated surface-mount assembly procedures.

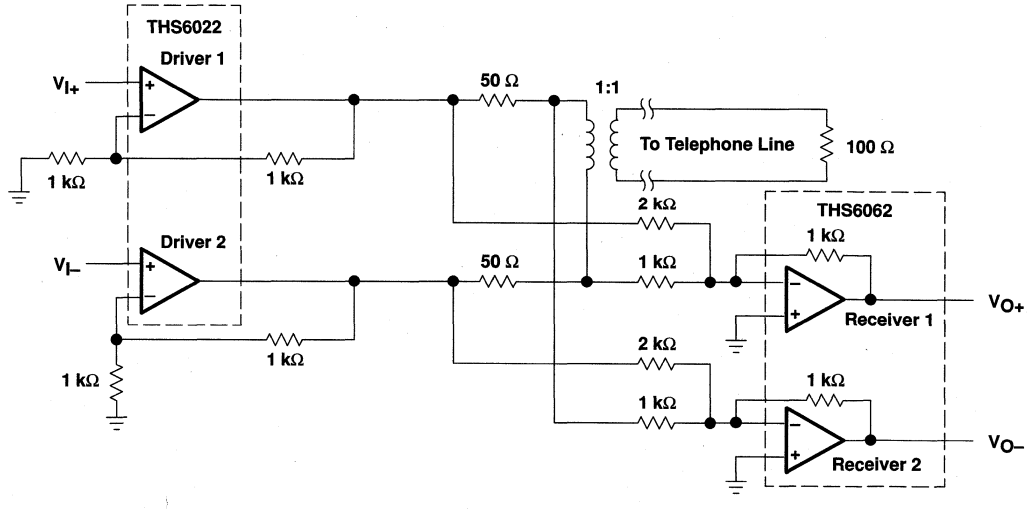


Figure 1. Typical Client-Side ADSL Application

CAUTION: The THS6062 provides ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

PowerPAD is a trademark of Texas Instruments Incorporated.

HIGH-SPEED xDSL LINE DRIVER/RECEIVER FAMILY

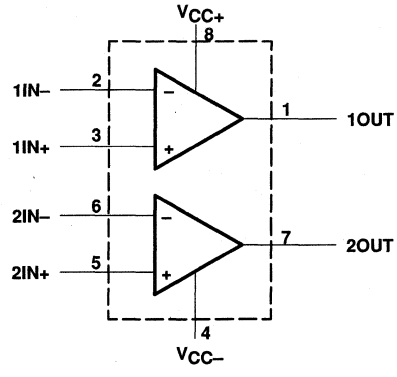
DEVICE	DRIVER	RECEIVER	5 V	±5 V	±15 V	BW (MHz)	SR (V/μs)	THD f = 1 MHz (dB)	I_O (mA)	V_n (nV/√Hz)
THS6002	•	•		•	•	140	1000	–62	500	1.7
THS6012	•			•	•	140	1300	–65	500	1.7
THS6022	•			•	•	210	1900	–66	250	1.7
THS6062		•	•	•	•	100	100	–72	90	1.6
THS7002		•		•	•	70	100	–84	25	2.0

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			
	PLASTIC SMALL OUTLINE† (D)	PowerPAD PLASTIC MSOP† (DGN)	MSOP SYMBOL	EVALUATION MODULE
0°C to 70°C	THS6062CD	THS6062CDGN	TIABE	THS6062EVM
–40°C to 85°C	THS6062ID	THS6062IDGN	TIABH	—

† The D and DGN packages are available taped and reeled. Add an R suffix to the device type (i.e., THS6062CDGNR).

functional block diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC+} to V_{CC-} 33V
Input voltage, V_I ..... $\pm V_{CC}$
Output current, I_O ..... 150 mA
Differential input voltage, V_{IO} ..... ±4 V
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature, T_A: C–suffix ..... 0°C to 70°C
I-suffix ..... –40°C to 85°C
Maximum junction temperature, T_J ..... 150°C
Storage temperature, T_{stg} ..... –65°C to 150°C
Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING
D	167†	38.3	740 mW
DGN‡	58.4	4.7	2.14 W

† This data was taken using the JEDEC standard Low-K test PCB. For the JEDEC Proposed High-K test PCB, the θ_{JA} is 95°C/W with a power rating at T_A = 25°C of 1.32 W.
‡ This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3 in. × 3 in. PC. For further information, refer to *Application Information* section of this data sheet.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} and V_{CC-}	Dual supply	±2.5		±16	V
	Single supply	5		32	
Operating free-air temperature, T_A	C-suffix	0		70	°C
	I-suffix	–40		85	

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage operating range	Dual supply		±2.25		±16.5	V
		Single supply		4.5		33	
I_{CC}	Supply current (per amplifier)	V_{CC} = ±15 V	T_A = 25°C		8.5	10	mA
			T_A = full range			11	
		V_{CC} = ±5 V	T_A = 25°C		7.5	9	
			T_A = full range			10.5	
		V_{CC} = ±2.5 V	T_A = 25°C		7.3	9	
			T_A = full range			10.5	
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.6		V
		V_{CC} = ±5 V		±3.4	±3.8		
		V_{CC} = ±2.5 V		±1	±1.3		
		V_{CC} = ±15 V	R_L = 250 Ω	±12	±12.9		
		V_{CC} = ±5 V	R_L = 150 Ω	±3	±3.5		
		V_{CC} = ±2.5 V		±0.9	±1.2		
I_O	Output current (see Note 1)	V_{CC} = ±15 V	R_L = 20 Ω	60	90		mA
		V_{CC} = ±5 V		50	70		
		V_{CC} = ±2.5 V		40	55		
I_{SC}	Short-circuit current (see Note 1)	V_{CC} = ±15 V			150		mA
V_{IO}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		1.5	6	mV
			T_A = full range			8	
	Offset drift	V_{CC} = ±5 V or ±15 V	T_A = full range		20		µV/°C
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		3	6	µA
			T_A = full range			8	
I_{OS}	Input offset current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		30	250	nA
			T_A = full range			400	
	Offset current drift	V_{CC} = ±5 V or ±15 V	T_A = full range		0.3		nA/°C
CMRR	Common mode rejection ratio	V_{CC} = ±15 V, V_{ICR} = ±12 V	T_A = 25°C	85	95		dB
			T_A = full range	80			
		V_{CC} = ±5 V, V_{ICR} = ±2.5 V	T_A = 25°C	90	100		
			T_A = full range	85			
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	85	95		dB
			T_A = full range	80			

† Full range = 0°C to 70°C for the THS6062C and –40°C to 85°C for the THS6062I.

NOTE 1: Observe power dissipation ratings to keep the junction temperature below absolute maximum ratings when the output is heavily loaded or shorted. See the absolute maximum ratings section for more information.

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V		±13.5	±14.3		V
		V_{CC} = ±5 V		±3.8	±4.3		
		V_{CC} = ±2.5 V		±1.4	±1.8		
R_I	Input resistance				2		MΩ
C_i	Input capacitance				1.5		pF
R_O	Output resistance	Open loop			13		Ω
	Open loop gain	V_{CC} = ±15 V, V_O = ±10 V, R_L = 1 kΩ	T_A = 25°C	40	70		V/mV
			T_A = full range	35			
		V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 1 kΩ	T_A = 25°C	35	50		V/mV
			T_A = full range	30			

† Full range = 0°C to 70°C for the THS6062C and –40°C to 85°C for the THS6062I.

operating characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
SR	Slew rate (see Note 2)	V_{CC} = ±15 V	Gain = –1		100		V/μs
		V_{CC} = ±5 V			80		
		V_{CC} = ±2.5 V			70		
t_s	Settling time to 0.1%	V_{CC} = ±15 V, 5-V step	Gain = –1		60		ns
		V_{CC} = ±5 V, 2.5-V step			45		
		V_{CC} = ±2.5 V, 1-V step			35		
	Settling time to 0.01%	V_{CC} = ±15 V, 5-V step	Gain = –1		90		ns
		V_{CC} = ±5 V, 2.5-V step			80		
		V_{CC} = ±2.5 V, 1-V step			75		
THD	Total harmonic distortion	V_{CC} = ±5 V or ±15 V, $V_{O(pp)}$ = 2 V, f = 1 MHz, Gain = 2	R_L = 150 Ω		–72		dBc
			R_L = 1 kΩ		–90		
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V, f = 10 kHz			1.6		nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V, f = 10 kHz			1.2		pA/√Hz
BW	Dynamic performance small-signal bandwidth (–3 dB)	V_{CC} = ±15 V	$V_{O(pp)}$ = 0.4 V, Gain = 2, –1		100		MHz
		V_{CC} = ±5 V			90		
		V_{CC} = ±2.5 V			85		
	Bandwidth for 0.1 dB flatness	V_{CC} = ±15 V	$V_{O(pp)}$ = 0.4 V, Gain = 2, –1		50		
		V_{CC} = ±5 V			45		
		V_{CC} = ±2.5 V			40		
	Full power bandwidth (see Note 3)	$V_{O(pp)}$ = 20 V, V_{CC} = ±15 V	R_L = 1 kΩ		1.6		MHz
		$V_{O(pp)}$ = 5 V, V_{CC} = ±5 V			5		
	Channel-to-channel crosstalk	V_{CC} = ±5 V or ±15 V, f = 1 MHz, Gain = 2			–61		dBc

† Full range = 0°C to 70°C for the THS6062C and –40°C to 85°C for the THS6062I.

NOTES: 2. Slew rate is measured from an output level range of 25% to 75%.

3. Full power bandwidth = slew rate /2 π $V_{(peak)}$

PARAMETER MEASUREMENT INFORMATION

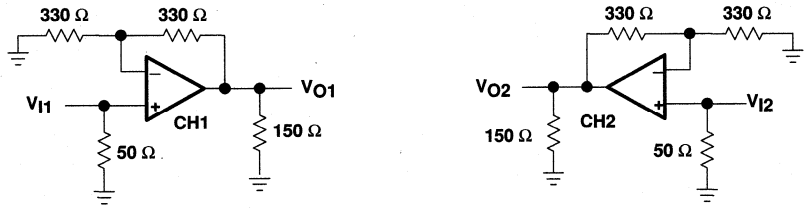


Figure 2. THS6062 Crosstalk Test Circuit

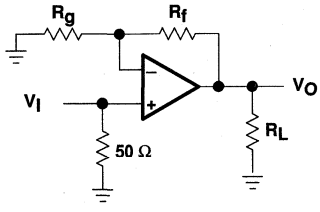


Figure 3. Step Response Test Circuit

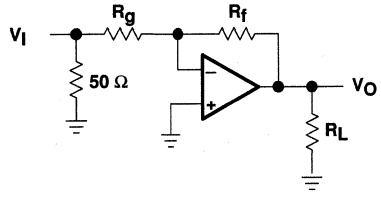


Figure 4. Step Response Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	vs Free-air temperature	5
I_{IB}	Input bias current	vs Free-air temperature	6
V_O	Output voltage	vs Supply voltage	7
	Maximum output voltage swing	vs Free-air temperature	8
I_O	Maximum output current	vs Free-air temperature	9
I_{CC}	Supply current	vs Free-air temperature	10
V_{IC}	Common-mode input voltage	vs Supply voltage	11
Z_O	Closed-loop output impedance	vs Frequency	12
	Open-loop gain		13
	Phase response		13
PSRR	Power-supply rejection ratio	vs Frequency	14
CMRR	Common-mode rejection ratio	vs Frequency	15
	Crosstalk	vs Frequency	16
	Harmonic distortion	vs Frequency	17, 18
	Harmonic distortion	vs Peak-to-peak output voltage	19, 20
SR	Slew rate	vs Free-air temperature	21
	0.1% settling time	vs Output voltage step size	22
	Output amplitude	vs Frequency	23–29
	Small and large frequency response		30–33
	1-V step response		34, 35
	4-V step response		36
	20-V step response		37

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

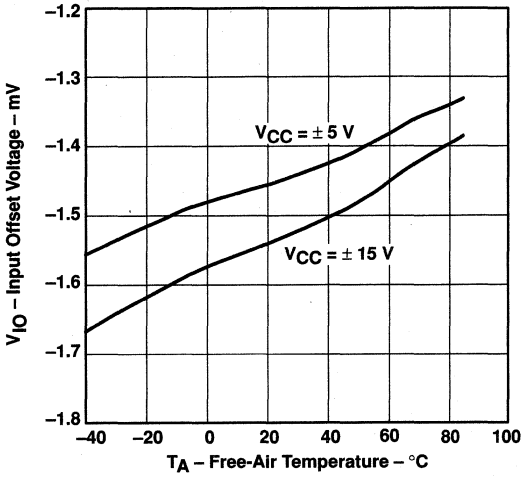


Figure 5

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

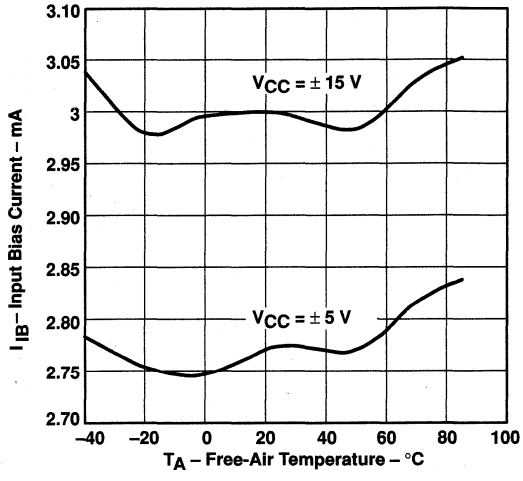


Figure 6

OUTPUT VOLTAGE vs SUPPLY VOLTAGE

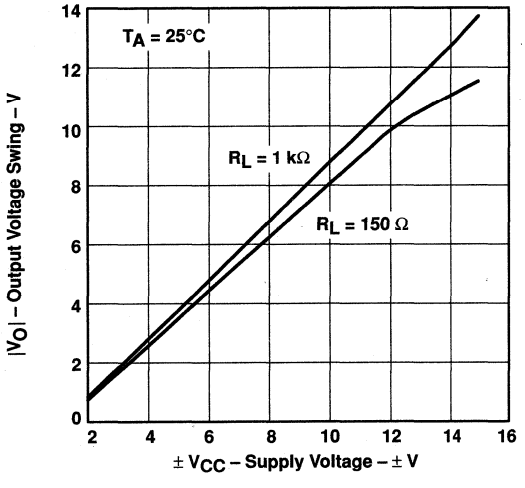


Figure 7

MAXIMUM OUTPUT VOLTAGE SWING vs FREE–AIR TEMPERATURE

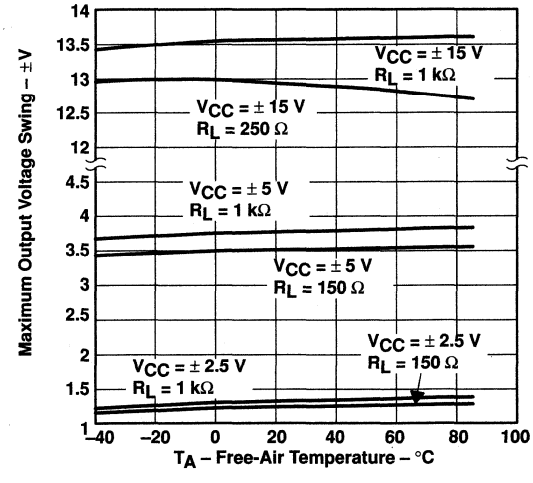


Figure 8

TYPICAL CHARACTERISTICS

MAXIMUM OUTPUT CURRENT vs FREE-AIR TEMPERATURE

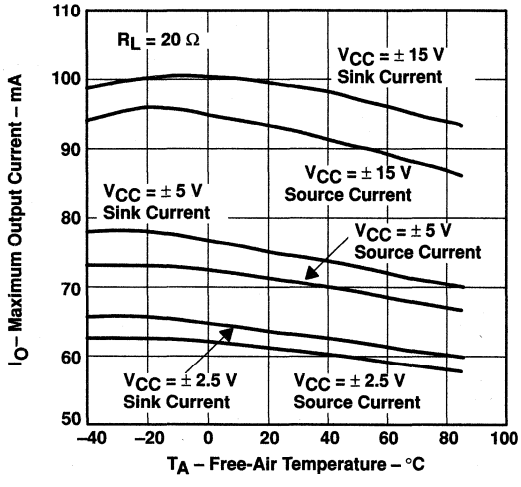


Figure 9

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

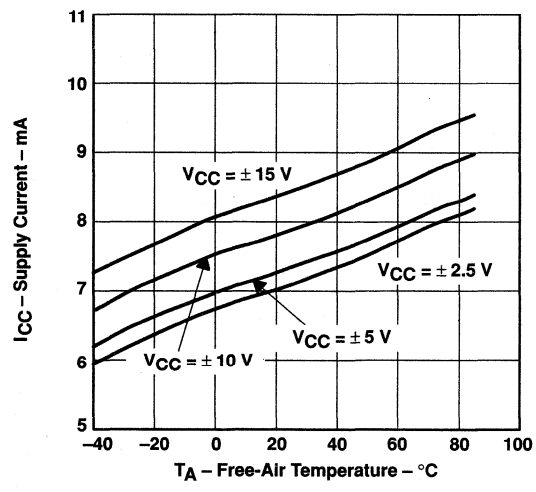


Figure 10

COMMON-MODE INPUT VOLTAGE vs SUPPLY VOLTAGE

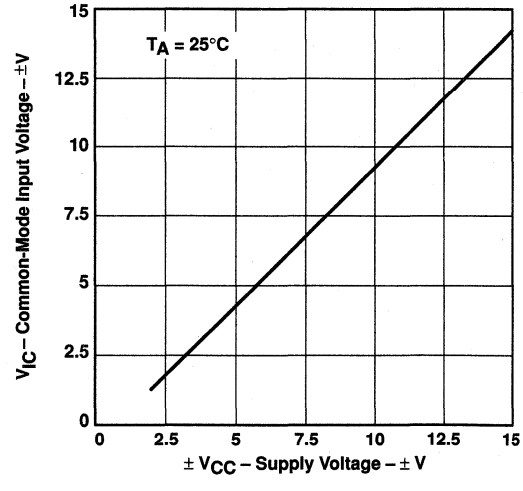


Figure 11

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

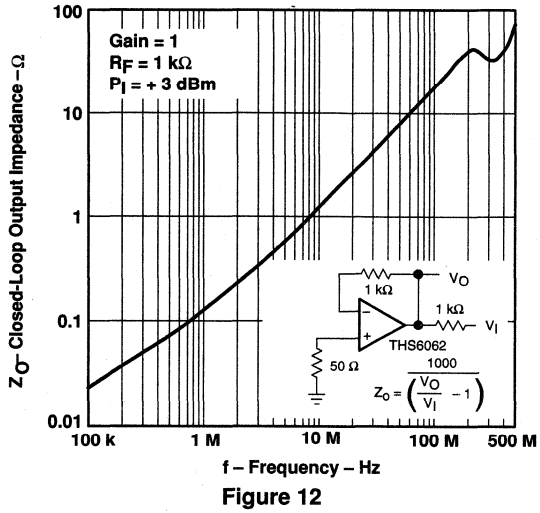


Figure 12

TYPICAL CHARACTERISTICS

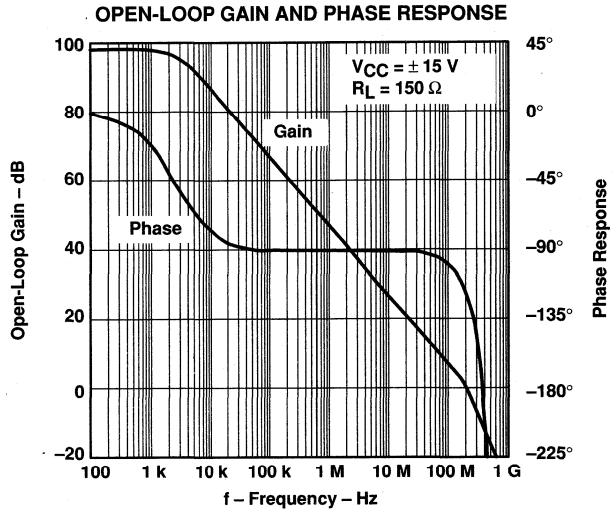


Figure 13

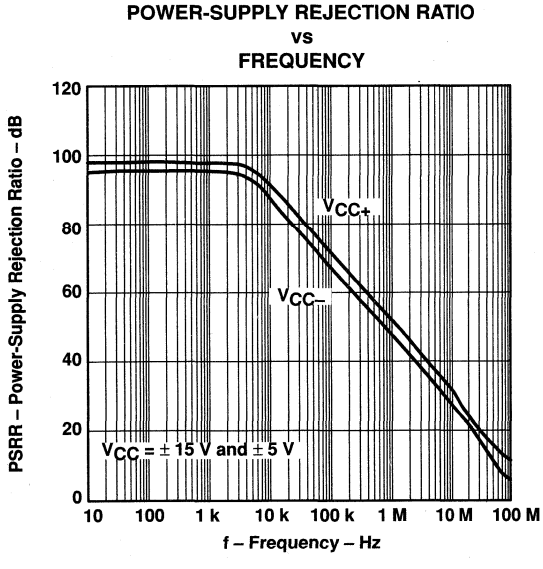


Figure 14

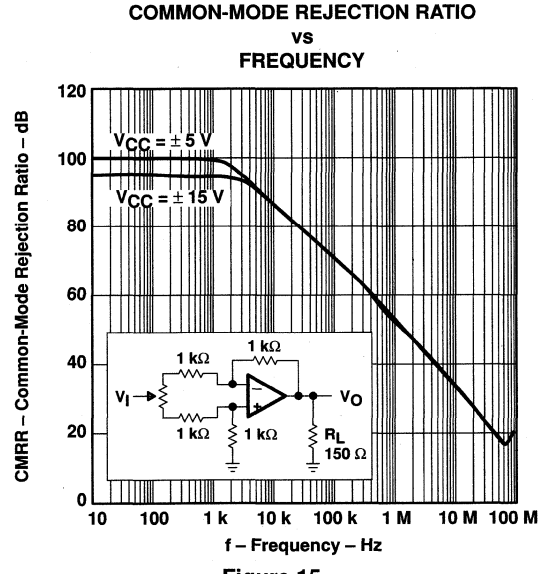


Figure 15

TYPICAL CHARACTERISTICS

CROSSTALK
vs
FREQUENCY

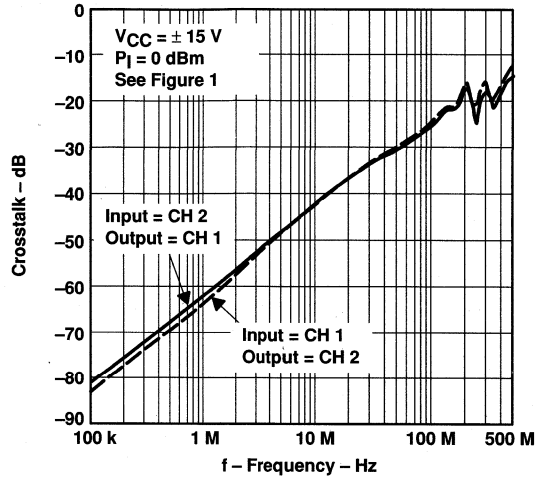


Figure 16

HARMONIC DISTORTION
vs
FREQUENCY

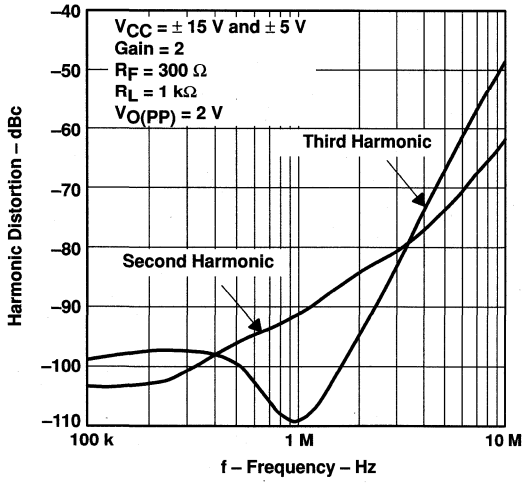


Figure 17

HARMONIC DISTORTION
vs
FREQUENCY

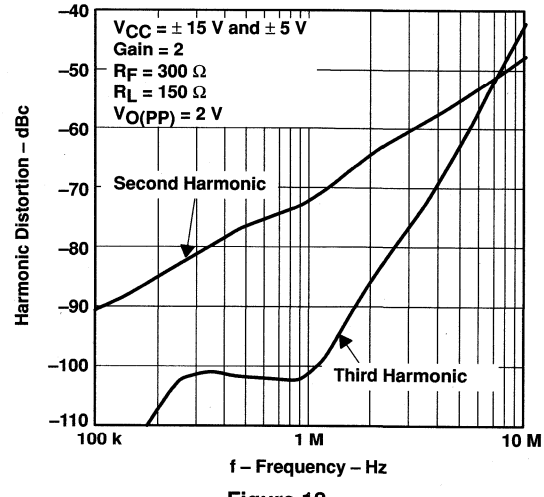


Figure 18

TYPICAL CHARACTERISTICS

HARMONIC DISTORTION
vs
PEAK-TO-PEAK OUTPUT VOLTAGE

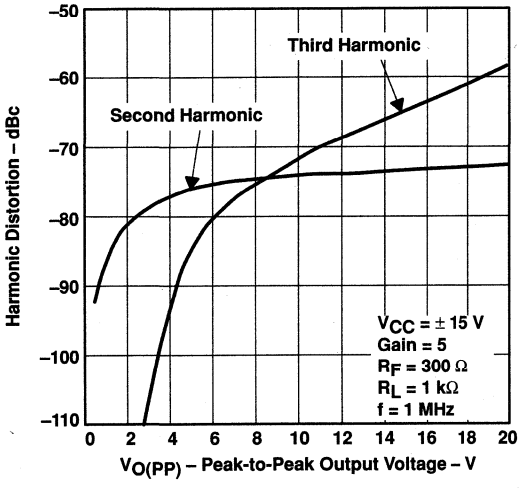


Figure 19

HARMONIC DISTORTION
vs
PEAK-TO-PEAK OUTPUT VOLTAGE

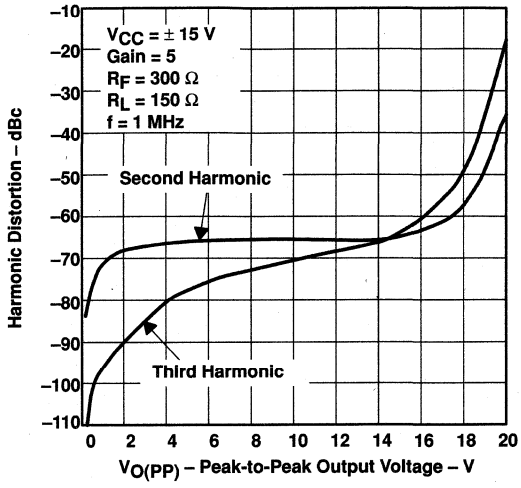


Figure 20

SLEW RATE
vs
FREE-AIR TEMPERATURE

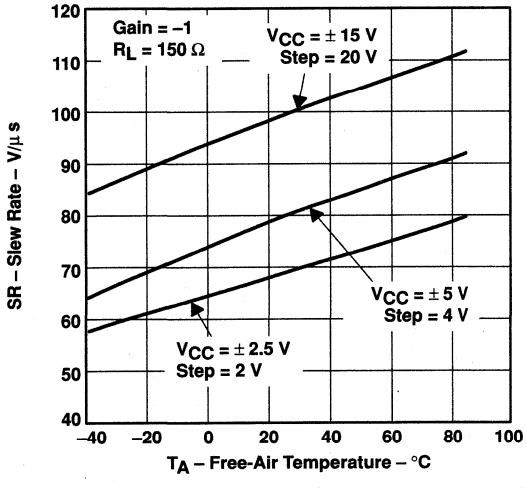


Figure 21

0.1% SETTLING TIME
vs
OUTPUT VOLTAGE STEP SIZE

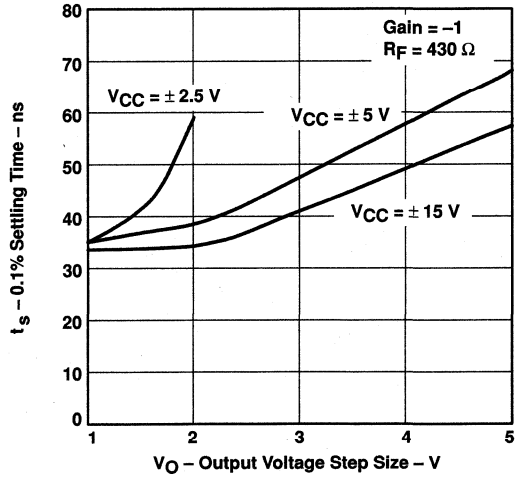


Figure 22

TYPICAL CHARACTERISTICS

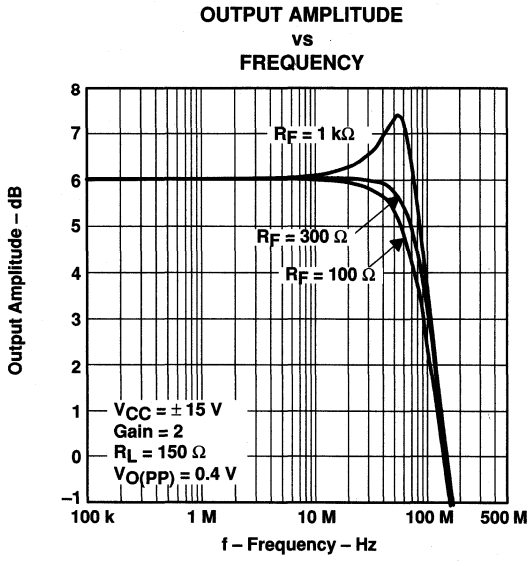


Figure 23

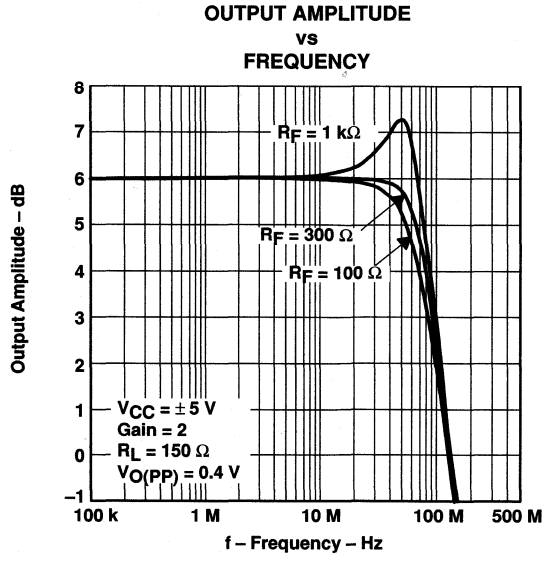


Figure 24

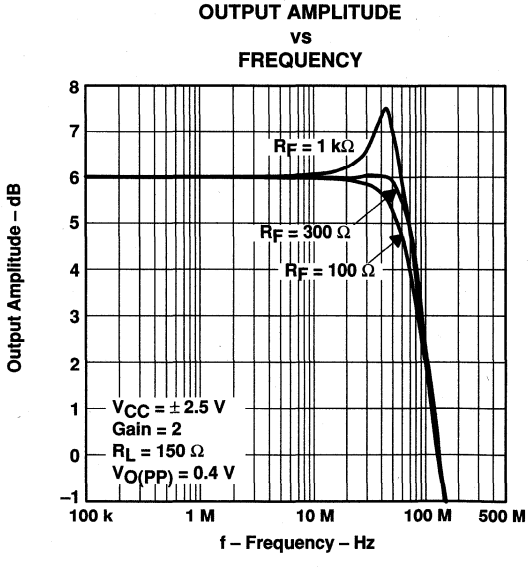


Figure 25

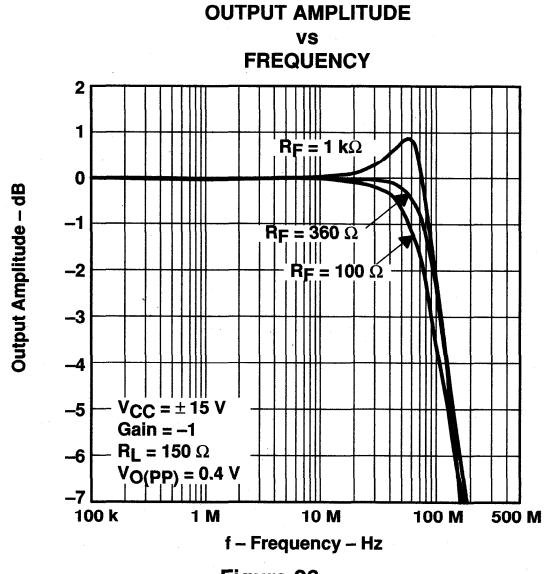


Figure 26

TYPICAL CHARACTERISTICS

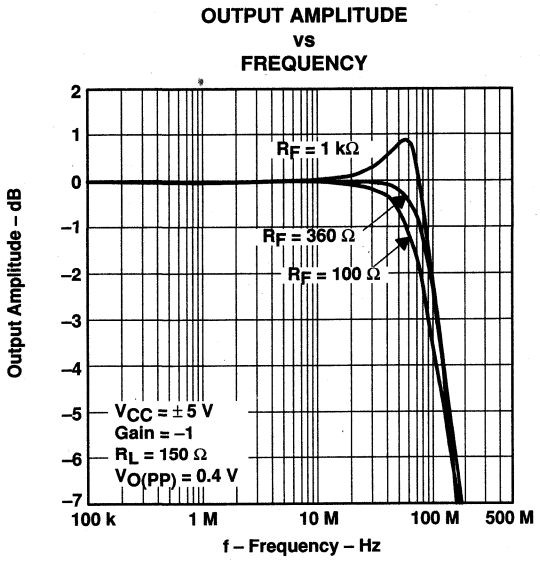


Figure 27

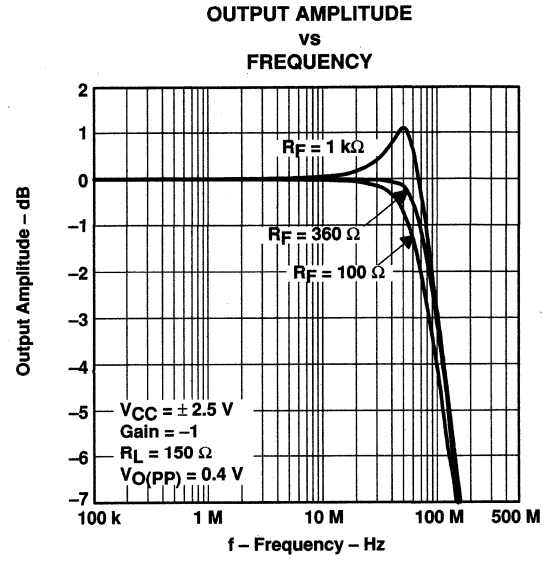


Figure 28

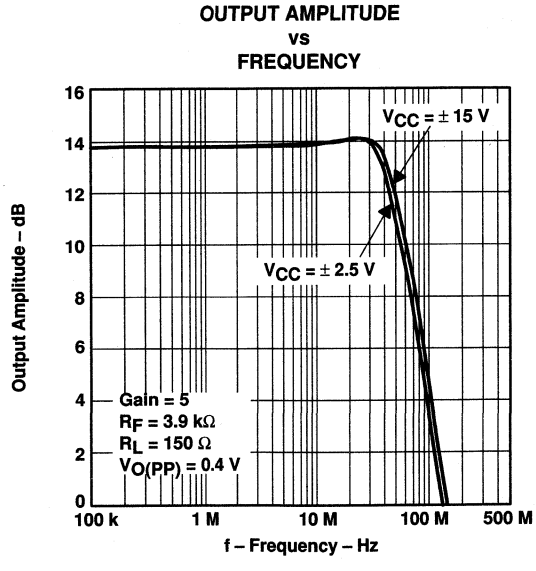


Figure 29

TYPICAL CHARACTERISTICS

SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

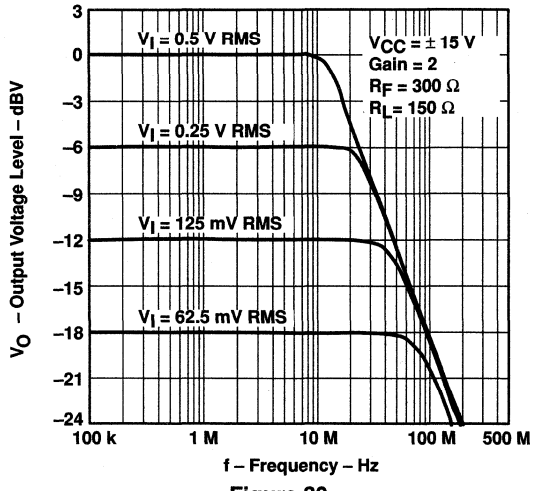


Figure 30

SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

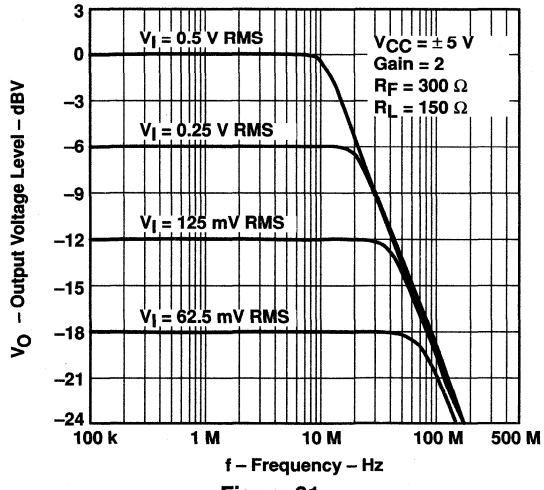


Figure 31

SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

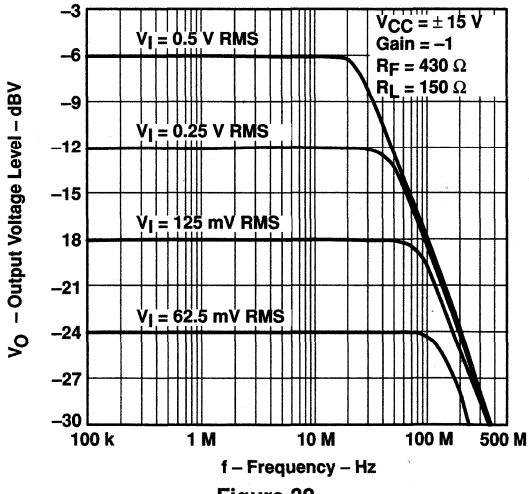


Figure 32

SMALL AND LARGE SIGNAL
FREQUENCY RESPONSE

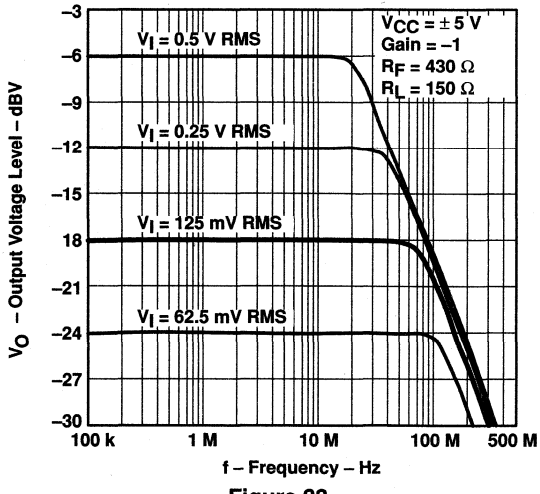


Figure 33

TYPICAL CHARACTERISTICS

1-V STEP RESPONSE

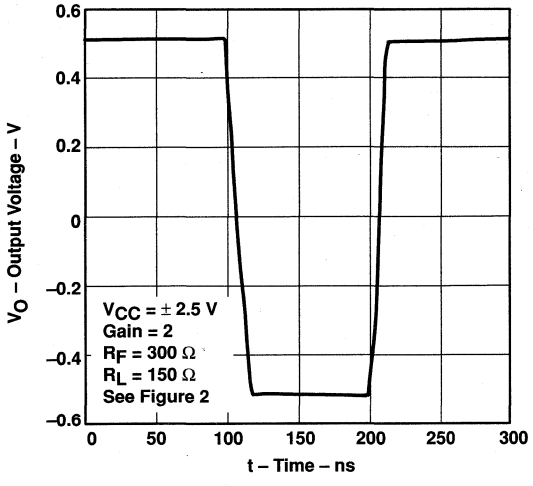


Figure 34

1-V STEP RESPONSE

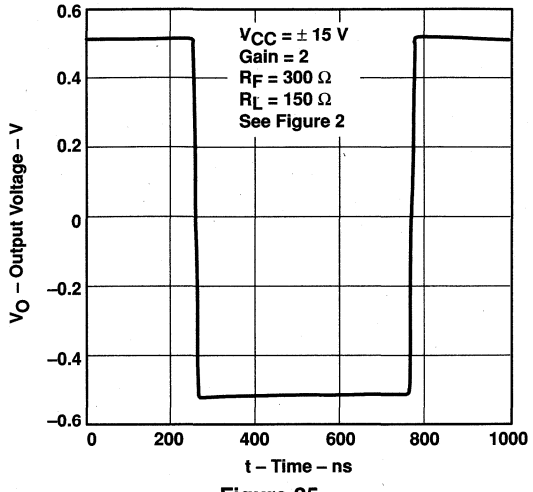


Figure 35

4-V STEP RESPONSE

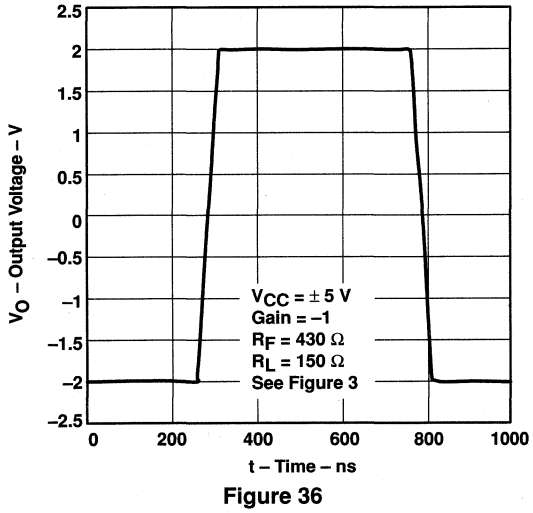


Figure 36

20-V STEP RESPONSE

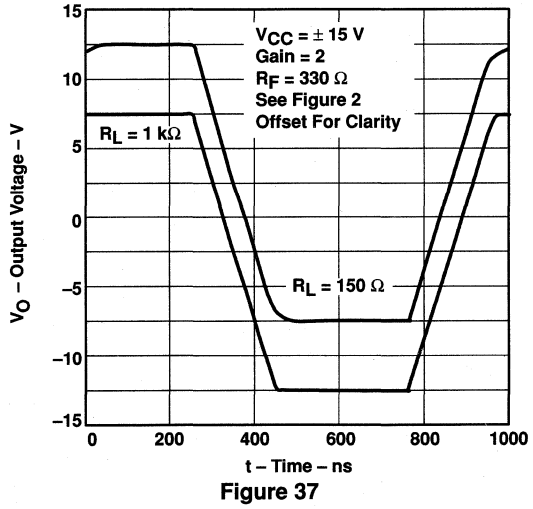


Figure 37

APPLICATION INFORMATION

theory of operation

The THS6062 is a high-speed, operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This results in an exceptionally high-performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 38.

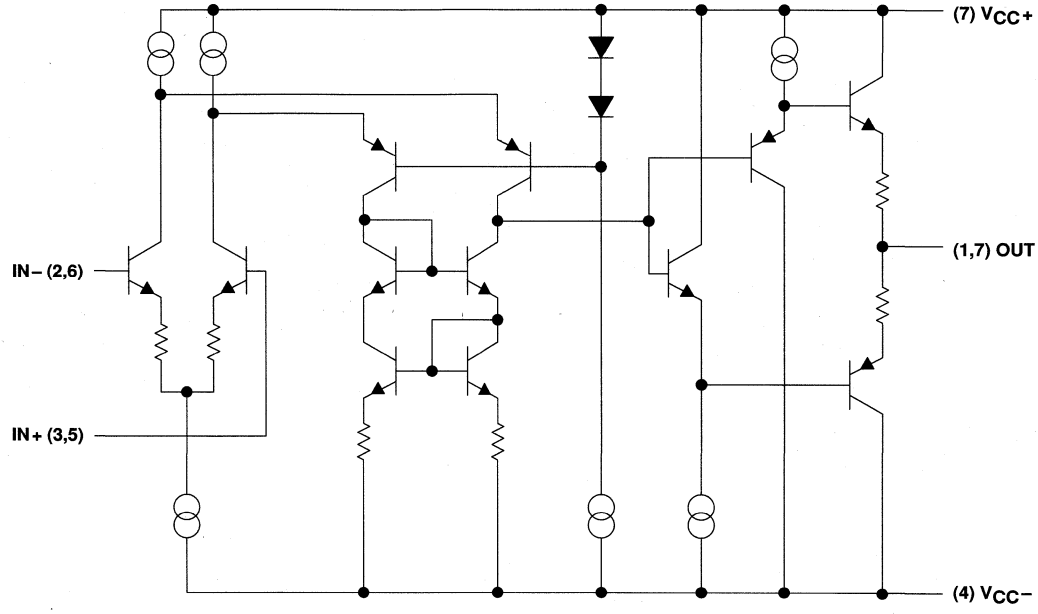


Figure 38. THS6062 Simplified Schematic

APPLICATION INFORMATION

The ADSL remote terminal receive band consists of 255 separate carrier frequencies each with its own modulation and amplitude level. With such an implementation, it is imperative that signals received off the telephone line have as high a signal-to-noise ratio (SNR) as possible. This is because of the numerous sources of interference on the line. The best way to accomplish this high SNR is to have a low-noise receiver on the front-end. It is also important to have the lowest distortion possible to help minimize against interference within the ADSL carriers. The THS6062 was designed with these two priorities in mind.

By taking advantage of the superb characteristics of the complimentary bipolar process (BICOM), the THS6062 offers extremely low noise and distortion while maintaining a high bandwidth. There are some aspects that help minimize distortion in any amplifier. The first is to extend the bandwidth of the amplifier as high as possible without peaking. This allows the amplifier to eliminate any nonlinearities in the output signal. Another thing that helps to minimize distortion is to increase the load impedance seen by the amplifier, thereby reducing the currents in the output stage. This will help keep the output transistors in their linear amplification range and will also reduce the heating effects. This can be seen in Figures 17 to 20, which show a 1-kΩ load distortion is much better than a 150 Ω load.

One client side terminal circuit implementation, shown in Figure 39, uses a 1:2 transformer ratio. While creating a power and output voltage advantage for the line drivers, the 1:2 transformer ratio reduces the SNR for the received signals. The ADSL standard, ANSI T1.413, stipulates a noise power spectral density of –140 dBm/Hz, which is equivalent to 31.6 nV/$\sqrt{\text{Hz}}$ for a 100 Ω system. Although many amplifiers can reach this level of performance, actual ADSL system testing has indicated that the noise power spectral density may typically be ≤ –150 dBm/Hz, or ≤ 10 nV/$\sqrt{\text{Hz}}$. With a transformer ratio of 1:2, this number reduces to less than 5 nV/$\sqrt{\text{Hz}}$. The THS6062, with an equivalent input noise of 1.6 nV/$\sqrt{\text{Hz}}$, is an excellent choice for this application. Coupled with a very low 1.2 pA/$\sqrt{\text{Hz}}$ equivalent input current noise and low value resistors, the THS6062 will ensure that the received signal SNR will be as high as possible.

APPLICATION INFORMATION

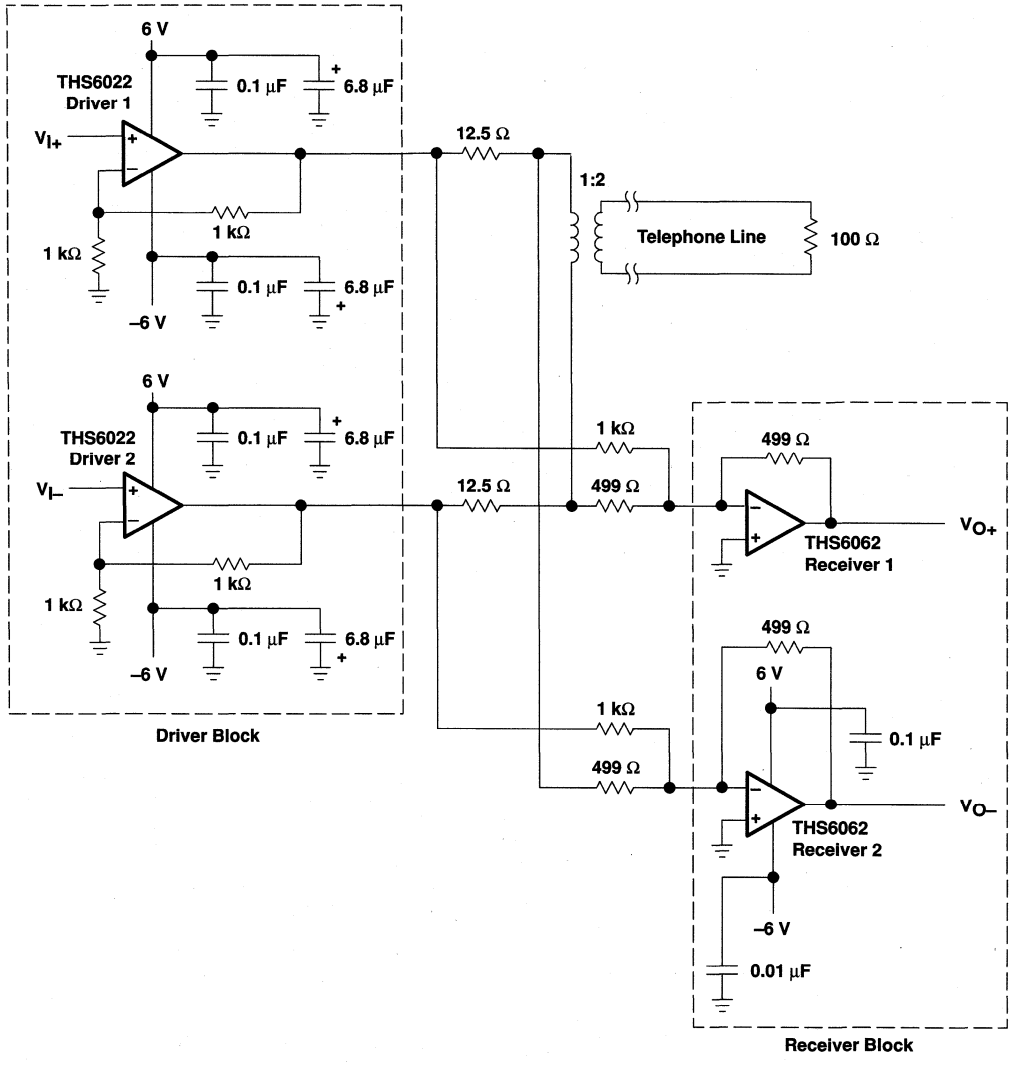


Figure 39. THS6062 Client-Side ADSL Application

APPLICATION INFORMATION

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true for the amplifying small signals. The noise model for current feedback amplifiers (CFB) is the same as voltage feedback amplifiers (VFB). The only difference between the two is that the CFB amplifiers generally specify different current noise parameters for each input, while VFB amplifiers usually only specify one noise current parameter. The noise model is shown in Figure 40. This model includes all of the noise sources as follows:

- e_n = amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = noninverting current noise (pA/$\sqrt{Hz}$)
- IN– = inverting current noise (pA/$\sqrt{Hz}$)
- e_{Rx} = thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR_x)

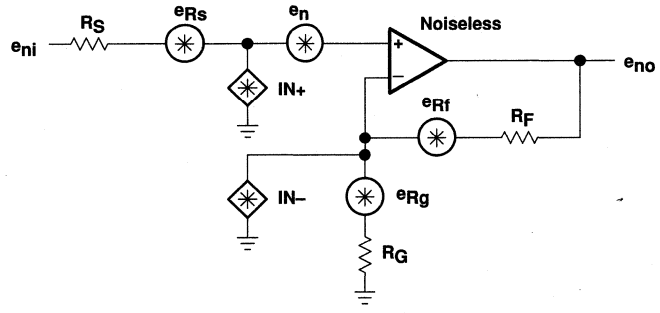


Figure 40. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN+ \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\ kTR_s + 4\ kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\ A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

APPLICATION INFORMATION

noise calculations and noise figure (continued)

For more information on noise analysis, please refer to the *Noise Analysis* section in *Operational Amplifier Circuits Applications Report* (literature number SLVA043).

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^2}{\left(e_{Rs}\right)^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate the noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\ kTR_S}\right]$$

Figure 40 shows the noise figure graph for the THS6062.

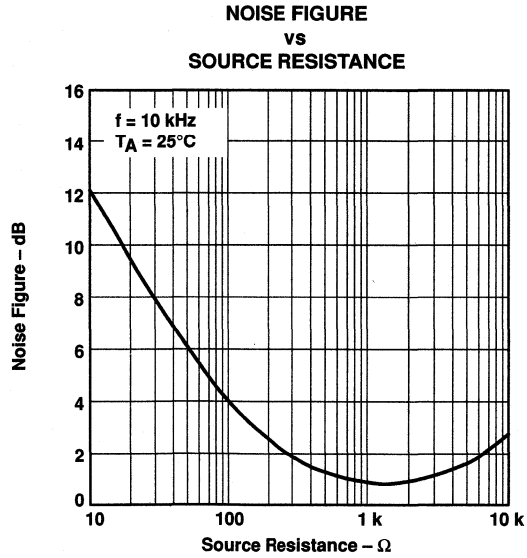


Figure 41. Noise Figure vs Source Resistance

APPLICATION INFORMATION

optimizing frequency response

Internal frequency compensation of the THS6062 was selected to provide very wide bandwidth performance and still maintain a very low noise floor. In order to meet these performance requirements, the THS6062 must have a minimum gain of 2 (–1). Because everything is referred to the noninverting terminal of an operational amplifier, the noise gain in a G = –1 configuration is the same as in a G = 2 configuration.

One of the keys to maintaining a smooth frequency response, and hence, a stable pulse response, is to pay particular attention to the inverting terminal. Any stray capacitance at this node causes peaking in the frequency response (see Figure 42 and Figure 43). There are two things that can be done to help minimize this effect. The first is to simply remove any ground planes under the inverting terminal of the amplifier. This also includes the trace that connects to this terminal. Additionally, the length of this trace should be minimized. The capacitance at this node causes a lag in the voltage being fed back due to the charging and discharging of the stray capacitance. If this lag becomes too long, the amplifier will not be able to correctly keep the noninverting terminal voltage at the same potential as the inverting terminal's voltage. Peaking and possibly oscillations will then occur.

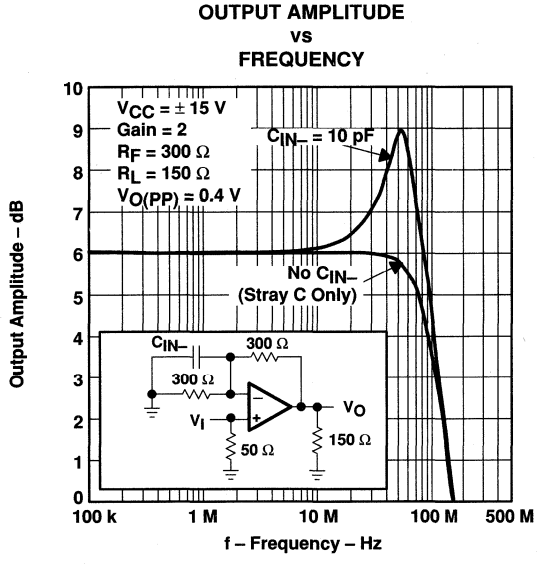


Figure 42

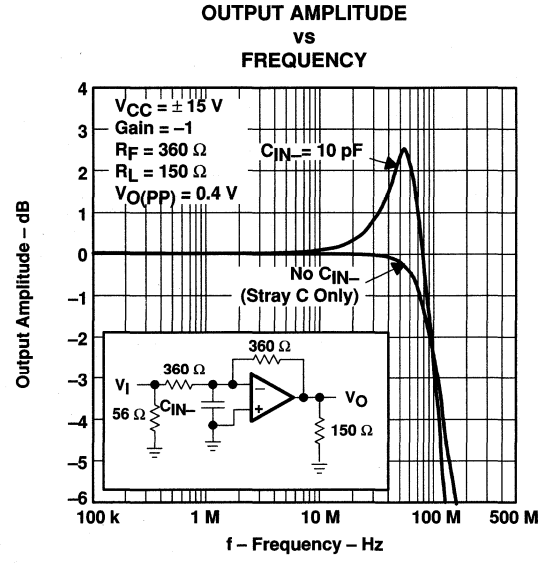


Figure 43

APPLICATION INFORMATION

optimizing frequency response (continued)

The next thing that helps to maintain a smooth frequency response is to keep the feedback resistor (R_f) and the gain resistor (R_g) values fairly low. These two resistors are effectively in parallel when looking at the ac small-signal response. This is why in Figure 29, a feedback resistor of 3.9 kΩ with a gain resistor of 1 kΩ only shows a small peaking in the frequency response. The parallel resistance is only 800 Ω. This value, in conjunction with a very small stray capacitance test PCB, forms a zero on the edge of the amplifier's natural frequency response. To eliminate this peaking, all that needs to be done is to reduce the feedback and gain resistances. One other way to compensate for this stray capacitance is to add a small capacitor in parallel with the feedback resistor. This helps to neutralize the effects of the stray capacitance. To keep this zero out of the operating range, the stray capacitance and resistor value's time constant must be kept low. But, as can be seen in Figures 23 – 28, a value too low starts to reduce the bandwidth of the amplifier. Table 1 shows some recommended feedback resistors to be used with the THS6062.

Table 1. Recommended Feedback Resistors

GAIN	R_f for V_{CC} = ±15 V, ± 5 V, 5 V
2	300 Ω
–1	360 Ω
5	3.3 kΩ (low stray-c PCB only)

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS6062 has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 44. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

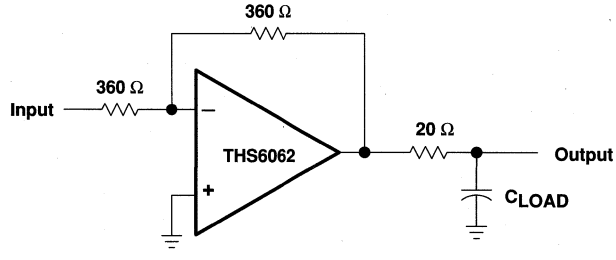
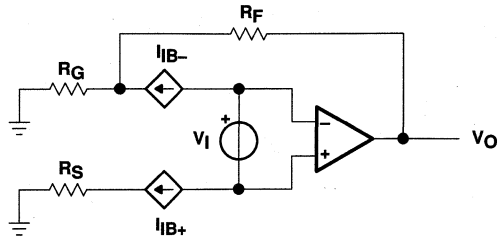


Figure 44. Driving a Capacitive Load

APPLICATION INFORMATION

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula are used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

Figure 45. Output Offset Voltage Model

circuit layout considerations

In order to achieve the high-frequency performance of the THS6062, it is essential that proper printed-circuit board high frequency design techniques be followed. A general set of guidelines is given below. In addition, a THS6062 evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

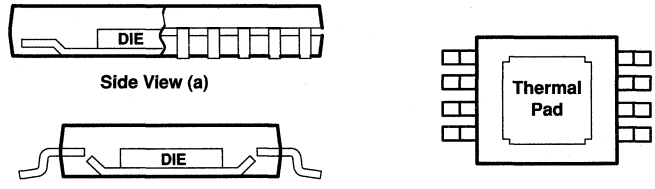
APPLICATION INFORMATION

general PowerPAD design considerations

The THS6062 is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 46(a) and Figure 46(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 45(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.



NOTE A. The thermal pad is electrically isolated from all terminals in the package.

Figure 46. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach.

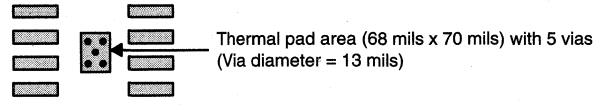


Figure 47. PowerPAD PCB Etch and Via Pattern

APPLICATION INFORMATION

general PowerPAD design considerations

1. Prepare the PCB with a top side etch pattern as shown in Figure 47. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS6062DGN IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS6062DGN package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the THS6062DGN IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

The actual thermal performance achieved with the THS6062DGN in its PowerPAD package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA}, is about 58.4°C/W. For comparison, the non-PowerPAD version of the THS6062 IC (SOIC) is shown. For a given θ_{JA}, the maximum power dissipation is shown in Figure 48 and is calculated by the following formula:

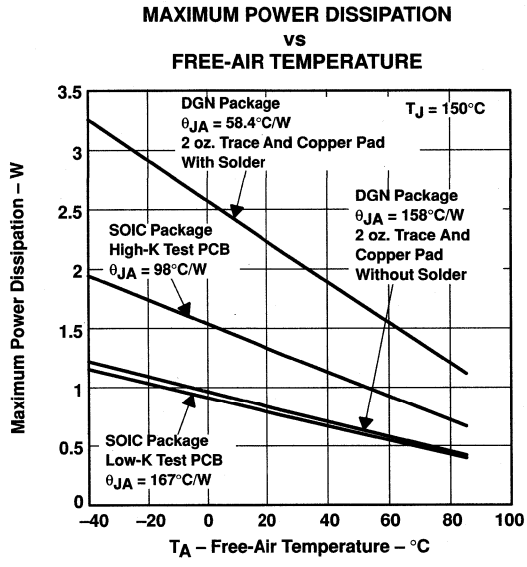
$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS6062 IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

APPLICATION INFORMATION

general PowerPAD design considerations (continued)



NOTE A. Results are with no air flow and PCB size = 3"× 3"

Figure 48. Maximum Power Dissipation vs Free-Air Temperature

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

The next thing that should be considered is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially a multiamplifier device. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 49 and Figure 50 show this effect, along with the quiescent heat, with an ambient air temperature of 50°C. When using V_{CC} = 5 V or ±5 V, there is generally not a heat problem, even with SOIC packages. But, when using V_{CC} = ±15 V, the SOIC package is severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package. Because the THS6062 is a dual amplifier, the sum of the RMS output currents and voltages should be used to choose the proper package.

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

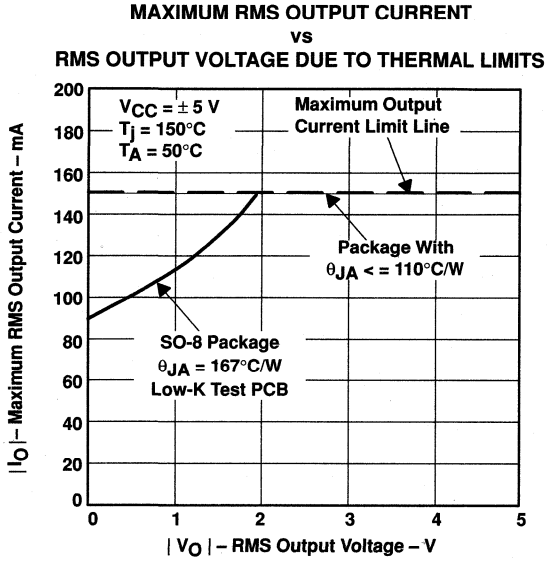


Figure 49

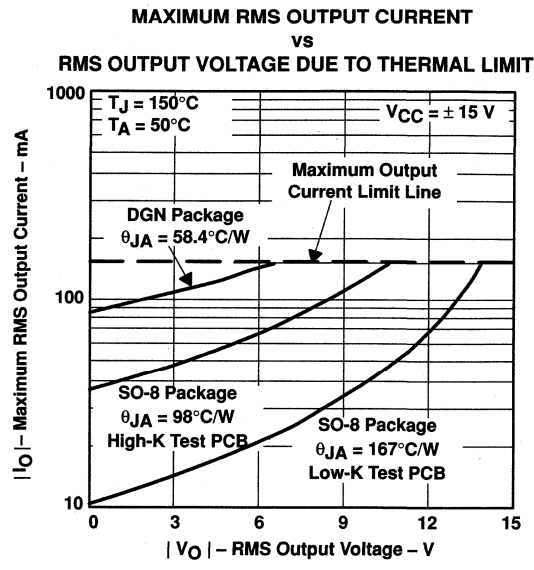


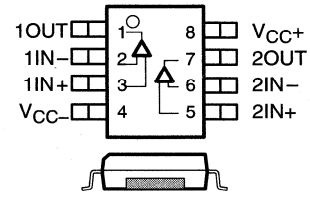
Figure 50

evaluation board

An evaluation board is available for the THS6062 (literature number SLOP221). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. For more information, refer to the *THS6062 EVM User's Guide* (literature number SLOU036) To order the evaluation board contact your local TI sales office or distributor.

- **ADSL Differential Receiver**
  - **Ideal for Central Office or Remote Terminal Applications**
- **Low 3.4 mA Per Channel Quiescent Current**
- **10 nV/√Hz Voltage Noise**
- **Very Low Distortion**
  - **THD = –79 dBc (f = 1 MHz, R_L = 1 kΩ)**
- **High Speed**
  - **175 MHz Bandwidth (–3 dB, G = 1)**
  - **230 V/μs Slew Rate**
- **High Output Drive, I_O = 85 mA (typ)**
- **Wide Range of Power Supplies**
  - **V_{CC} = ±5 V to ±15 V**
- **Available in Standard SOIC or MSOP PowerPAD™ Package**
- **Evaluation Module Available**

THS6072
D OR DGN† PACKAGE
(TOP VIEW)



Cross Section View Showing
PowerPAD Option (DGN)

† This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

description

The THS6072 is a high-speed, low-power differential receiver designed for ADSL communication systems. Its low 3.4-mA per channel quiescent current reduces power to half that of other ADSL receivers making it ideal for low power ADSL applications. This receiver operates with a very low distortion of –79 dBc (f = 1 MHz, R_L = 1 kΩ). The THS6072 is a voltage feedback amplifier offering a high 175-MHz bandwidth and 230-V/μs slew rate and is unity gain stable. It operates over a wide range of power supply voltages including ±4.5 V to ±15 V. This device is available in a standard SOIC or MSOP PowerPAD package.

HIGH-SPEED xDSL LINE DRIVER/RECEIVER FAMILY

DEVICE	DRIVER	RECEIVER	5 V	±5 V	±15 V	DESCRIPTION
THS6002	•	•		•	•	500-mA differential line driver and receiver
THS6012	•			•	•	500-mA differential line driver
THS6022	•			•	•	250-mA differential line driver
THS6032	•			•	•	500-mA low-power ADSL central-office line driver
THS6062		•	•	•	•	Low-noise ADSL receiver
THS6072		•		•	•	Low-power ADSL receiver
THS7002		•		•	•	Low-noise programmable-gain ADSL receiver

CAUTION: The THS6072 provides ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

PowerPAD is a trademark of Texas Instruments Incorporated.

AVAILABLE OPTIONS

T_A	NUMBER OF CHANNELS	PACKAGED DEVICES		MSOP SYMBOL	EVALUATION MODULE
		PLASTIC SMALL OUTLINE† (D)	PLASTIC MSOP† (DGN)		
0°C to 70°C	2	THS6072CD	THS6072CDGN‡	AHZ	THS6072EVM
–40°C to 85°C	2	THS6072ID	THS6072IDGN‡	AIA	—

† The D and DGN packages are available taped and reeled. Add an R suffix to the device type (i.e., THS6072CDGN).
‡ This device is in the Product Preview stage of development. Please contact your local TI sales office for availability.

functional block diagram

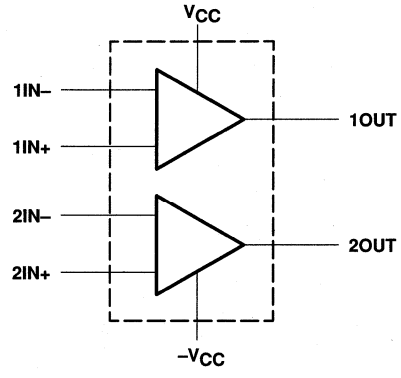


Figure 1. THS6072 – Dual Channel

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} ..... ±16.5 V
Input voltage, V_I ..... $\pm V_{CC}$
Output current, I_O ..... 150 mA
Differential input voltage, V_{IO} ..... ±4 V
Continuous total power dissipation ..... See Dissipation Rating Table
Maximum junction temperature, T_J ..... 150°C
Operating free-air temperature, T_A: C-suffix ..... 0°C to 70°C
I-suffix ..... −40°C to 85°C
Storage temperature, T_{stg} ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	θ_{JA} (°C/W)	θ_{JC} (°C/W)	T_A = 25°C POWER RATING
D	167‡	38.3	740 mW
DGN§	58.4	4.7	2.14 W

‡ This data was taken using the JEDEC standard Low-K test PCB. For the JEDEC Proposed High-K test PCB, the θ_{JA} is 95°C/W with a power rating at T_A = 25°C of 1.32 W.
§ This data was taken using 2 oz. trace and copper pad that is soldered directly to a 3 in. × 3 in. PC. For further information, refer to *Application Information* section of this data sheet.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} and V_{CC-}	Dual supply	±4.5		±16	V
	Single supply	9		32	
Operating free-air temperature, T_A	C-suffix	0		70	°C
	I-suffix	−40		85	

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted)

dynamic performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
BW	Small-signal bandwidth (–3 dB)	V_{CC} = ±15 V		Gain = 1		175		MHz
		V_{CC} = ±5 V				160		
		V_{CC} = ±15 V		Gain = –1		70		MHz
		V_{CC} = ±5 V				65		
	Bandwidth for 0.1 dB flatness	V_{CC} = ±15 V		Gain = 1		35		MHz
		V_{CC} = ±5 V				35		
	Full power bandwidth†	$V_{O(pp)}$ = 20 V,	V_{CC} = ±15 V			2.7		MHz
		$V_{O(pp)}$ = 5 V,	V_{CC} = ±5 V			7.1		
SR	Slew rate‡	V_{CC} = ±15 V,	20-V step	Gain = 5		230		V/µs
		V_{CC} = ±5 V,	5-V step	Gain = 1		170		
t_s	Settling time to 0.1%	V_{CC} = ±15 V,	5-V step	Gain = –1		43		ns
		V_{CC} = ±5 V,	2-V step			30		
	Settling time to 0.01%	V_{CC} = ±15 V,	5-V step	Gain = –1		233		ns
		V_{CC} = ±5 V,	2-V step			280		

† Slew rate is measured from an output level range of 25% to 75%.
‡ Full power bandwidth = slew rate/2π $V_{O(Peak)}$.

noise/distortion performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
THD	Total harmonic distortion	$V_{O(pp)}$ = 2 V, f = 1 MHz, Gain = 2	V_{CC} = ±15 V	R_L = 1 kΩ		–79		dBc
			V_{CC} = ±5 V	R_L = 1 kΩ		–77		
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V, f = 10 kHz				10		nV/√Hz
I_n	Input current noise	V_{CC} = ±5 V or ±15 V, f = 10 kHz				0.7		pA/√Hz
X_T	Channel-to-channel crosstalk	V_{CC} = ±5 V or ±15 V, f = 1 MHz				–75		dB

dc performance

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Open loop gain	V_{CC} = ±15 V, V_O = ±10 V, R_L = 1 kΩ	T_A = 25°C	10	19		V/mV
			T_A = full range	9			
		V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 250 Ω	T_A = 25°C	8	16		V/mV
			T_A = full range	7			
V_{OS}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		1	7	mV
			T_A = full range			8	
	Offset voltage drift		T_A = full range		15		µV/°C
I_{IB}	Input bias current		T_A = 25°C		1.2	6	µA
			T_A = full range			8	
I_{OS}	Input offset current		T_A = 25°C		20	250	nA
			T_A = full range			400	
	Offset current drift	T_A = full range			0.3		nA/°C

electrical characteristics at T_A = 25°C, V_{CC} = ±15 V, R_L = 150 Ω (unless otherwise noted) (continued)

input characteristics

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{ICR}	Common-mode input voltage range	V_{CC} = ±15 V			±13.8	±14.1		V
		V_{CC} = ±5 V			±3.8	±3.9		
CMRR	Common mode rejection ratio	V_{CC} = ±15 V,	V_{ICR} = ±12 V,	T_A = full range	78	93		dB
		V_{CC} = ±5 V,	V_{ICR} = ±2 V,	T_A = full range	84	90		dB
R_I	Input resistance					1		MΩ
C_I	Input capacitance					1.5		pF

output characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage swing	V_{CC} = ±15 V	R_L = 250 Ω	±12	±13.6		V
		V_{CC} = ±5 V	R_L = 150 Ω	±3.4	±3.8		
		V_{CC} = ±15 V	R_L = 1 kΩ	±13	±13.8		V
		V_{CC} = ±5 V		±3.5	±3.9		
I_O	Output current†	V_{CC} = ±15 V	R_L = 20 Ω	65	85		mA
		V_{CC} = ±5 V		50	70		
I_{SC}	Short-circuit current†	V_{CC} = ±15 V			100		mA
R_O	Output resistance	Open loop			13		Ω

† Observe power dissipation ratings to keep the junction temperature below the absolute maximum rating when the output is heavily loaded or shorted. See the absolute maximum ratings section of this data sheet for more information.

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage operating range	Dual supply		±4.5		±16.5	V
		Single supply		9		33	
I_{CC}	Supply current (per amplifier)	V_{CC} = ±15 V	T_A = 25°C		3.4	4.2	mA
			T_A = full range			5	
		V_{CC} = ±5 V	T_A = 25°C		2.9	3.7	
			T_A = full range			4.5	
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = full range	79	90		dB

‡ Full range = 0°C to 70°C for C suffix and −40°C to 85°C for I suffix
§ Slew rate is measured from an output level range of 25% to 75%.
¶ Full power bandwidth = slew rate/2π $V_{O(Peak)}$.

TYPICAL CHARACTERISTICS

OPEN LOOP GAIN & PHASE RESPONSE vs FREQUENCY

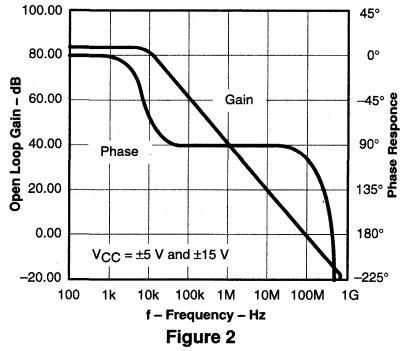


Figure 2

CROSSTALK vs FREQUENCY

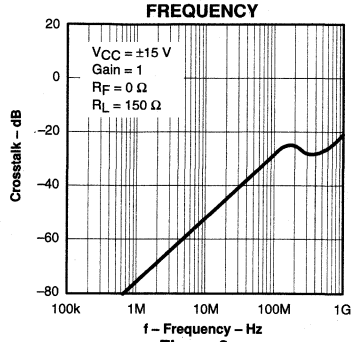


Figure 3

TOTAL HARMONIC DISTORTION vs FREQUENCY

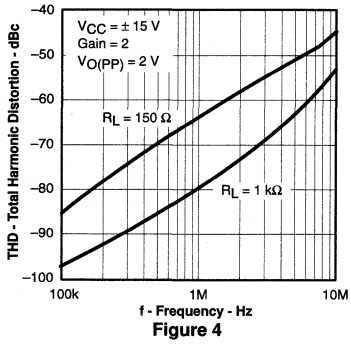


Figure 4

TOTAL HARMONIC DISTORTION vs FREQUENCY

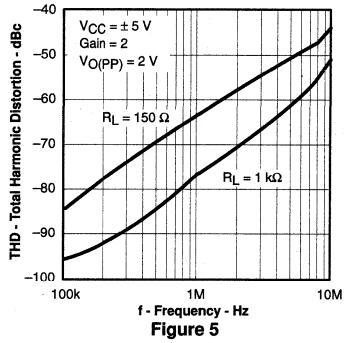


Figure 5

SETTLING vs OUTPUT STEP

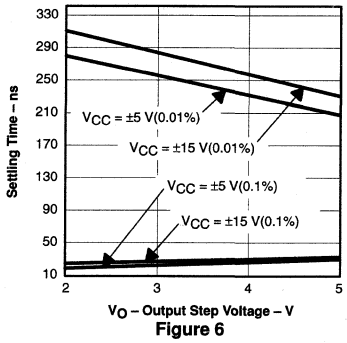


Figure 6

POWER SUPPLY REJECTION RATIO vs FREQUENCY

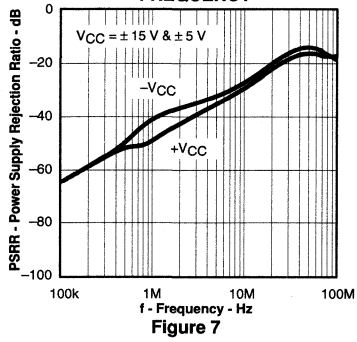


Figure 7

DISTORTION vs OUTPUT VOLTAGE

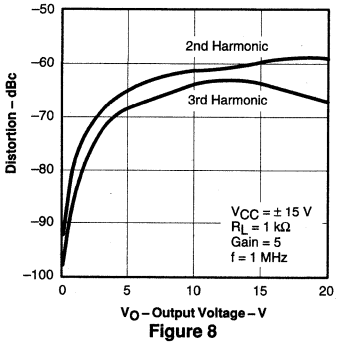


Figure 8

DISTORTION vs OUTPUT VOLTAGE

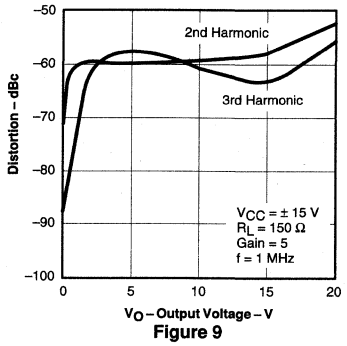


Figure 9

TYPICAL CHARACTERISTICS

DISTORTION vs FREQUENCY

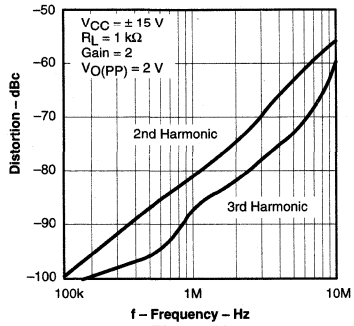


Figure 10

DISTORTION vs FREQUENCY

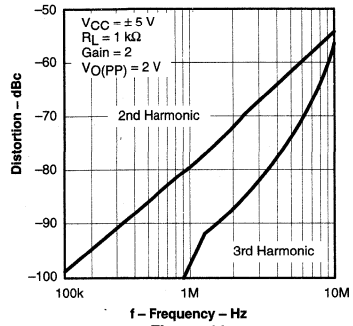


Figure 11

DISTORTION vs FREQUENCY

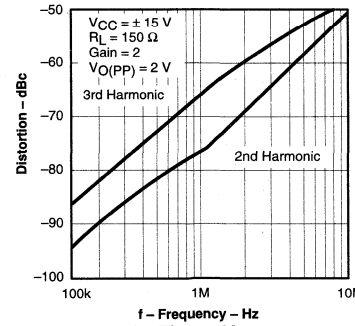


Figure 12

DISTORTION vs FREQUENCY

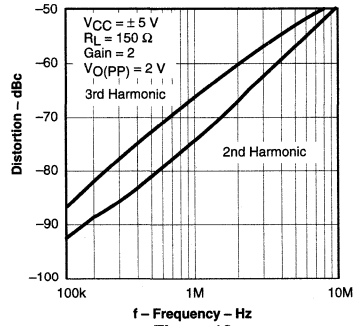


Figure 13

OUTPUT AMPLITUDE vs FREQUENCY

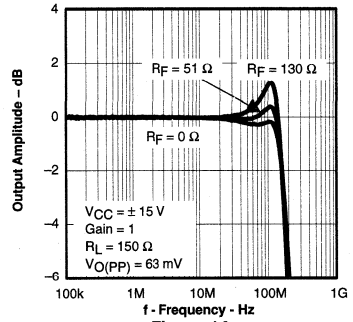


Figure 14

OUTPUT AMPLITUDE vs FREQUENCY

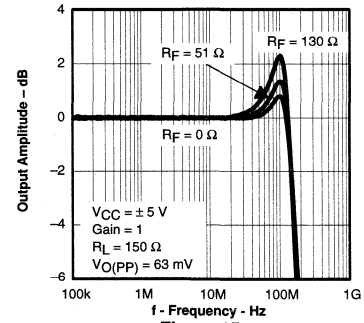


Figure 15

OUTPUT AMPLITUDE vs FREQUENCY

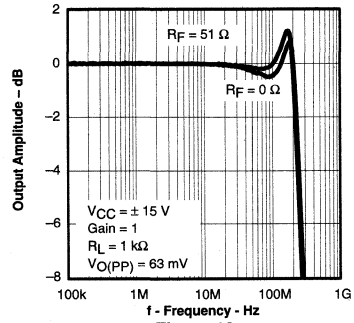


Figure 16

OUTPUT AMPLITUDE vs FREQUENCY

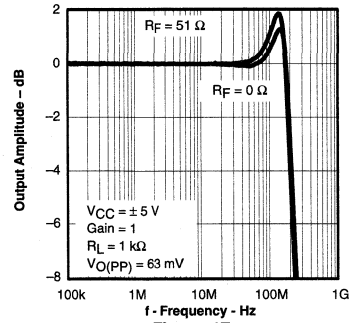


Figure 17

OUTPUT AMPLITUDE vs FREQUENCY

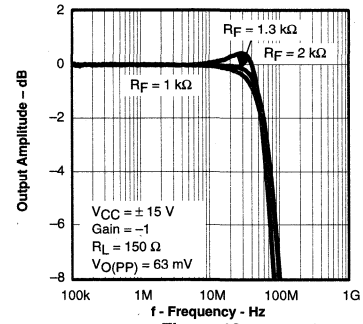


Figure 18

TYPICAL CHARACTERISTICS

OUTPUT AMPLITUDE vs FREQUENCY

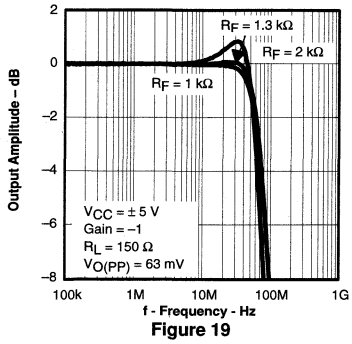


Figure 19

OUTPUT AMPLITUDE vs FREQUENCY

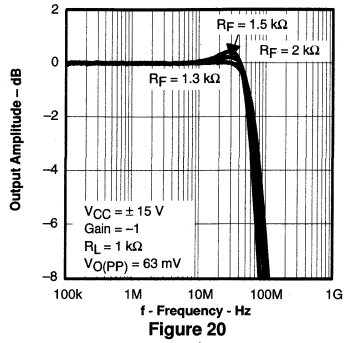


Figure 20

OUTPUT AMPLITUDE vs FREQUENCY

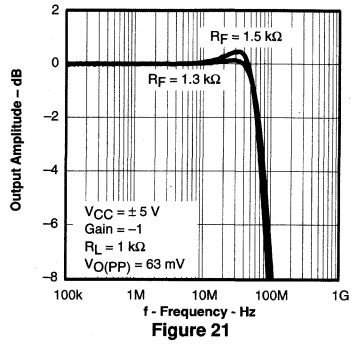


Figure 21

OUTPUT AMPLITUDE vs FREQUENCY

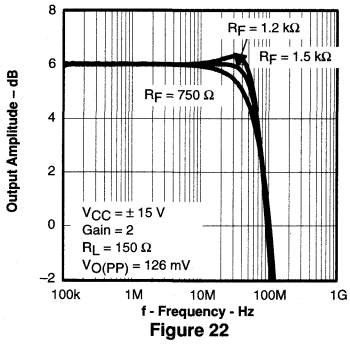


Figure 22

OUTPUT AMPLITUDE vs FREQUENCY

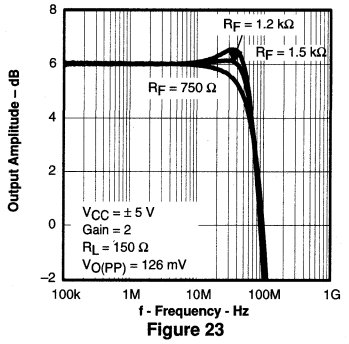


Figure 23

OUTPUT AMPLITUDE vs FREQUENCY

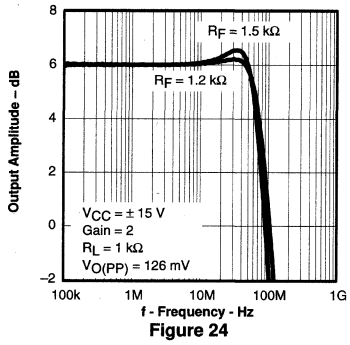


Figure 24

OUTPUT AMPLITUDE vs FREQUENCY

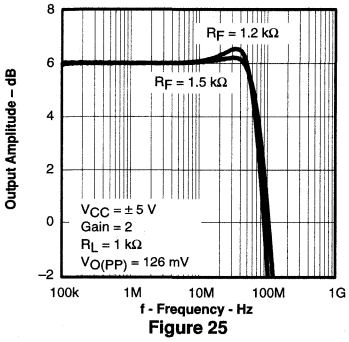


Figure 25

2-V STEP RESPONSE

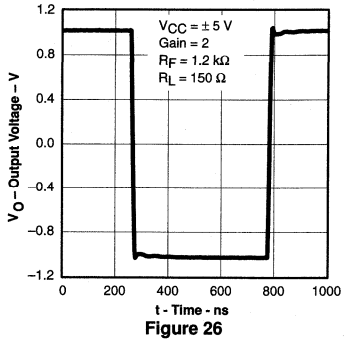


Figure 26

5-V STEP RESPONSE

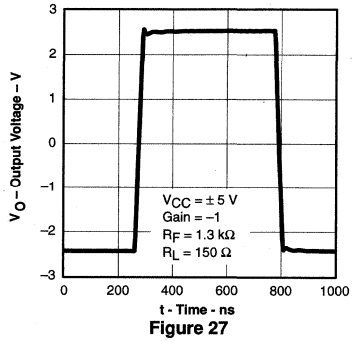


Figure 27

TYPICAL CHARACTERISTICS

2-V STEP RESPONSE

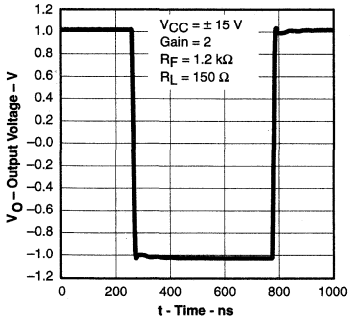


Figure 28

20-V STEP RESPONSE

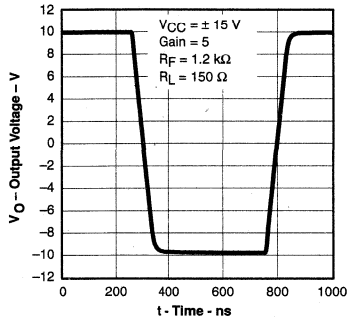


Figure 29

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

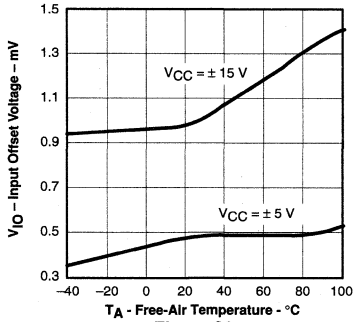


Figure 30

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

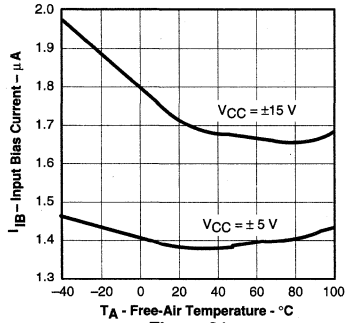


Figure 31

OUTPUT VOLTAGE vs SUPPLY VOLTAGE

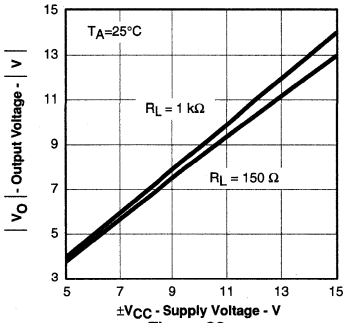


Figure 32

COMMON-MODE INPUT VOLTAGE vs SUPPLY VOLTAGE

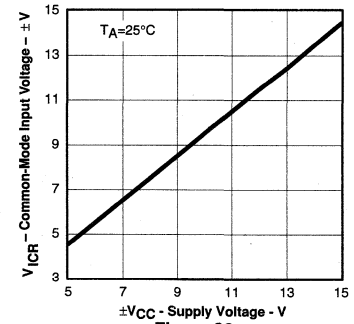


Figure 33

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

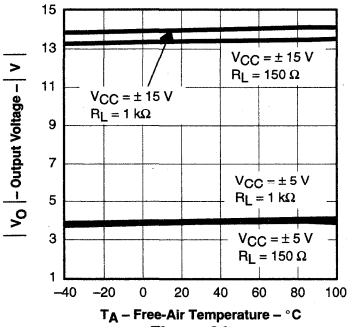


Figure 34

SUPPLY CURRENT vs SUPPLY VOLTAGE

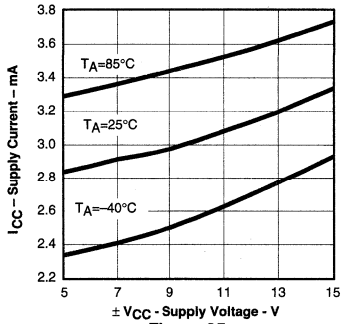


Figure 35

VOLTAGE & CURRENT NOISE vs FREQUENCY

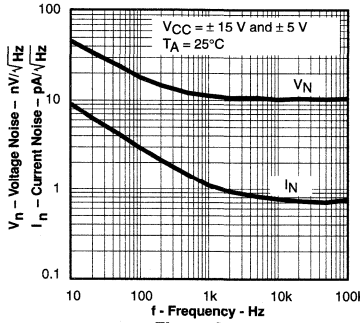


Figure 36

APPLICATION INFORMATION

ADSL line noise

Per ANSI T1.413, the noise power spectral density for an ADSL line is –140 dBm/$\sqrt{\text{Hz}}$. This results in a voltage noise requirement of less than 31.6 nV/$\sqrt{\text{Hz}}$ for the receiver in an ADSL system with a 1:1 transformer ratio.

Noise Power Spectral Density = –140 dBm/$\sqrt{\text{Hz}}$

Power = 1e–17 × 1 Hz = 0.01 fW

Assume: R_L = 100 Ω

$V_{noise} = \sqrt{(P \times R)} = \sqrt{(0.01\ \text{fW} \times 100\ \Omega)} = 31.6\ \text{nV}/\sqrt{\text{Hz}}$

For ADSL systems that use a 1:2 transformer ratio, such as central office line cards, the voltage noise requirement for the receiver is lowered to 15.8 nV/$\sqrt{\text{Hz}}$.

TRANSFORMER RATIO	V_{noise} ON LINE
1:1	31.6 nV/$\sqrt{\text{Hz}}$
1:2	15.8 nV/$\sqrt{\text{Hz}}$

The THS6072 was designed to operate with 10 nV/$\sqrt{\text{Hz}}$ voltage noise, exceeding the noise requirements for an ADSL system operating with 1:1 or 1:2 transformer ratios. For systems where a voltage noise of less than 10 nV/$\sqrt{\text{Hz}}$ voltage noise is required, see the THS6062 low noise ADSL receiver which operates with a voltage noise level of 1.6 nV/$\sqrt{\text{Hz}}$.

minimizing distortion

One way to minimize distortion is to increase the load impedance seen by the amplifier, thereby reducing the currents in the output stage. This will help keep the output transistors in their linear amplification range and will also reduce the heating effects. This can be seen in Figure 10 through Figure 13, which show a 1-kΩ load distortion is much better than a 150-Ω load.

APPLICATION INFORMATION

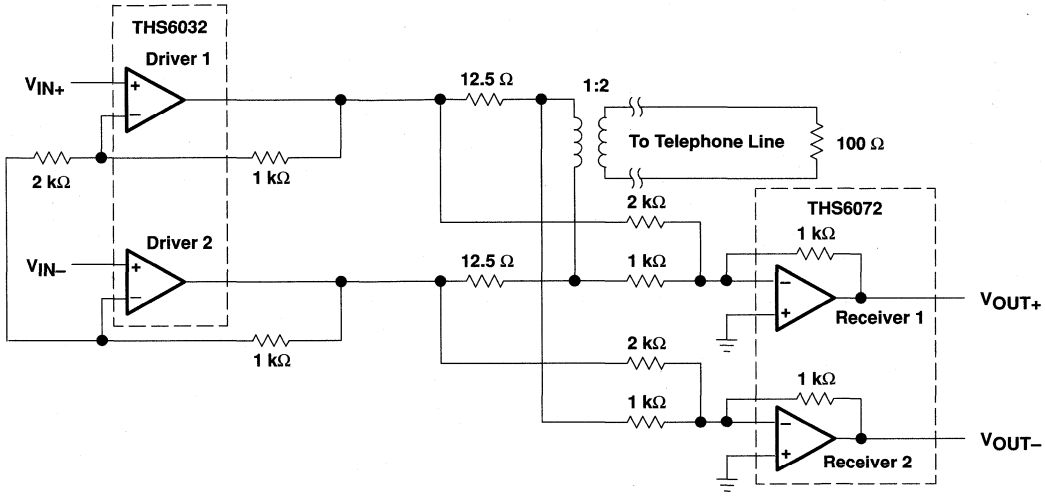


Figure 37. Typical ADSL Central Office Application

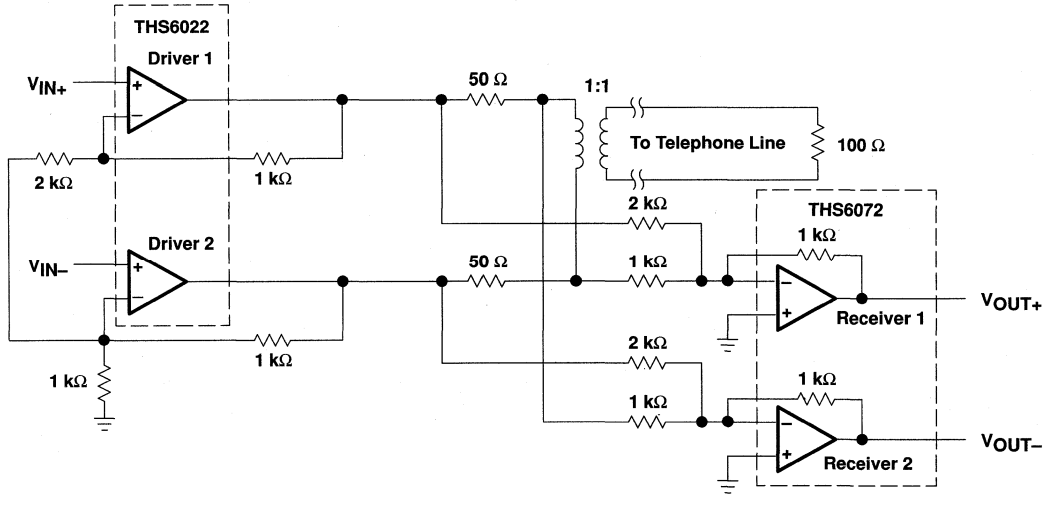


Figure 38. Typical ADSL Remote Terminal Application

APPLICATION INFORMATION

theory of operation

The THS6072 is a high-speed, operational amplifier configured in a voltage feedback architecture. It is built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This results in an exceptionally high performance amplifier that has a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic is shown in Figure 39.

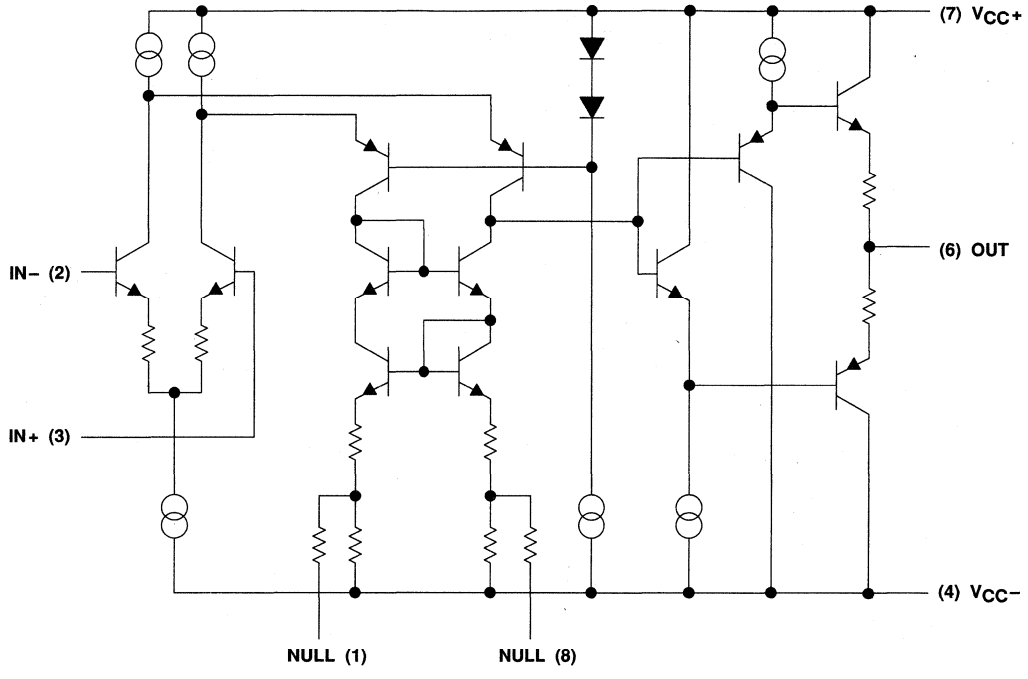


Figure 39. THS6072 Simplified Schematic

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true when amplifying small signals, where signal-to-noise ratio (SNR) is very important. The noise model for the THS6072 is shown in Figure 40. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = Noninverting current noise (pA/$\sqrt{Hz}$)
- IN– = Inverting current noise (pA/$\sqrt{Hz}$)
- e_{Rx} = Thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR_x)

APPLICATION INFORMATION

noise calculations and noise figure (continued)

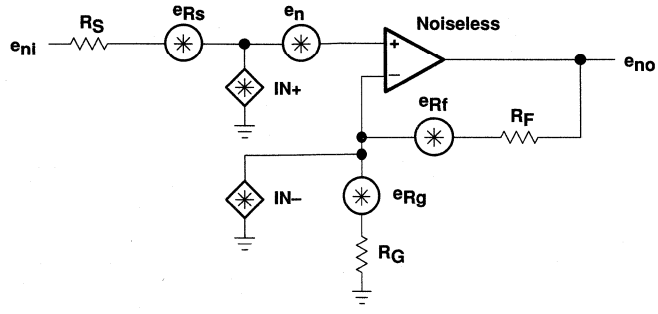


Figure 40. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN + \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\ kTR_s + 4\ kT\left(R_F \parallel R_G\right)}$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = Temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\ A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (noninverting case)}$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

For more information on noise analysis, please refer to the *Noise Analysis* section in *Operational Amplifier Circuits Applications Report* (literature number SLVA043).

APPLICATION INFORMATION

noise calculations and noise figure (continued)

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^{2}}{\left(e_{Rs}\right)^{2}}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate the noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^{2} + \left(IN + \times R_S\right)^{2}\right]}{4\ kTR_S}\right]$$

Figure 41 shows the noise figure graph for the THS6072.

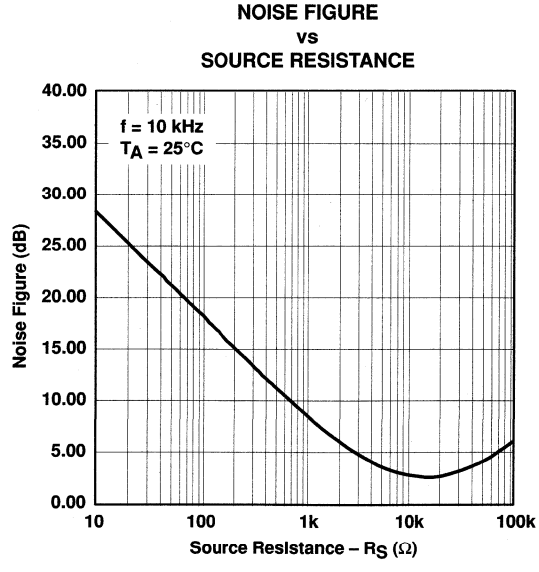


Figure 41. Noise Figure vs Source Resistance

APPLICATION INFORMATION

driving a capacitive load

Driving capacitive loads with high performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS6072 has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 42. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

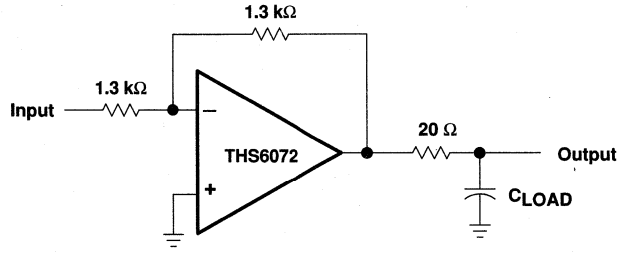
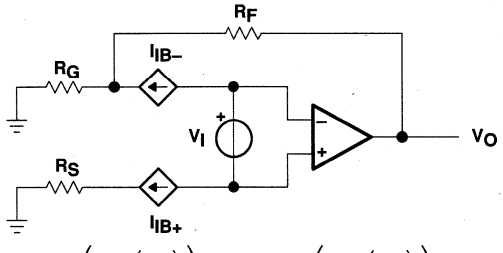


Figure 42. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\ R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\ R_F$$

Figure 43. Output Offset Voltage Model

APPLICATION INFORMATION

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the amplifier (see Figure 44).

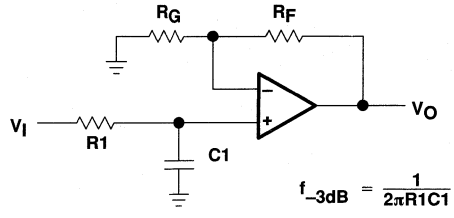


Figure 44. Single-Pole Low-Pass Filter

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APPLICATION INFORMATION

circuit layout considerations

To achieve the levels of high frequency performance of the THS6072, follow proper printed-circuit board high frequency design techniques. A general set of guidelines is given below. In addition, a THS6072 evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes – It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling – Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets – Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- Short trace runs/compact part placements – Optimum high frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components – Using surface-mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

general PowerPAD design considerations

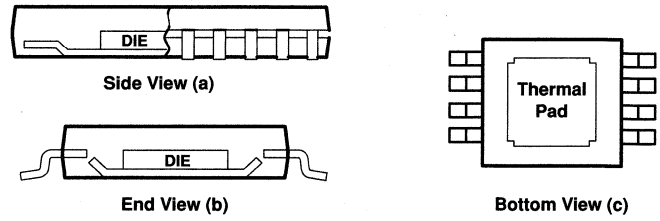
The THS6072 is available packaged in a thermally-enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 45(a) and Figure 45(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 45(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the, heretofore, awkward mechanical methods of heatsinking.

APPLICATION INFORMATION

general PowerPAD design considerations (continued)



NOTE A. The thermal pad is electrically isolated from all terminals in the package.

Figure 45. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach.

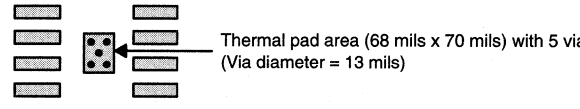


Figure 46. PowerPAD PCB Etch and Via Pattern

1. Prepare the PCB with a top side etch pattern as shown in Figure 46. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS6072DGN IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered, so wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS6072DGN package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the THS6072DGN IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

APPLICATION INFORMATION

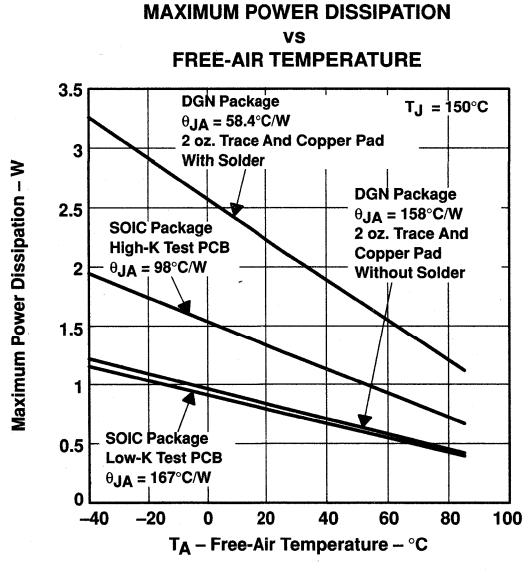
general PowerPAD design considerations (continued)

The actual thermal performance achieved with the THS6072DGN in its PowerPAD package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA}, is about 58.4°C/W. For comparison, the non-PowerPAD version of the THS6072 IC (SOIC) is shown. For a given θ_{JA}, the maximum power dissipation is shown in Figure 47 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS6072 IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A. Results are with no air flow and PCB size = 3"× 3"

Figure 47. Maximum Power Dissipation vs Free-Air Temperature

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

APPLICATION INFORMATION

general PowerPAD design considerations (continued)

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multiamplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents. Figure 48 and Figure 49 show this effect, along with the quiescent heat, with an ambient air temperature of 50°C. Obviously, as the ambient temperature increases, the limit lines shown will drop accordingly. The area under each respective limit line is considered the safe operating area. Any condition above this line will exceed the amplifier's limits and failure may result. When using $V_{CC} = \pm 5$ V, there is generally not a heat problem, even with SOIC packages. But, when using
$V_{CC} = \pm 15$ V, the SOIC package is severely limited in the amount of heat it can dissipate. The other key factor when looking at these graphs is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat dissipation capability increases. The currents and voltages shown in these graphs are for the total package.

THS6072
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

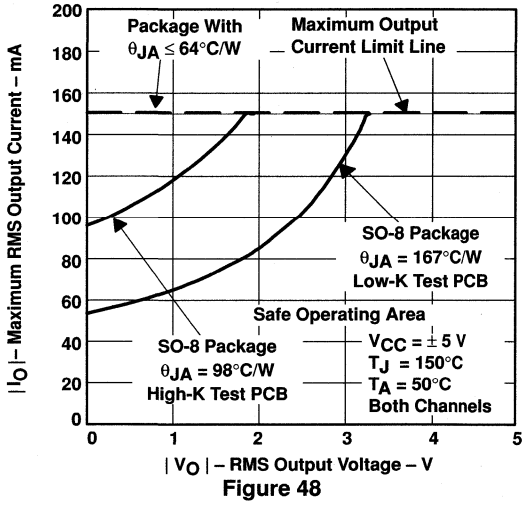


Figure 48

THS6072
MAXIMUM RMS OUTPUT CURRENT
vs
RMS OUTPUT VOLTAGE DUE TO THERMAL LIMITS

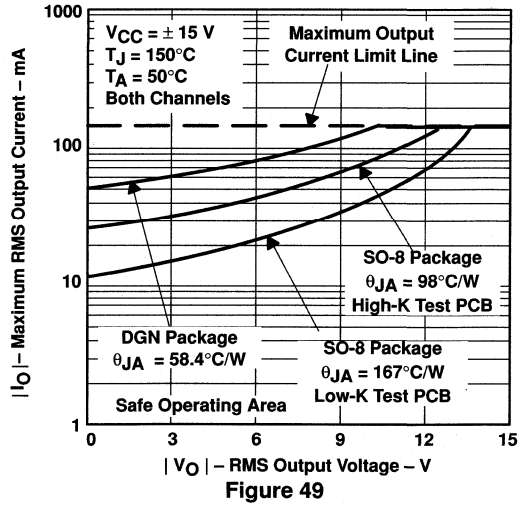


Figure 49

APPLICATION INFORMATION

evaluation board

An evaluation board is available for the THS6072 (literature number SLOP322). This board has been configured for very low parasitic capacitance in order to realize the full performance of the amplifier. A schematic of the evaluation board is shown in Figure 50. The circuitry has been designed so that the amplifier may be used in either an inverting or noninverting configuration. For more information, please refer to the *THS6072 EVM User's Guide*. To order the evaluation board, contact your local TI sales office or distributor.

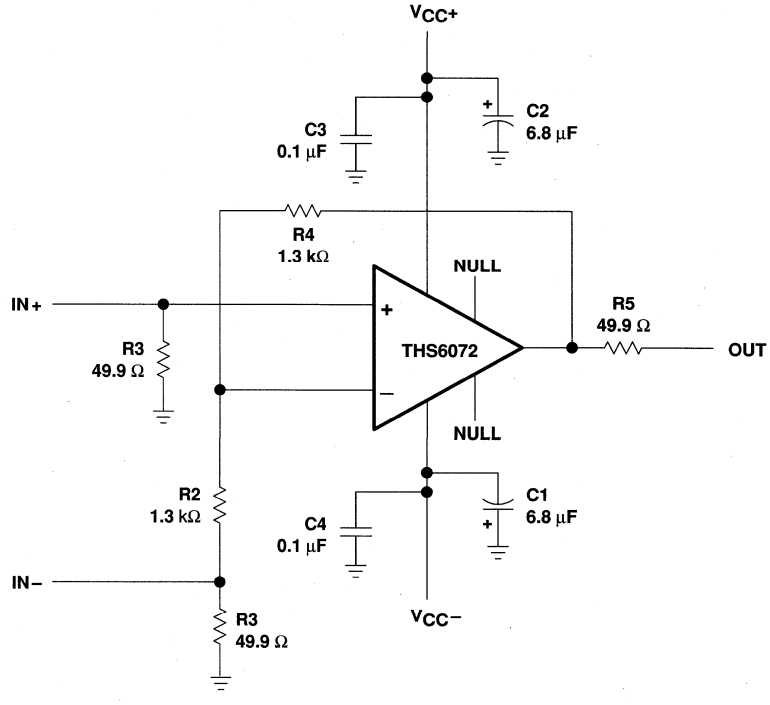


Figure 50. THS6072 Evaluation Board

- **Separate Low Noise Preamp and PGA Stages**
- **Shutdown Control**
- **Preamp Features**
  - **Low Voltage Noise . . . 1.7 nV/$\sqrt{\text{Hz}}$**
  - **Accessible Output Pin for External Filtering**
  - **Voltage Feedback, G_{min} = –1, 2**
  - **100 MHz Bandwidth (–3 dB)**
- **PGA Features**
  - **Digitally Programmable Gain**
  - **–22 dB to 20 dB Gain/Attenuation Range**
  - **6 dB Step Resolution**
  - **Output Clamp Protection**
  - **70 MHz Bandwidth (–3 dB)**
  - **175 V/μs Slew Rate**
- **Wide Supply Range ±4.5 V to ±16 V**
- **PowerPAD™ Package for Enhanced Thermal Performance**

description

The THS7001 (single) and THS7002 (dual) are high-speed programmable-gain amplifiers, ideal for applications where load impedance can often vary. Each channel on this device consists of a separate low-noise input preamp and a programmable gain amplifier (PGA). The preamp is a voltage-feedback amplifier offering a low 1.7-nV/$\sqrt{\text{Hz}}$ voltage noise with a 100-MHz (–3 dB) bandwidth. The output pin of the preamp is accessible so that filters can be easily added to the amplifier.

The 3-bit digitally-controlled PGA provides a –22-dB to 20-dB attenuation/gain range with a 6-dB step resolution. In addition, the PGA provides both high and low output clamp protection to prevent the output signal from swinging outside the common-mode input range of an analog-to-digital converter. The PGA provides a wide 70-MHz (–3 dB) bandwidth, which remains relatively constant over the entire gain/attenuation range. Independent shutdown control is also provided for power conservation and multiplexing. These devices operate over a wide ±4.5-V to ±16-V supply voltage range.

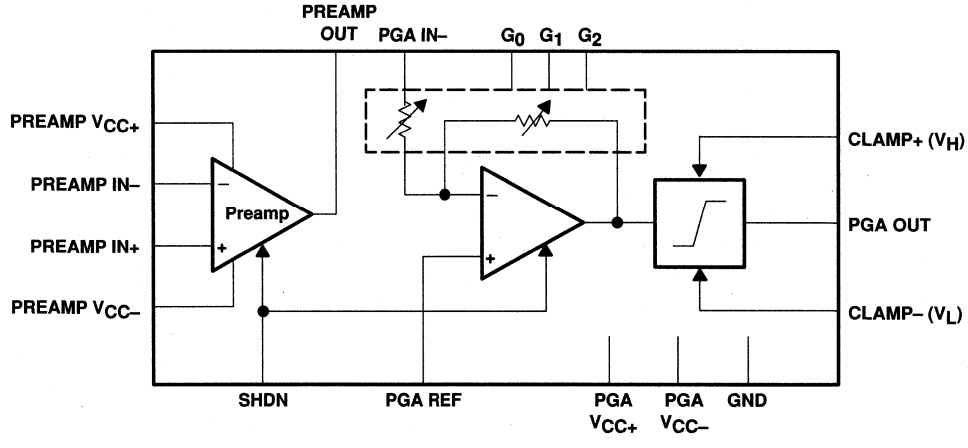
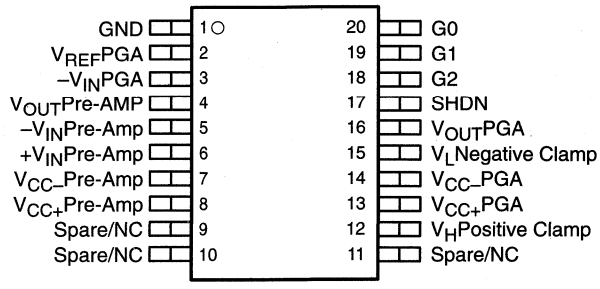


Figure 1. THS7001 Block Diagram

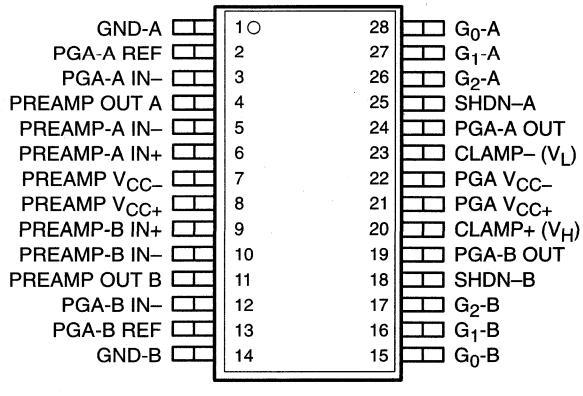
CAUTION: The THS7001 and THS7002 provides ESD protection circuitry. However, permanent damage can still occur if this device is subjected to high-energy electrostatic discharges. Proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

PowerPAD is a trademark of Texas Instruments Incorporated.

THS7001
PWP PACKAGE
(TOP VIEW)



THS7002
PWP PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A	NUMBER OF CHANNELS	PACKAGED DEVICES	EVALUATION MODULE
		PowerPAD PLASTIC TSSOP (PWP)	
0°C to 70°C	1	THS7001CPWP	THS7001EVM
	2	THS7002CPWP	THS7002EVM
–40°C to 85°C	1	THS7001IPWP	—
	2	THS7002IPWP	—

block diagram

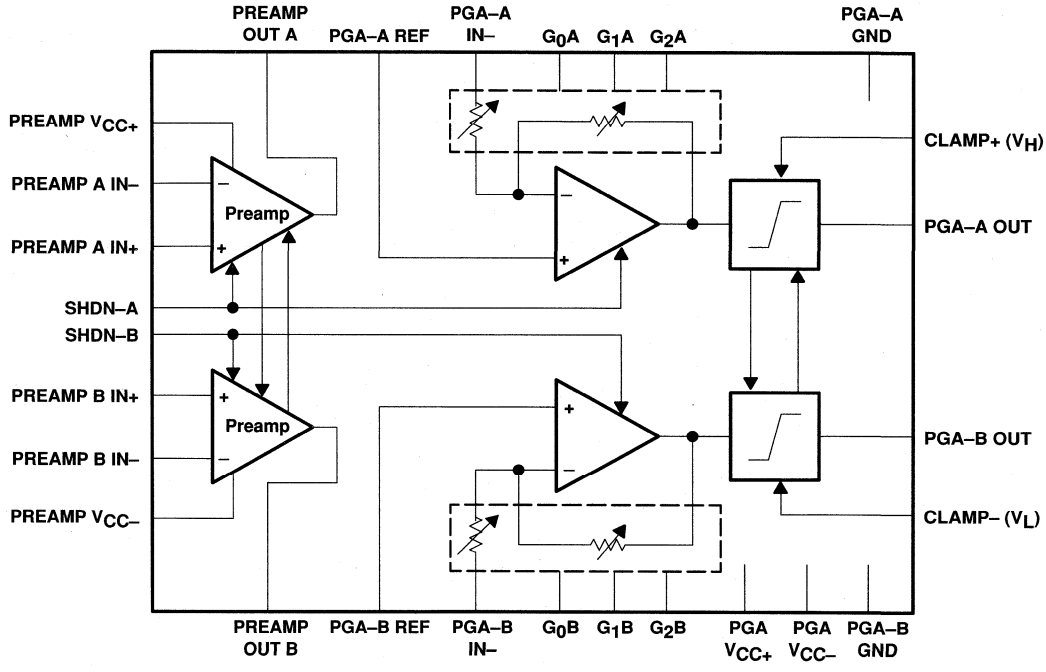


Figure 2. THS7002 Dual Channel PGA

input preamp

To achieve the minimum input equivalent noise required for very small input signals, the input preamp is configured as a classic voltage feedback amplifier with a minimum gain of 2 or –1. The output of the preamp is accessible, allowing for adjustment of gain using external resistors and for external filtering between the preamp and the PGA.

programmable gain amplifier (PGA)

The PGA is an inverting, programmable gain amplifier. The gain is digitally programmable using three control bits (TTL-compatible terminals) that are encoded to provide eight distinct levels of gain/attenuation. Nominal gain/attenuation is shown in Table 1.

Table 1. Nominal Gain/Attenuation

G_2	G_1	G_0	PGA GAIN (dB)	PGA GAIN (V/V)
0	0	0	–22	0.08
0	0	1	–16	0.16
0	1	0	–10	0.32
0	1	1	–4	0.63
1	0	0	2	1.26
1	0	1	8	2.52
1	1	0	14	5.01
1	1	1	20	10.0

output clamping

Output clamping for both upper (V_H) and lower (V_L) levels for the PGAs is provided. There is only one terminal for the positive output clamp and one for the negative output clamp for both channels.

shutdown control

The SHDN terminals allow for powering down the internal circuitry for power conservation or for multiplexing. Separate shutdown controls are available for each channel. The control levels are TTL compatible.

absolute maximum ratings over operating free-air temperature (see Notes 1 and 2)†

Supply voltage, V_{CC} ..... ±16.5 V
Input voltage, V_I ..... $\pm V_{CC}$
Output current, I_O (preamp) (see Note 1) ..... 150 mA
I_O (PGA) (see Note 1) ..... 85 mA
Differential input voltage, V_{ID} ..... ±4 V
Total continuous power dissipation at (or below) T_A = 25°C (see Note 2): THS7001 ..... 3.83 W
THS7002 ..... 4.48 W
Maximum junction temperature, T_J ..... 150°C
Operating free-air temperature, T_A: C-suffix ..... 0°C to 70°C
I-suffix ..... –40°C to 85°C
Storage temperature, T_{stg} ..... –65°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The THS7001 and THS7002 incorporates a PowerPAD on the underside of the chip. The PowerPAD acts as a heatsink and must be connected to a thermal dissipation plane for proper power dissipation. Failure to do so can result in exceeding the maximum junction temperature, which could permanently damage the device. See the *Thermal Information* section of this document for more information about PowerPAD technology.

2. For operation above T_A = 25°C, derate the THS7001 linearly to 2 W at the rate of 30.6 mW/°C and derate the THS7002 linearly to 2.33 W at the rate of 35.9 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Preamp supply voltage, V_{CC+} and V_{CC-}	Split supply	±4.5		±16	V
PGA supply voltage, V_{CC+} and V_{CC-}	Split supply	±4.5‡		±16	V
Operating free-air temperature, T_A	C-suffix	0		70	°C
	I-suffix	–40		85	°C

‡ PGA minimum supply voltage **must be** less than or equal to preamp supply voltage.

preamp electrical characteristics, G = 2, T_A = 25°C, R_L = 150 Ω, (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage operating range	Split supply		±4.5		±16.5	V
V_{OM}	Maximum output voltage swing	R_L = 1 kΩ	V_{CC} = ±5 V	±3.6	±3.8		V
			V_{CC} = ±15 V	±13	±13.6		
		R_L = 150 Ω	V_{CC} = ±5 V	±3.5	±3.7		
		R_L = 250 Ω	V_{CC} = ±15 V	±11	±12.6		
V_{IO}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		1	5	mV
			T_A = full range			7	
	Input offset voltage drift				10		µV/°C
V_{ICR}	Common-mode input voltage range	V_{CC} = ±5 V		±3.8	±4.2		V
		V_{CC} = ±15 V		±13.8	±14		
I_O	Output current (see Note 3)	R_L = 20 Ω	V_{CC} = ±5 V	40	70		mA
			V_{CC} = ±15 V	60	95		
I_{OC}	Short-circuit output current (see Note 3)	V_{CC} = ±15 V			120		mA
I_{IB}	Input bias current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		2.5	6	µA
			T_A = full range			8	
I_{IO}	Input offset current	V_{CC} = ±5 V or ±15 V	T_A = 25°C		30	175	nA
			T_A = full range			400	
	Input offset current drift				0.3		nA/°C
CMRR	Common-mode rejection ratio	V_{CC} = ±5 V, V_{IC} = ±2.5 V	T_A = 25°C	80	89		dB
			T_A = full range	78			
		V_{CC} = ±15 V, V_{IC} = ±12 V	T_A = 25°C	80	88		
			T_A = full range	78			
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	85	100		dB
			T_A = full range	80			
R_I	Input resistance				1		MΩ
C_I	Input capacitance				1.5		pF
R_O	Output resistance	Open loop			13		Ω
I_{CC}	Quiescent current (per channel)	V_{CC} = ±5 V	T_A = 25°C		5.5	7	mA
			T_A = full range			8	
		V_{CC} = ±15 V	T_A = 25°C		7	8	
			T_A = full range			9	

† Full range for the THS7001/02C is 0°C to 70°C. Full range for the THS7001/022I is –40°C to 85°C.

NOTE 3: A heatsink may be required to keep the junction temperature below absolute maximum when an output is heavily loaded or shorted. (See absolute maximum ratings and thermal information section.)

preamp operating characteristics, G = 2, T_A = 25°C, R_L = 150 Ω, (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
SR	Slew rate (see Note 4)	G = –1	V_O = ±2 V, V_{CC} = ±5 V		65		V/µs
			V_O = ±10 V, V_{CC} = ±15 V		85		
t_s	Settling time to 0.1%	G = –1, 5 V Step	V_{CC} = ±5 V		85		ns
			V_{CC} = ±15 V		70		
	Settling time to 0.01%		V_{CC} = ±5 V		95		
			V_{CC} = ±15 V		90		
THD	Total harmonic distortion	V_{CC} = ±15 V, $V_{O(PP)}$ = 2V	f_c = 1 MHz, R_L = 250 Ω		–88		dBc
V_n	Input noise voltage	V_{CC} = ±5 V or ±15 V,	f = 10 kHz		1.7		nV/√Hz
I_n	Input noise current	V_{CC} = ±5 V or ±15 V,	f = 10 kHz		0.9		pA/√Hz
BW	Small-signal bandwidth (–3 dB)	$V_{O(PP)}$ = 0.4V, G = 2	V_{CC} = ±5 V		85		MHz
			V_{CC} = ±15 V		100		
	Bandwidth for 0.1 dB flatness	$V_{O(PP)}$ = 0.4V, G = 2	V_{CC} = ±5 V		35		MHz
			V_{CC} = ±15 V		45		
	Full power bandwidth (see Note 5)	V_{CC} = ±5 V,	V_O = 5 $V_{O(PP)}$		4.1		MHz
		V_{CC} = ±15 V,	V_O = 20 $V_{O(PP)}$		1.4		
A_D	Differential gain error	G = 2, 100 IRE, NTSC	V_{CC} = ±5 V		0.02%		
			V_{CC} = ±15 V		0.02%		
ϕ_D	Differential phase error	G = 2, 100 IRE, NTSC	V_{CC} = ±5 V		0.01°		
			V_{CC} = ±15 V		0.01°		
	Open loop gain	V_{CC} = ±5 V, V_O = ±2.5 V, R_L = 1 kΩ	T_A = 25°C	85	89		dB
			T_A = full range	83			
		V_{CC} = ±15 V, V_O = ±10 V, R_L = 1 kΩ	T_A = 25°C	86	91		
			T_A = full range	84			
	Channel-to-channel crosstalk (THS7002)	V_{CC} = ±5 V or ±15 V,	f = 1 MHz		–85		dB

† Full range for the THS7001/02C is 0°C to 70°C. Full range for the THS7001/02I is –40°C to 85°C.

NOTES: 4. Slew rate is measured from an output level range of 25% to 75%.
5. Full power bandwidth = slew rate/2π $V_{(PP)}$.

shutdown electrical characteristics

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{CC(standby)}$	Standby current, disabled (per channel)	Preamp	$V_{I(SHDN)}$ = 2.5 V	V_{CC} = ±5 V		0.2	0.3	mA
				V_{CC} = ±15 V		0.65	0.8	
		PGA		V_{CC} = ±5 V or ±15 V		0.8	1.2	
$V_{IH(SHDN)}$	Shutdown voltage for power up		V_{CC} = ±5 V or ±15 V,	Relative to GND			0.8	V
$V_{IL(SHDN)}$	Shutdown voltage for power down				2			V
$I_{IH(SHDN)}$	Shutdown input current high		V_{CC} = ±5 V or ±15 V,	$V_{I(SHDN)}$ = 5 V		300	400	µA
$I_{IL(SHDN)}$	Shutdown input current low			$V_{I(SHDN)}$ = 0.5 V		25	50	µA
t_{dis}	Disable time†		V_{CC} = ±5 V or ±15 V,	Preamp and PGA		100		ns
t_{en}	Enable time†		V_{CC} = ±5 V or ±15 V,	Preamp and PGA		1.5		µs

† Disable time and enable time are defined as the interval between application of the logic signal to SHDN and the point at which the supply current has reached half its final value.

PGA electrical characteristics, T_A = 25°C, Gain = 2 dB, R_L = 1 kΩ, (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range	Split supply		±4.5‡		±16.5	V
V_{OM}	Maximum output voltage swing	R_L = 1 kΩ	V_{CC} = ±5 V	±3.6	±4.1		V
			V_{CC} = ±15 V	±13.2	±13.8		
V_{IO}	Input offset voltage	V_{CC} = ±5 V or ±15 V	T_A = 25°C		2	9	mV
			T_A = full range			11	
	Input offset voltage drift				10		µV/°C
	Reference input voltage range	V_{CC} = ±5 V		±3.8	±4.0		V
		V_{CC} = ±15 V		±13.5	±13.8		
I_{IB}	Input bias current (reference terminal)	V_{CC} = ±5 V or ±15 V	T_A = 25°C		1	2	µA
			T_A = full range			3	
I_O	Output current	R_L = 20 Ω	V_{CC} = ±5 V	30	50		mA
I_{OS}	Short-circuit output current				80		mA
PSRR	Power supply rejection ratio	V_{CC} = ±5 V or ±15 V	T_A = 25°C	75	82		dB
			T_A = full range	72			
R_I	Input resistance	Gain = 20 dB			0.27		kΩ
		Gain = –22 dB			3		
R_O	Output resistance	Open loop			20		Ω
I_{CC}	Quiescent supply current (per channel)	V_{CC} = ±5 V	T_A = 25°C		4.8	6	mA
			T_A = full range			7	
		V_{CC} = ±15 V	T_A = 25°C		5	7	
			T_A = full range			8	

† Full range for the THS7001/02C is 0°C to 70°C. Full range for the THS7001/02I is –40°C to 85°C.
‡ PGA minimum supply voltage **must be** less than or equal to preamp supply voltage.

output limiting characteristics

PARAMETER	TEST CONDITIONS†			MIN	TYP	MAX	UNIT
Clamp accuracy	V_{CC} = ±15 V, V_I = ±10 V, Gain = 2 dB	V_H = 10 V, V_L = –10 V,	T_A = 25°C		±250	±300	mV
			T_A = full range			±350	
	V_{CC} = ±5 V, V_I = ±2.5 V, Gain = 2 dB	V_H = 2 V, V_L = –2 V,	T_A = 25°C		±50	±80	
			T_A = full range			±100	
Clamp overshoot	V_{CC} = ±15 V, V_I = ±10 V,	V_H = 10 V, t_r and t_f = 1 ns	V_L = –10 V,		0.5%		
	V_{CC} = ±5 V, V_I = ±2.5 V,	V_H = 2 V, t_r and t_f = 1 ns	V_L = –2 V,		0.3%		
Overdrive recovery time	V_{CC} = ±15 V, V_I = ±10 V	V_H = 10 V,	V_L = –10 V,		7		ns
	V_{CC} = ±5 V, V_I = ±2.5 V	V_H = 2 V,	V_L = 2 V,		6		
Clamp input bias current	V_O = 3.3 V, V_H = 3.3 V	V_L = 3.3 V,	T_A = 25°C		1	5	µA
			T_A = full range			8	

† Full range for the THS7002C is 0°C to 70°C. Full range for the THS7002I is –40°C to 85°C.

PGA electrical characteristics, T_A = 25°C, Gain = 2 dB, R_L = 1 kΩ, (unless otherwise noted) (continued)

digital gain characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	Relative to GND	2			V
V_{IL}	Low-level input voltage				0.8	V
I_{IH}	High-level input current	V_{IH} = 5 V		20	100	nA
I_{IL}	Low-level input current (sink current)	V_{IL} = 0.5 V		0.9	2	µA
t_d	Gain-change delay time†	V_{CC} = ±5 V or ±15 V		2		µs

† Gain-change delay time is the time needed to reach 90% of its final gain value.

PGA operating characteristics, T_A = 25°C, Gain = 2 dB, R_L = 1 kΩ, (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP	MAX	UNIT
SR	Slew rate (see Note 4)	V_{CC} = ±5 V,	V_O = ±2.5 V		160		V/µs
		V_{CC} = ±15 V,	V_O = ±10 V		175		
t_s	Settling time to 0.1%	5 V Step	V_{CC} = ±15 V		125		ns
			V_{CC} = ±5 V		120		
THD	Total harmonic distortion	V_{CC} = ±15 V, f_C = 1 MHz,	$V_{O(PP)}$= 2 V, Gain = 8 dB		–69		dBc
BW	Small-signal bandwidth (–3 dB)	Gain = 20 dB, $V_{O(PP)}$ = 0.4 V	V_{CC} = ±15 V		65		MHz
			V_{CC} = ±5 V		60		
		Gain = 2 dB, $V_{O(PP)}$ = 0.4 V	V_{CC} = ±15 V		75		
			V_{CC} = ±5 V		70		
		Gain = –22 dB, $V_{O(PP)}$ = 0.4 V	V_{CC} = ±15 V		80		
			V_{CC} = ±5 V		70		
	Bandwidth for 0.1 dB flatness	Gain = 2 dB, $V_{O(PP)}$ = 0.4 V	V_{CC} = ±15 V		20		MHz
			V_{CC} = ±5 V		18		
	Full power bandwidth (see Note 5)	$V_{O(PP)}$ = 5 V,	V_{CC} = ±5 V		10		MHz
		$V_{O(PP)}$ = 20 V,	V_{CC} = ±15 V		2.8		
A_D	Differential gain error	G = 8 dB, 100 IRE, NTSC, R_L = 150 Ω	V_{CC} = ±5 V		0.04%		
			V_{CC} = ±15 V		0.04%		
ϕ_D	Differential phase error	G = 8 dB, ±100 IRE, NTSC, R_L = 150 Ω	V_{CC} = ±15 V		0.07		°
			V_{CC} = ±5 V		0.09		
	Gain accuracy (see Note 6)	Gain = –22 dB to 20 dB, All 8 steps, V_{CC} = ±5 V or ±15 V	T_A = 25°C	–7.5%	0%	7.5%	
			T_A = full range	–8.5%		8.5%	
	Channel-to-channel gain accuracy (THS7002 only) (see Note 7)	Gain = –22 dB to 20 dB, All 8 steps, V_{CC} = ±5 V or ±15 V	T_A = 25°C	–5.5%	0%	5.5%	
			T_A = full range	–6.5%		6.5%	
V_n	Input referred noise voltage	V_{CC} = ±5 V or ±15 V, f = 10 kHz	Gain = 20 dB		10		nV/√Hz
			Gain = –22 dB		500		
	PGA channel-to-channel crosstalk (THS7002 only)	V_{CC} = ±5 V or ±15 V,	f = 1 MHz		–77		dB

† Full range for the THS7001/02C is 0°C to 70°C. Full range for the THS7001/02I is –40°C to 85°C.

NOTES: 4. Slew rate is measured from an output level range of 25% to 75%.
5. Full power bandwidth = slew rate/2π V_{PEAK}
6. Specified as –100 × (output voltage – (input voltage × gain))/(input voltage × gain)
7. Specified as 100 × (output voltage B– output voltage A)/output voltage A

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

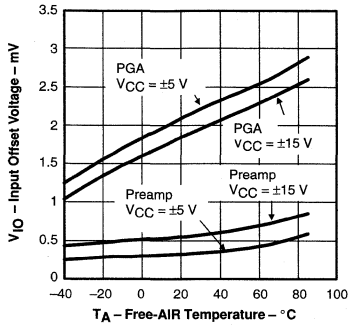


Figure 3

STANDBY SUPPLY CURRENT vs FREE-AIR TEMPERATURE

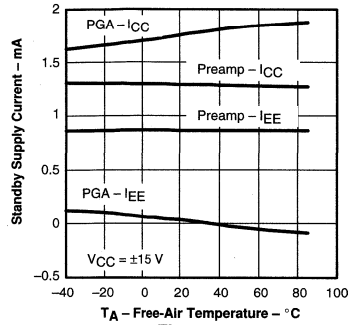


Figure 4

QUIESCENT SUPPLY CURRENT vs FREE-AIR TEMPERATURE

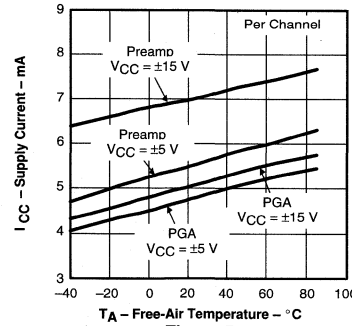


Figure 5

PSRR vs FREQUENCY

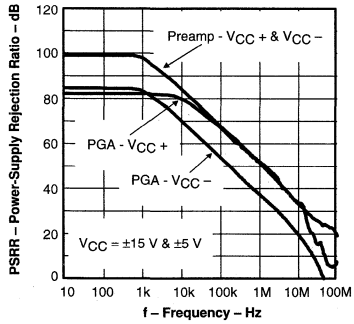


Figure 6

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

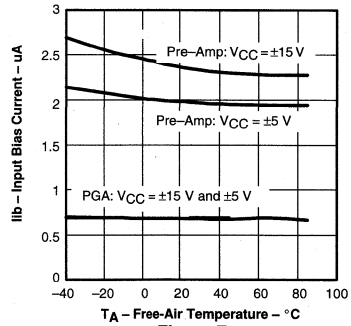


Figure 7

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

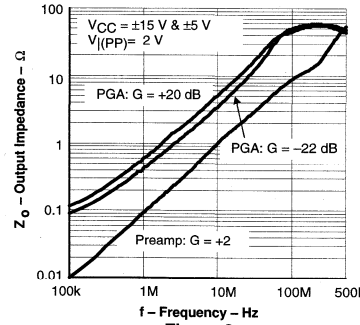


Figure 8

PREAMP INPUT COMMON-MODE VOLTAGE RANGE vs SUPPLY VOLTAGE

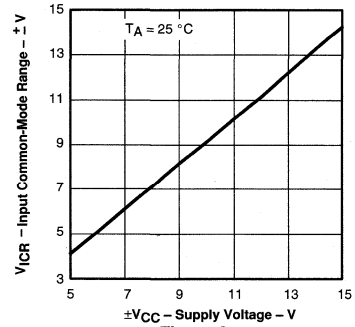


Figure 9

PREAMP OUTPUT VOLTAGE vs SUPPLY VOLTAGE

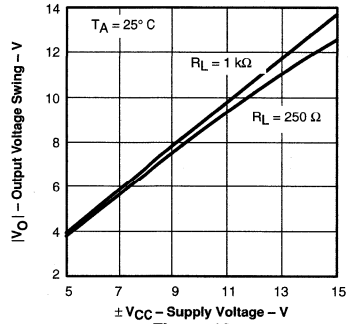


Figure 10

PREAMP CMRR vs FREQUENCY

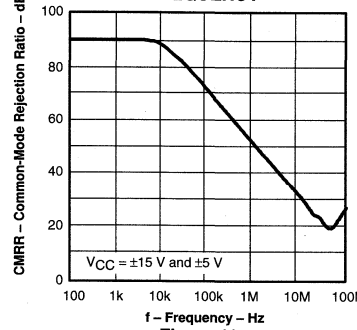


Figure 11

TYPICAL CHARACTERISTICS

PREAMP OPEN LOOP GAIN AND PHASE RESPONSE vs FREQUENCY

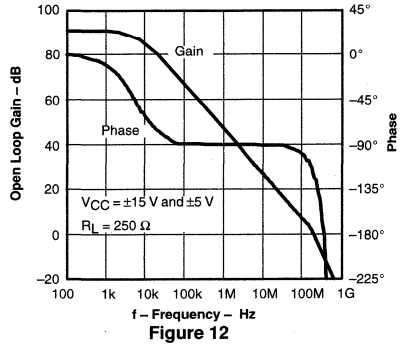


Figure 12

PREAMP INPUT REFERRED VOLTAGE NOISE AND CURRENT NOISE vs FREQUENCY

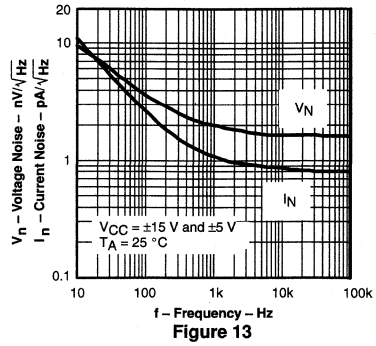


Figure 13

PREAMP OUTPUT AMPLITUDE vs FREQUENCY

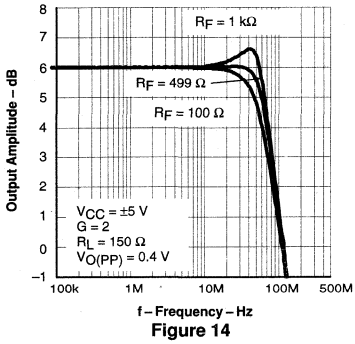


Figure 14

PREAMP OUTPUT AMPLITUDE vs FREQUENCY

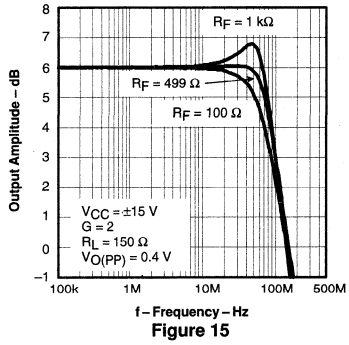


Figure 15

PREAMP OUTPUT AMPLITUDE vs FREQUENCY

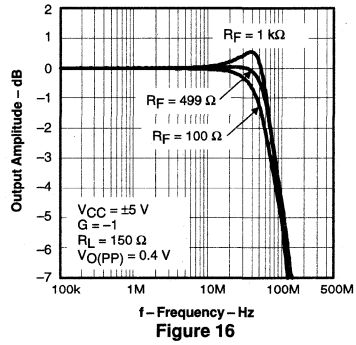


Figure 16

PREAMP OUTPUT AMPLITUDE vs FREQUENCY

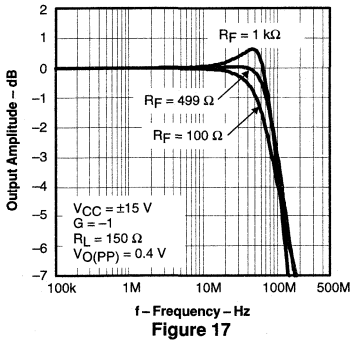


Figure 17

PREAMP OUTPUT AMPLITUDE vs FREQUENCY

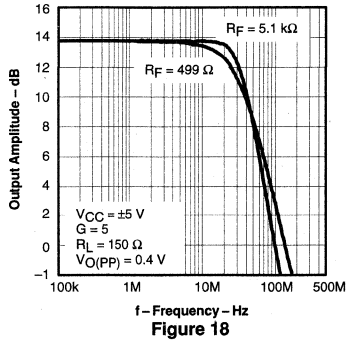


Figure 18

PREAMP OUTPUT AMPLITUDE vs FREQUENCY

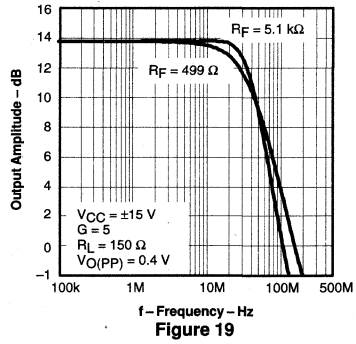


Figure 19

TYPICAL CHARACTERISTICS

PREAMP LARGE AND SMALL SIGNAL FREQUENCY RESPONSE

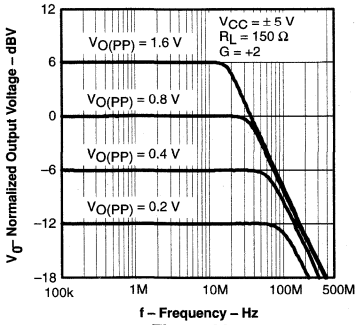


Figure 20

PREAMP LARGE AND SMALL SIGNAL FREQUENCY RESPONSE

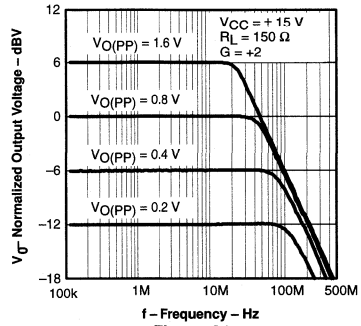


Figure 21

PREAMP HARMONIC DISTORTION vs FREQUENCY

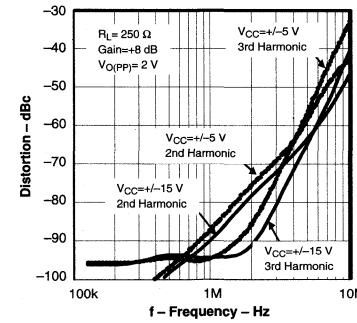


Figure 22

PREAMP HARMONIC DISTORTION vs OUTPUT VOLTAGE

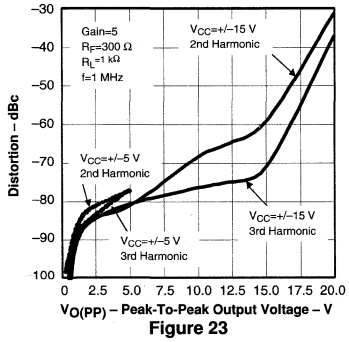


Figure 23

PREAMP SLEW RATE vs FREE-AIR TEMPERATURE

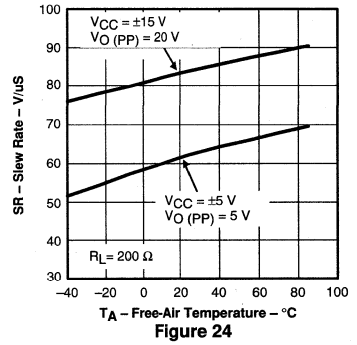


Figure 24

PREAMP 400-mV STEP RESPONSE

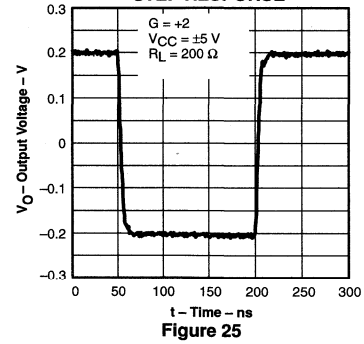


Figure 25

PREAMP 5-V STEP RESPONSE

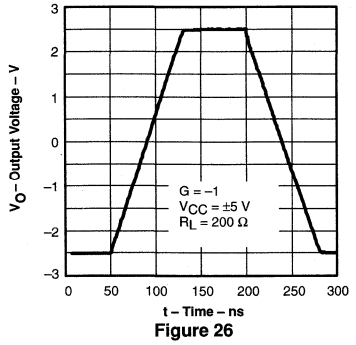


Figure 26

PREAMP 5-V STEP RESPONSE

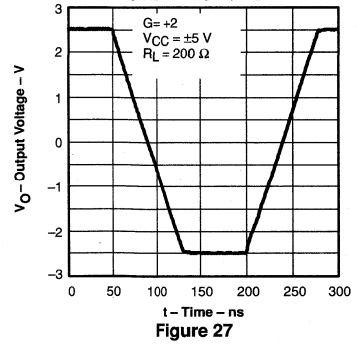


Figure 27

PREAMP 20-V STEP RESPONSE

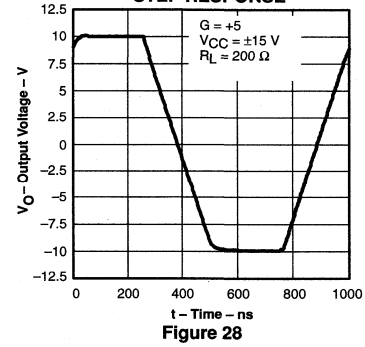


Figure 28

TYPICAL CHARACTERISTICS

THS7002 PREAMP CHANNEL-TO-CHANNEL CROSSTALK

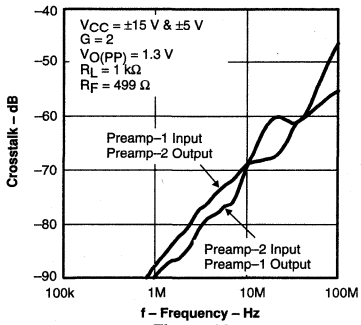


Figure 29

PREAMP-TO-PGA CROSSTALK vs FREQUENCY

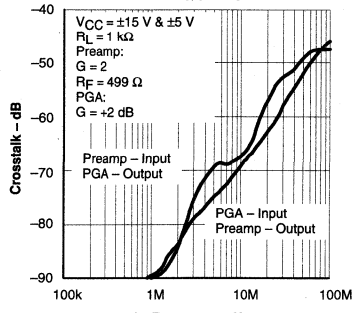


Figure 30

PGA INPUT REFERRED VOLTAGE NOISE vs FREQUENCY

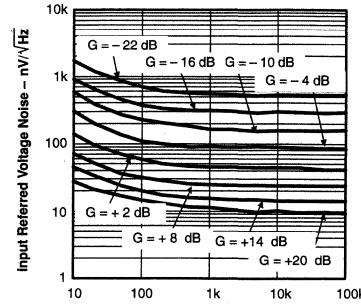


Figure 31

PGA CHANNEL-TO-CHANNEL GAIN ACCURACY vs GAIN SETTING

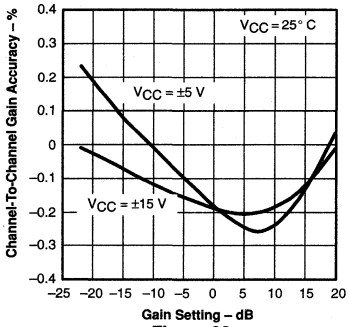


Figure 32

NORMALIZED PGA GAIN ACCURACY vs TEMPERATURE

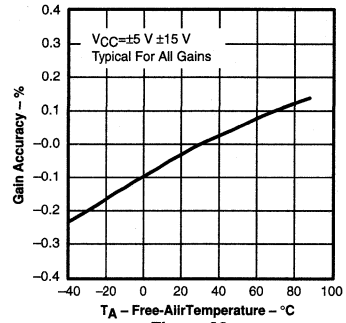


Figure 33

PGA FREQUENCY RESPONSE

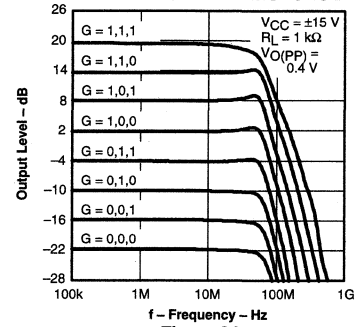


Figure 34

PGA FREQUENCY RESPONSE

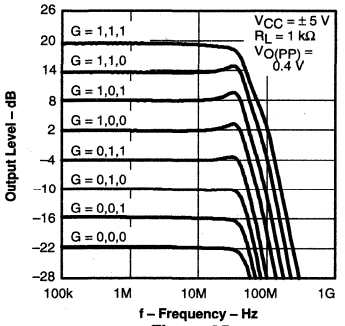


Figure 35

PGA LARGE AND SMALL SIGNAL FREQUENCY RESPONSE

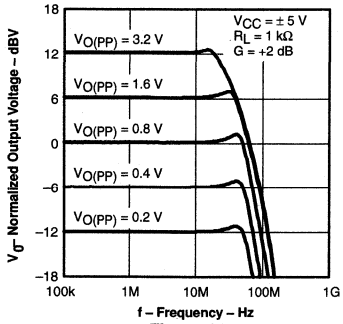


Figure 36

PGA LARGE AND SMALL SIGNAL FREQUENCY RESPONSE

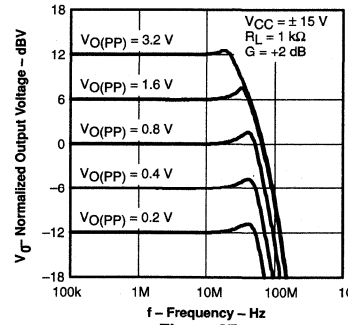


Figure 37

TYPICAL CHARACTERISTICS

PGA HARMONIC DISTORTION vs FREQUENCY

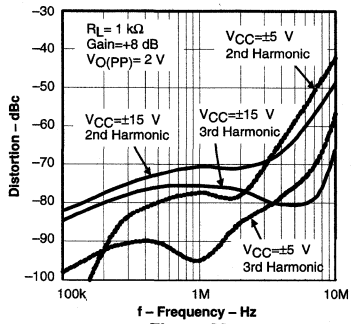


Figure 38

PGA HARMONIC DISTORTION vs OUTPUT VOLTAGE

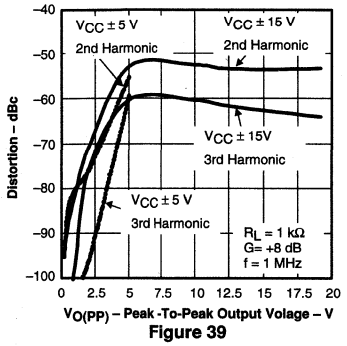


Figure 39

PGA SLEW RATE vs FREE-AIR TEMPERATURE

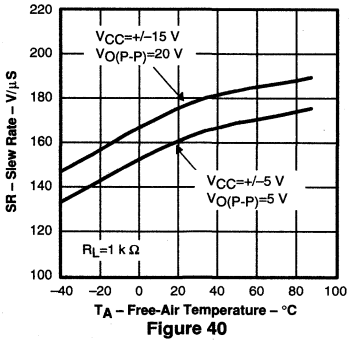


Figure 40

PGA CLAMP ACCURACY vs FREE-AIR TEMPERATURE

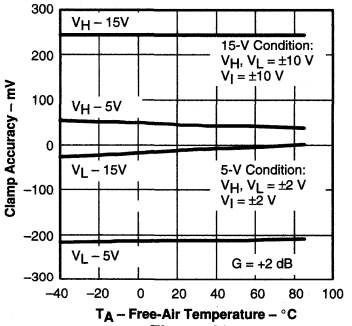


Figure 41

PGA CLAMP RESPONSE

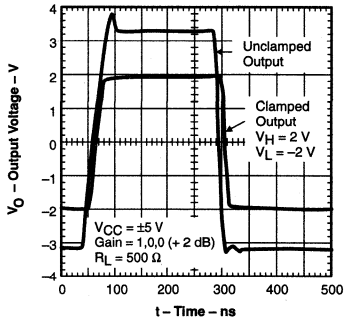


Figure 42

PGA CLAMP RESPONSE

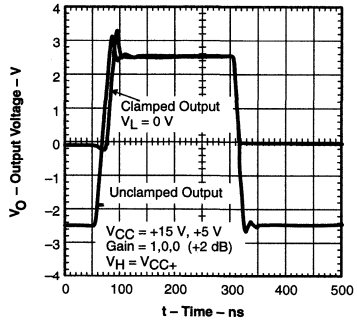


Figure 43

PGA CLAMP RESPONSE

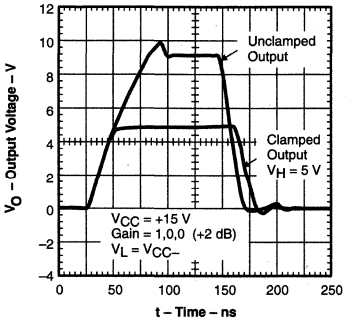


Figure 44

SHUTDOWN ISOLATION vs FREQUENCY

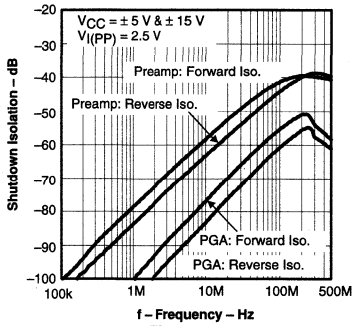


Figure 45

PGA SHUTDOWN RESPONSE

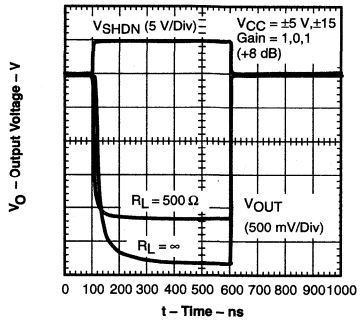


Figure 46

TYPICAL CHARACTERISTICS

PGA SHUTDOWN RESPONSE

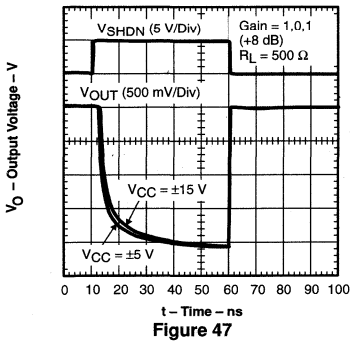


Figure 47

PREAMP SHUTDOWN RESPONSE

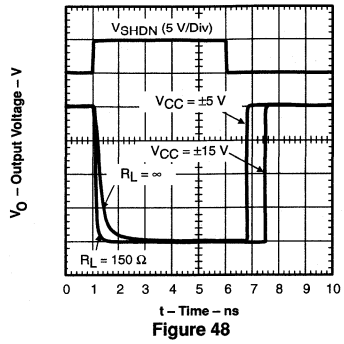


Figure 48

PGA 5-V STEP RESPONSE

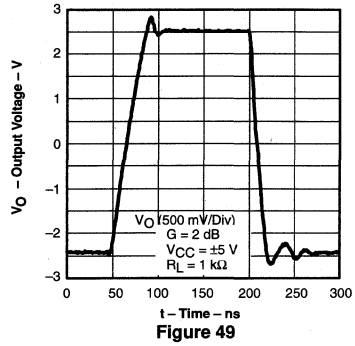


Figure 49

PGA 20-V STEP RESPONSE

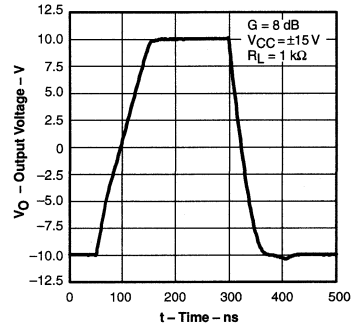


Figure 50

APPLICATION INFORMATION

theory of operation

Each section of the THS7001 and THS7002 consists of a pair of high speed operational amplifiers configured in a voltage feedback architecture. They are built using a 30-V, dielectrically isolated, complementary bipolar process with NPN and PNP transistors possessing f_Ts of several GHz. This results in exceptionally high performance amplifiers that have a wide bandwidth, high slew rate, fast settling time, and low distortion. A simplified schematic of the preamplifiers are shown in Figure 51.

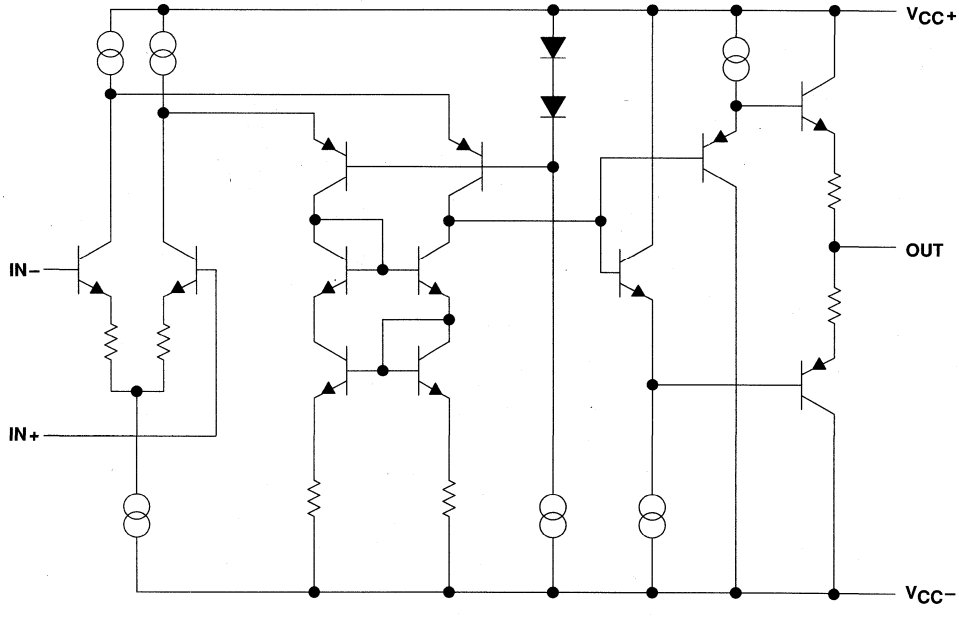


Figure 51. Pre-Amp Simplified Schematic

noise calculations and noise figure

Noise can cause errors on very small signals. This is especially true for the preamplifiers, which typically amplify small signals. The noise model is shown in Figure 52. This model includes all of the noise sources as follows:

- e_n = amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = noninverting current noise (pA/$\sqrt{Hz}$)
- IN– = inverting current noise (pA/$\sqrt{Hz}$)
- e_{Rx} = thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR_x)

APPLICATION INFORMATION

noise calculations and noise figure (continued)

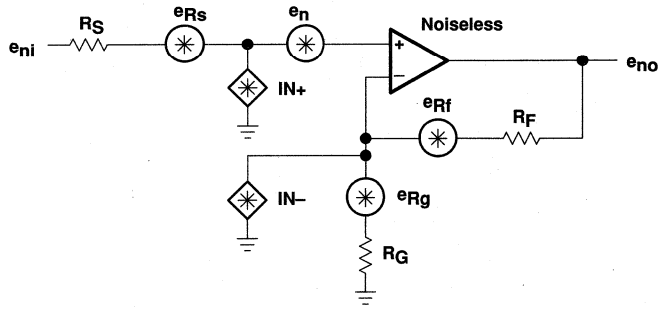


Figure 52. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN + \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\ kTR_s + 4\ kT\left(R_F \parallel R_G\right)} \quad (1)$$

Where:

k = Boltzmann's constant = 1.380658×10^{-23}
T = temperature in degrees Kelvin (273 +°C)
$R_F \parallel R_G$ = parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\ A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)} \quad (2)$$

As the previous equations show, to keep noise at a minimum, small value resistors should be used. As the closed-loop gain is increased (by reducing $R_F + R_G$), the input noise can be reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

By using the low noise preamplifiers as the first element in the signal chain, the input signal's signal-to-noise ratio (SNR) is maintained throughout the entire system. This is because the dominant system noise is due to the first amplifier. This can be seen with the following example:

APPLICATION INFORMATION

noise calculations and noise figure (continued)

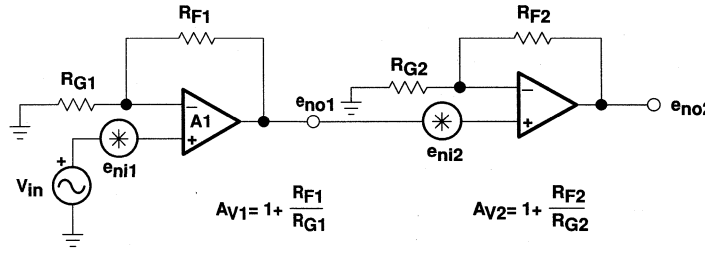


Figure 53. Simplified Composite Amplifier System

The noise due to amplifier 1 (A1) is the same as derived in equations 1 and 2. The composite system noise is calculated as follows:

$$e_{no2} = \sqrt{e_{ni2}^2 + e_{no1}^2} \times A_{V2}$$

$$= \sqrt{e_{ni2}^2 + \left(e_{ni1} A_{V1}\right)^2} \times A_{V2} \quad (3)$$

In a typical system, amplifier 1 (A1) has a large gain (A_{V1}). Because the noise is summed in the RMS method, if the A1 output noise is more than 25% larger than the input noise of amplifier 2, the contribution of amplifier 2's input noise to the composite amplifier output noise can effectively be ignored. This reduces equation 3 down to:

$$e_{no2} \cong e_{ni1}\ A_{V1}\ A_{V2} \quad (4)$$

Equation 4 shows that the very first amplifier (the preamplifier) is critical in any low-level signal system. This also shows that practically any noisy amplifier can be used after the preamplifier with minimal SNR degradation.

For more information on noise analysis, please refer to the *Noise Analysis* section in *Operational Amplifier Circuits Applications Report* (literature number SLVA043).

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^2}{\left(e_{Rs}\right)^2}\right]$$

APPLICATION INFORMATION

noise calculations and noise figure (continued)

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN + \times R_S\right)^2\right]}{4\ kTR_S}\right]$$

Figure 54 shows the noise figure graph for the THS7001 and THS7002.

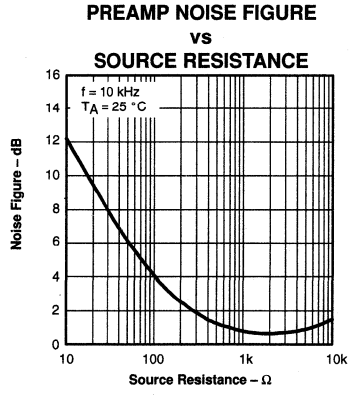


Figure 54. Noise Figure vs Source Resistance

optimizing frequency response for the preamplifiers

Internal frequency compensation of the THS7001 and THS7002 was selected to provide very wide bandwidth performance and still maintain a very low noise floor. In order to meet these performance requirements, the preamplifiers must have a minimum gain of 2 (–1). Because everything is referred to the noninverting terminal of an operational amplifier, the noise gain in a G = –1 configuration is the same as a G = 2 configuration.

One of the keys of maintaining a smooth frequency response, and hence, a stable pulse response, is to pay particular attention to the inverting terminal. Any stray capacitance at this node causes peaking in the frequency response. There are two things that can be done to help minimize this effect. The first is to simply remove any ground planes under the inverting terminal of the amplifier. This also includes the trace that connects to this terminal. Additionally, the length of this trace should be minimized. The capacitance at this node causes a lag in the voltage being fed back due to the charging and discharging of the stray capacitance. If this lag becomes too long, the amplifier will not be able to correctly keep the noninverting terminal voltage at the same potential as the inverting terminal's voltage. Peaking and possibly oscillations can occur if this happens.

APPLICATION INFORMATION

optimizing frequency response for the preamplifiers (continued)

The next thing that helps to maintain a smooth frequency response is to keep the feedback resistor (R_f) and the gain resistor (R_g) values fairly low. These two resistors are effectively in parallel when looking at the ac small-signal response. This is why in a configuration with a gain of 5, a feedback resistor of 5.1 kΩ with a gain resistor of 1.2 kΩ only shows a small peaking in the frequency response. The parallel resistance is less than 1 kΩ. This value, in conjunction with a very small stray capacitance test PCB, forms a zero on the edge of the amplifier's natural frequency response. To eliminate this peaking, all that needs to be done is to reduce the feedback and gain resistances. One other way to compensate for this stray capacitance is to add a small capacitor in parallel with the feedback resistor. This helps to neutralize the effects of the stray capacitance. To keep this zero out of the operating range, the stray capacitance and resistor value's time constant must be kept low. But, as can be seen in Figures 14 – 19, a value too low starts to reduce the bandwidth of the amplifier. Table 1 shows some recommended feedback resistors to be used with the THS7001 and THS7002 preamplifiers.

Table 2. Recommended Feedback Resistors

GAIN	R_f for V_{CC} = ±15 V and ± 5 V
2	499 Ω
–1	499 Ω
5	1 kΩ

PGA gain control

The PGA section of the THS7001 and THS7002 IC allows for digital control of the gain. There are three digital control pins for each side of the PGA (AG0 – AG2, and BG0 – BG2). Standard TTL or CMOS Logic will control these pins without any difficulties. The applied logic levels are referred to the DGND pins of the THS7002. The gain functions are not latched and therefore always rely on the logic at these pins to maintain the correct gain settings. A 3.3 kΩ resistor to ground is usually applied at each input to ensure a fixed logic state. The gain control acts like break-before-make SPDT switches. Because of this action, the PGA will go into an open-loop condition. This may cause the output to behave unpredictably until the switches closes in less than 1.5 µs. Due to the topology of this circuit, the controlling circuitry must be able to sink up to 2 µA of current when 0-V is applied to the gain control pin. A simplified circuit diagram of the gain control circuitry is shown in Figure 55.

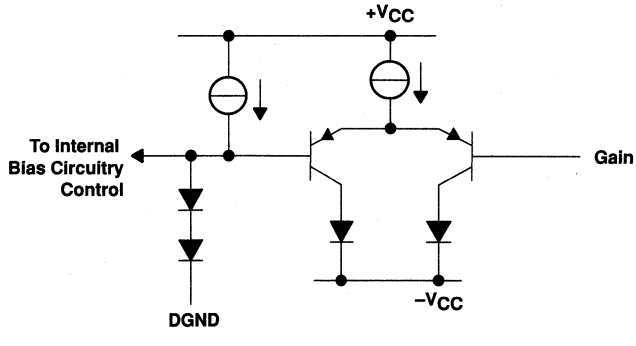


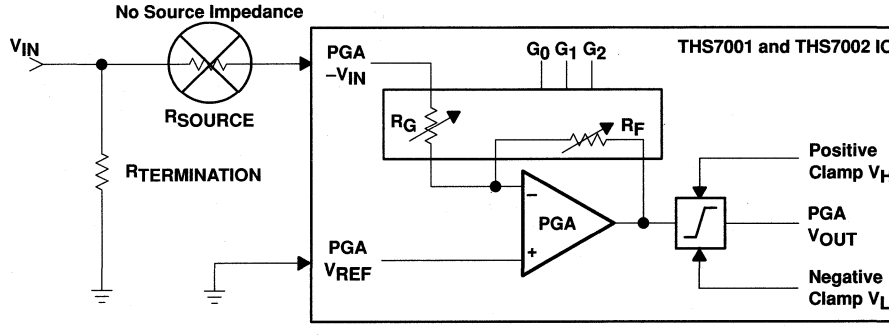
Figure 55. Simplified PGA Gain Control

APPLICATION INFORMATION

PGA gain control (continued)

One aspect of the THS7001 and THS7002 PGA signal inputs is that there are internal variable resistors (R_F and R_G), which set the gain. The resistance of R_G changes from about 270-Ω (Gain = +20 dB) to about 3-kΩ (Gain = –22 dB). Therefore, any source impedance at the input to the PGA amplifiers will cause a gain error to be seen at the output. A buffer/amplifier is highly recommended to directly drive the input of the PGA section to help minimize this effect.

Another thing which should be kept in mind is that when each amplifier's V_{REF} is connected to ground, the internal R_G resistor is connected to a virtual ground. Therefore, if a termination resistor is used on the source side, the total terminating resistance is the parallel combination of the terminating resistance and the internal R_G resistor. This, in conjunction with the series impedance problem mentioned previously, can potentially cause a voltage mismatch between the output of a 50-Ω source and the expected PGA output voltage. These points can be easily seen in the simplified diagram of the THS7001 and THS7002 PGA section (see Figure 56).



$$R_{TOTAL\ TERMINATION} = \frac{R_{TERMINATION} \times (R_{SOURCE} + R_G)}{R_{TERMINATION} + (R_{SOURCE} + R_G)}$$

Figure 56. Simplified PGA Section of the THS7001 and THS7002

voltage reference terminal

If a voltage is applied to the PGA's V_{REF} terminal, then the output of the PGA section will amplify the applied reference voltage by one plus the selected gain. Thus, the output gain strictly due to V_{REF} will be from +0.6 dB to +21 dB according to the following formula:

$$\frac{V_{OUT}}{V_{REF}} = 20 \text{ X } \text{Log}_{10}[1 + (\text{PGA Gain(V/V)})]$$

For most configurations, it is recommended that this pin be connected to the signal ground.

APPLICATION INFORMATION

output clamping

Typically, the output of the PGA will directly drive an analog-to-digital converter (ADC). Because of the limited linear input range and saturation characteristics of most ADCs, the PGA's outputs incorporate a voltage clamp. Unlike a lot of clamping amplifiers which clamp only at the input, the THS7001 and THS7002 clamps at the output stage. This insures that the output will always be protected regardless of the Gain setting and the input voltage. The clamps activate almost instantaneously and recover from saturation in less than 7 ns. This can be extremely important when the THS7001 and THS7002 is used to drive some ADCs which have a very long overdrive recovery time. It is also recommended to add a pair of high frequency bypass capacitors to the clamp inputs. These capacitors will help eliminate any ringing which may ocur when a large pulse is applied to the amplifier. This pulse will force the clamp diodes to abruptly turn on, drawing current from the reference voltages. Just like a power supply trace, you must minimize the inductance seen by the clamp pins. The bypass capacitors will supply the sudden current demands when the clamps are suddenly turned on. A simplified clamping circuit diagram is shown in Figure 57.

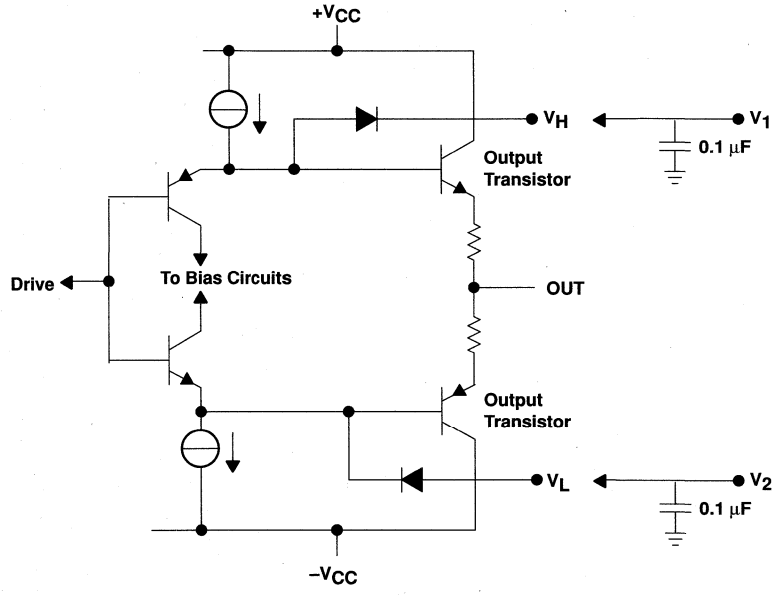


Figure 57. Simplified THS7001 and THS7002 Clamp Circuit

Because the internal clamps utilize the same clamping reference voltages, the outputs of both PGAs on the THS7002 are clamped to the same values. These clamps are typically connected to the power supply pins to allow a full output range. But, they can be connected to any voltage reference desired. The clamping range is limited to $+V_{CC}$ and GND for V_H and $-V_{CC}$ and GND for V_L. It is possible to go beyond GND for each respective clamp, but it is not recommended. This is because this operation relies on the internal bias currents in the Class AB output stage to maintain their linearity. There may also be a chance to reverse bias the PN junctions and possibly cause internal damage to these junctions. But for reference, the graphs in Figure 58 show the output voltage versus the clamping voltage with different loads.

APPLICATION INFORMATION

output clamping (continued)

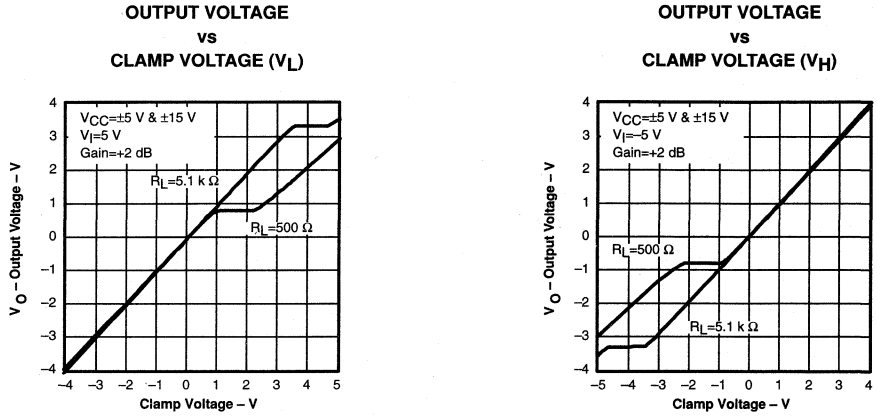


Figure 58. Output Voltage vs Clamp Voltage

The accuracy of this clamp is dependant on the amount of current flowing through the internal clamping diodes. As is typical with all diodes, the voltage drop across this diode increases with current. Therefore, the accuracy of the clamp is highly dependant upon the output voltage, the clamping voltage difference, and the output current. The accuracy of the clamps with different load resistances are shown in Figure 59.

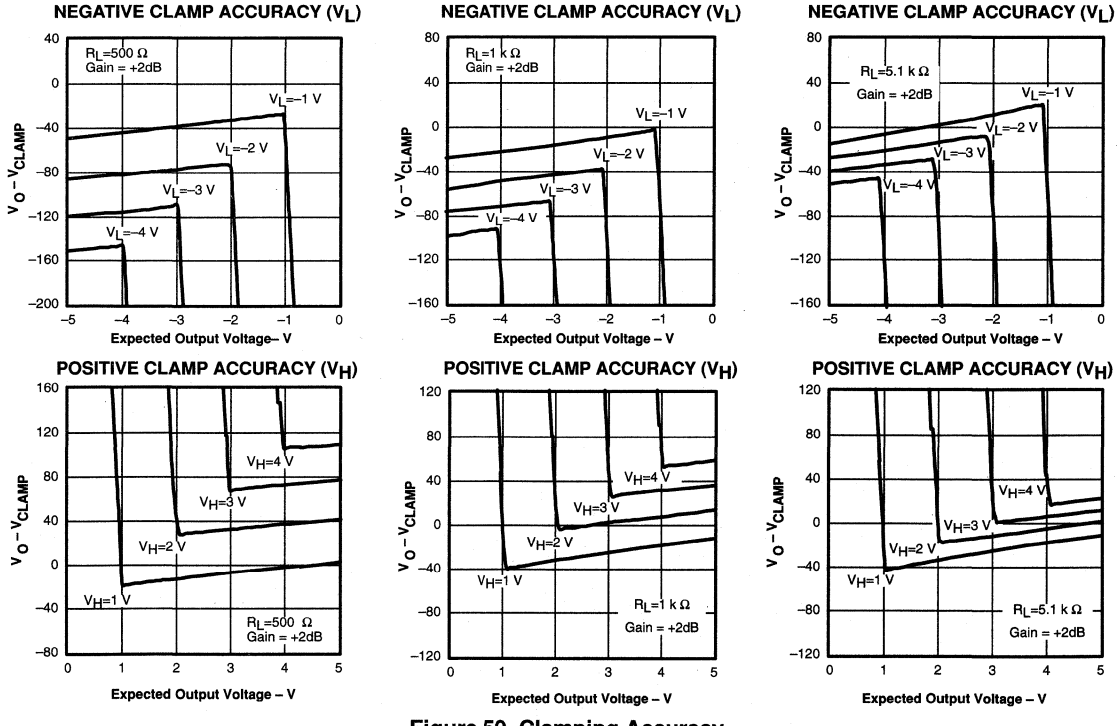


Figure 59. Clamping Accuracy

APPLICATION INFORMATION

shutdown control

There are two shutdown pins which control the shutdown for each half of the THS7002 and one shutdown pin for the THS7001. When the shutdown pins signals are low, the THS7001 and THS7002 is active. But, when a shutdown pin is high (+5 V), a preamplifier and the respective PGA section is turned off. Just like the Gain controls, the shutdown logic is not latched and should always have a signal applied to them. A 3.3-kΩ resistor to ground is usually applied to ensure a fixed logic state. A simplified circuit can be seen in Figure 60.

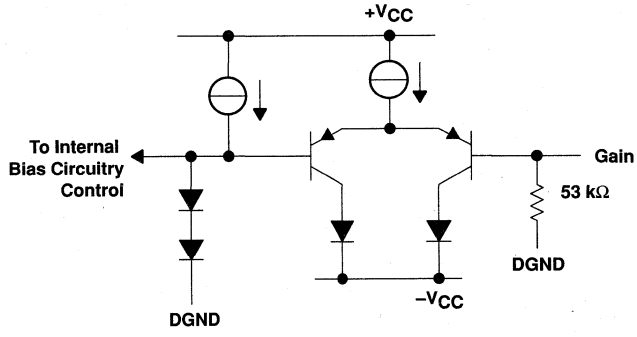


Figure 60. Simplified THS7001 and THS7002 Shutdown Circuit

One aspect of the shutdown feature, which is often over-looked, is that the PGA section will still have an output while in shutdown mode. This is due to the internally fixed R_F and R_G resistors. This effect is true for any amplifier connected as an inverter. The internal circuitry may be powered down and in a high-impedance state, but the resistors are always there. This will then allow the input signal current to flow through these resistors and into the output. The equivalent resistance of R_F and R_G is approximately 3 kΩ. To minimize this effect, a shunt resistor to ground may be utilized, This will act as a classic voltage divider and will reduce the feed-through voltage seen at the PGA output. The drawback to this is the increased load on the PGA while in the active state.

driving a capacitive load

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS7001 and THS7002 has been internally compensated to maximize its bandwidth and slew rate performance. When an amplifier is compensated in this manner, capacitive loading directly on the output will decrease the device's phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 61. A minimum value of 20 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

APPLICATION INFORMATION

driving a capacitive load (continued)

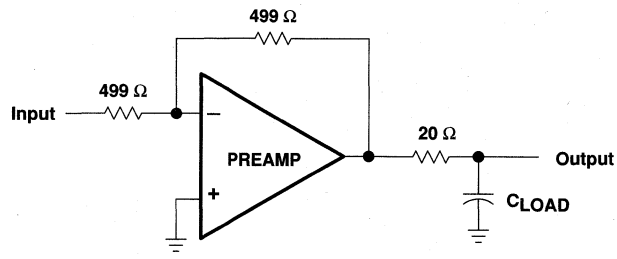
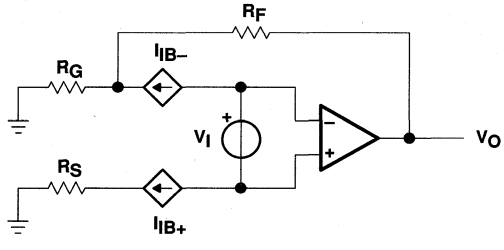


Figure 61. Driving a Capacitive Load

offset voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:

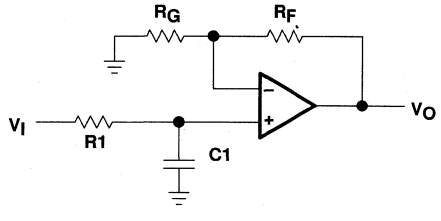


$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB+}\, R_S \left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-}\, R_F$$

Figure 62. Output Offset Voltage Model

general configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal of the THS7001 and THS7002 preamplifier (see Figure 63).



$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

$$\frac{V_O}{V_I} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR1C1}\right)$$

Figure 63. Single-Pole Low-Pass Filter

APPLICATION INFORMATION

general configurations (continued)

If even more attenuation is needed, a multiple-pole filter is required. The Sallen-Key filter can be used for this task. For best results, the THS7001 and THS7002 preamplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do this can result in phase shift of the amplifier.

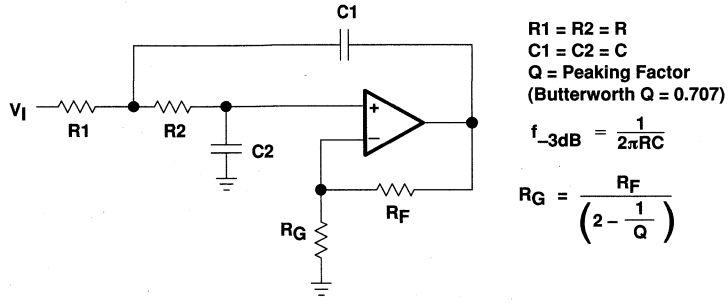


Figure 64. 2-Pole Low-Pass Sallen-Key Filter

ADSL

The ADSL receive band consists of up to 255 separate carrier frequencies each with its own modulation and amplitude level. With such an implementation, it is imperative that signals received off the telephone line have as high a signal-to-noise ratio (SNR) as possible. This is because of the numerous sources of interference on the line. The best way to accomplish this high SNR is to have a low-noise preamplifier on the front-end. It is also important to have the lowest distortion possible to help minimize against interference within the ADSL carriers. The THS7001 and THS7002 was designed with these two priorities in mind.

By taking advantage of the superb characteristics of the complimentary bipolar process (BICOM), the THS7001 and THS7002 offers extremely low noise and distortion while maintaining a high bandwidth. There are some aspects that help minimize distortion in any amplifier. The first is to extend the bandwidth of the amplifier as high as possible without peaking. This allows the amplifier to eliminate any nonlinearities in the output signal. Another thing that helps to minimize distortion is to increase the load impedance seen by the amplifier, thereby reducing the currents in the output stage. This will help keep the output transistors in their linear amplification range and will also reduce the heating effects.

One central-office side terminal circuit implementation, shown in Figure 65, uses a 1:2 transformer ratio. While creating a power and output voltage advantage for the line drivers, the 1:2 transformer ratio reduces the SNR for the received signals. The ADSL standard, ANSI T1.413, stipulates a noise power spectral density of –140 dBm/Hz, which is equivalent to 31.6 nV/$\sqrt{\text{Hz}}$ for a 100 Ω system. Although many amplifiers can reach this level of performance, actual ADSL system testing has indicated that the noise power spectral density may typically be ≤ –150 dBm/Hz, or ≤ 10 nV/$\sqrt{\text{Hz}}$. With a transformer ratio of 1:2, this number reduces to less than 5 nV/$\sqrt{\text{Hz}}$. The THS7002 preamplifiers, with an equivalent input noise of 1.7 nV/$\sqrt{\text{Hz}}$, is an excellent choice for this application. Coupled with a very low 0.9 pA/$\sqrt{\text{Hz}}$ equivalent input current noise and low value resistors, the THS7001 and THS7002 will ensure that the received signal SNR will be as high as possible.

APPLICATION INFORMATION

ADSL (continued)

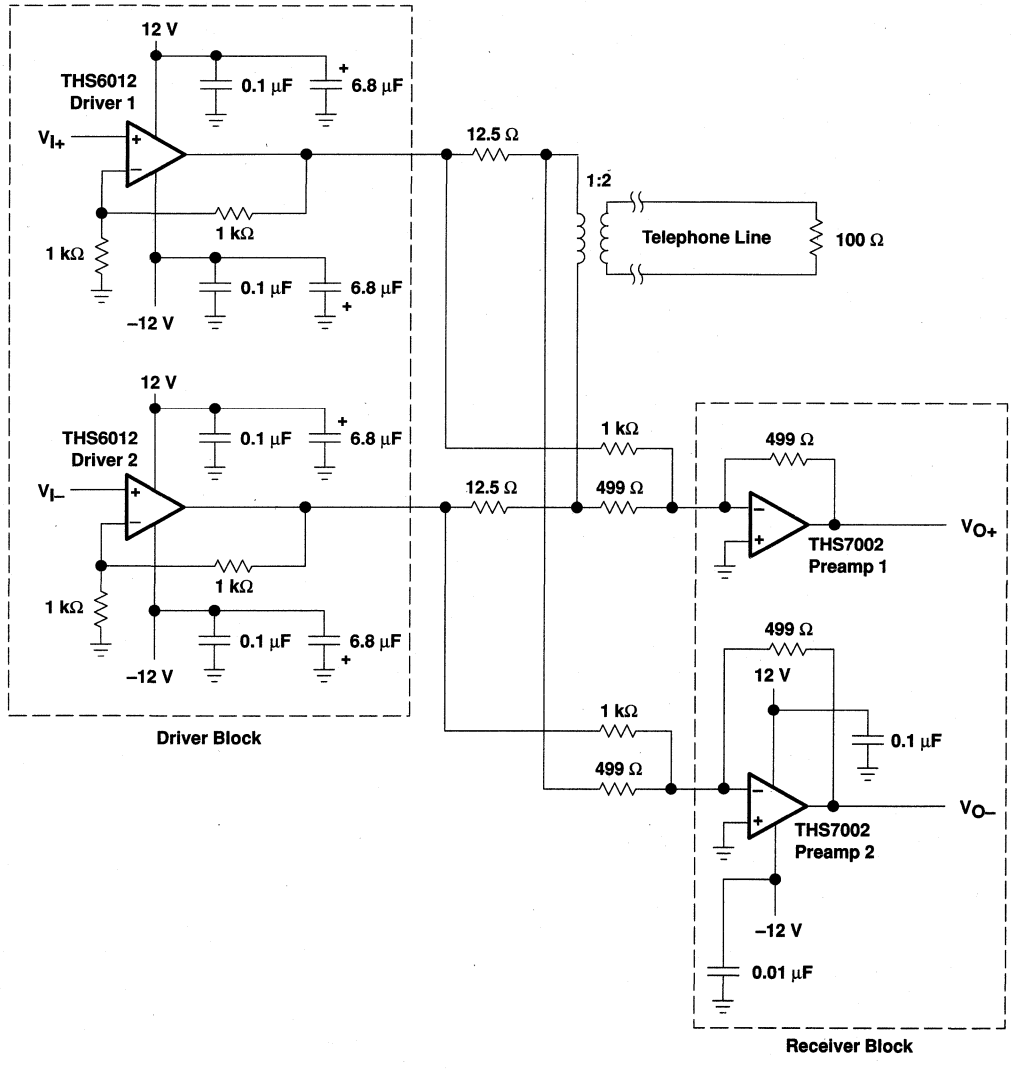


Figure 65. THS7002 Central-Office ADSL Application

APPLICATION INFORMATION

ADSL (continued)

Typically, the outputs of the preamplifiers are carried into a CODEC, which incorporates an analog-to-digital converter (ADC). The problem with this setup is that it only uses fixed gain elements. But, when the client is close to the central office, the gain must be set to receive a high-level signal; or for the opposite, set to receive a low-level signal. To solve this problem, a programmable-gain amplifier (PGA) should be used. The THS7001 and THS7002 PGAs allow the gain of the receiver signals to be varied from –22 dB to 20 dB. By allowing the gains to be controlled with a TTL-compatible signal, it is very easy to integrate the THS7001 and THS7002 into any system.

By having the preamplifier output separate from the PGA input, inserting more amplifiers into the system can be accomplished easily. The functionality of the amplifier is typically as an active fixed gain filter. This is shown in Figure 66.

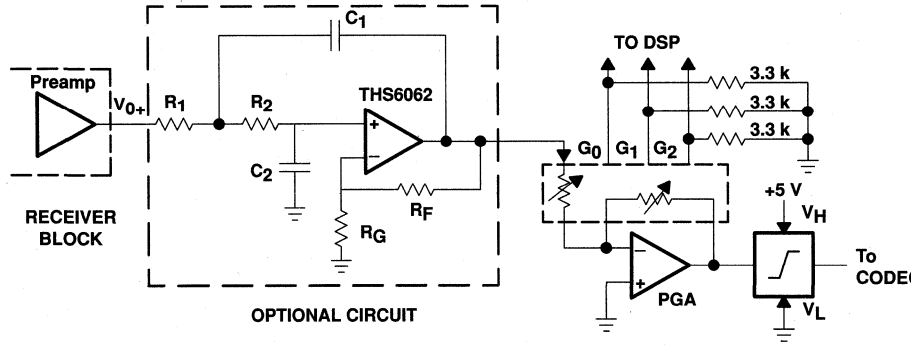


Figure 66. Typical PGA Setup (One Channel)

circuit layout considerations

In order to achieve the levels of high-frequency performance of the THS7001 and THS7002, it is essential that proper printed-circuit board high-frequency design techniques be followed. A general set of guidelines is given below. In addition, a THS7001 and THS7002 evaluation board is available to use as a guide for layout or for evaluating the device performance.

- Ground planes—It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.

APPLICATION INFORMATION

circuit layout considerations (continued)

- Short trace runs/compact part placements—Optimum high-frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This will help to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

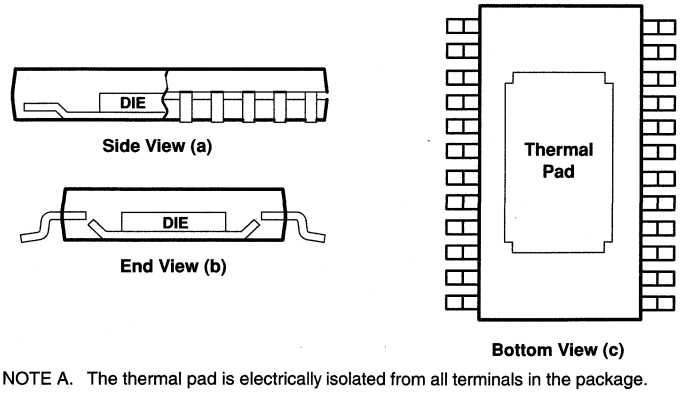
thermal information

The THS7001 and THS7002 is supplied in a thermally-enhanced PWP package, which is a member of the PowerPAD. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 67(a) and Figure 67(b)]. This arrangement exposes the lead frame as a thermal pad on the underside of the package [see Figure 67(c)]. Because this pad has direct contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area requirement and ease of assembly of surface mount with the heretofore awkward mechanical methods of heatsinking.

thermal information (continued)



NOTE A. The thermal pad is electrically isolated from all terminals in the package.

Figure 67. Views of Thermally Enhanced PWP Package

APPLICATION INFORMATION

general PowerPAD design considerations

Although there are many ways to properly heatsink this device, the following steps illustrate the recommended approach.

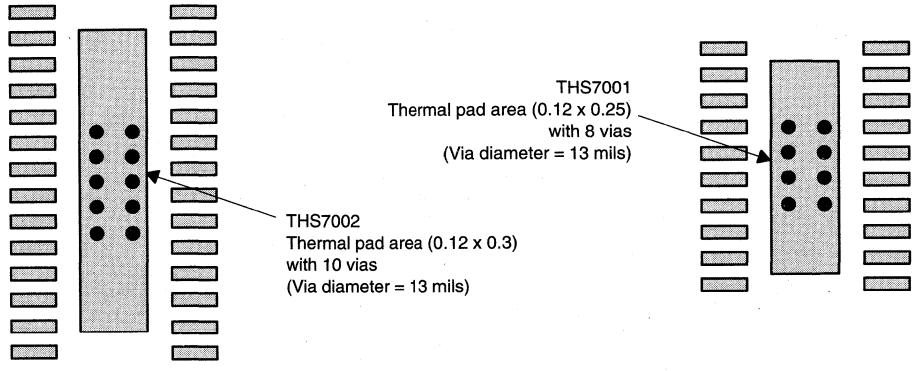


Figure 68. PowerPAD PCB Etch and Via Pattern

1. Prepare the PCB with a top side etch pattern as shown in Figure 68. There should be etch for the leads as well as etch for the thermal pad.
2. Place the thermal transfer holes in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the IC package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its thermal transfer holes exposed. The bottom-side solder mask should cover the thermal transfer holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the THS7001PWP/THS7002PWP IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

APPLICATION INFORMATION

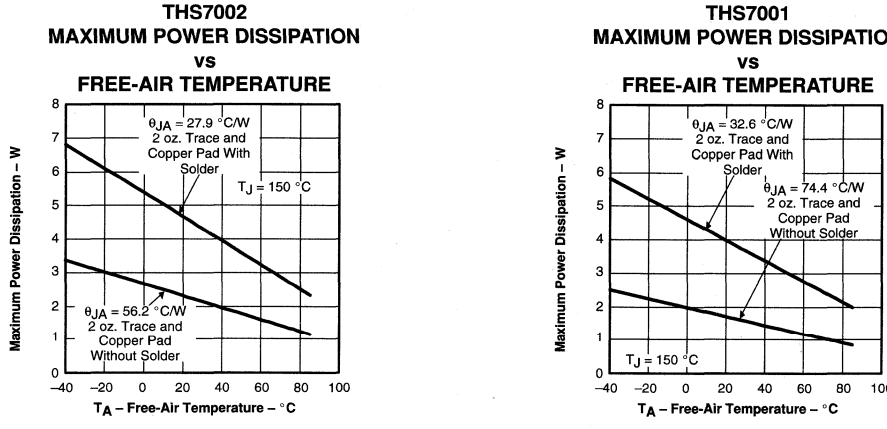
general PowerPAD design considerations (continued)

The actual thermal performance achieved with the THS7001PWP/THS7002PWP in its PowerPAD package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches × 3 inches, then the expected thermal coefficient, θ_{JA}, is about 32.6°C/W for the THS7001 and 27.9°C/W for the THS7002. For a given θ_{JA}, the maximum power dissipation is shown in Figure 69 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

P_D = Maximum power dissipation of THS7001 and THS7002 IC (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Free-ambient air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case (THS7001 = 1.4°C/W; THS7002 = 0.72°C/W)
θ_{CA} = Thermal coefficient from case to ambient air (°C/W)



NOTE A. Results are with no air flow and PCB size = 3"× 3"

Figure 69. Maximum Power Dissipation vs Free-Air Temperature

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments technical brief, *PowerPAD Thermally Enhanced Package.* This document can be found at the TI web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number SLMA002 when ordering.

evaluation board

An evaluation board is available both the THS7001 (literature number SLOP250) and for the THS7002 (literature number SLOP136). These boards has been configured for very low parasitic capacitance in order to realize the full performance of the amplifiers. These EVM's incorporate DIP switches to demonstrate the full capabilities of the THS7001 and THS7002 independent of any digital control circuitry. For more information, please refer to the *THS7001 EVM User's Guide* (literature number SLOU057)and the *THS7002 EVM User's Guide* (literature number SLOU037). To order a evaluation board contact your local TI sales office or distributor.

Contents

Analysis of the Sallen-Key Architecture

Literature Number: SL0A024A
July 1999

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Contents

List of Figures

Analysis of the Sallen-Key Architecture

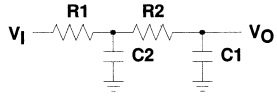
James Karki

ABSTRACT

This application report discusses the Sallen-Key architecture. The report gives a general overview and derivation of the transfer function, followed by detailed discussions of low-pass and high-pass filters, including design information, and ideal and non-ideal operation. To illustrate the limitations of real circuits, data on low-pass and high-pass filters using the Texas Instruments THS3001 is included. Finally, component selection is discussed.

1 Introduction

Figure 1 shows a two-stage RC network that forms a second order low-pass filter. This filter is limited because its Q is always less than 1/2. With R1=R2 and C1=C2, Q=1/3. Q approaches the maximum value of 1/2 when the impedance of the second RC stage is much larger than the first. Most filters require Qs larger than 1/2.



$$\frac{Vo}{Vi} = \frac{1}{s^2(R1C2R2C1) + s(R1C2 + R2C1 + R1C1) + 1}$$

Figure 1. Basic Second Order Low-Pass Filter

Larger Qs are attainable by using a positive feedback amplifier. If the positive feedback is controlled—localized to the cut-off frequency of the filter—almost any Q can be realized, limited mainly by the physical constraints of the power supply and component tolerances. Figure 2 shows a unity gain amplifier used in this manner. Capacitor C2, no longer connected to ground, provides a positive feedback path. In 1955, R. P. Sallen and E. L. Key described these filter circuits, and hence they are generally known as Sallen-Key filters.

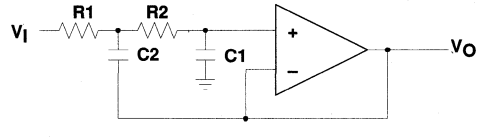


Figure 2. Unity Gain Sallen-Key Low-Pass Filter

The operation can be described qualitatively:

- At low frequencies, where C1 and C2 appear as open circuits, the signal is simply buffered to the output.
- At high frequencies, where C1 and C2 appear as short circuits, the signal is shunted to ground at the amplifier's input, the amplifier amplifies this input to its output, and the signal does not appear at Vo.
- Near the cut-off frequency, where the impedance of C1 and C2 is on the same order as R1 and R2, positive feedback through C2 provides Q enhancement of the signal.

2 Generalized Circuit Analysis

The circuit shown in Figure 3 is a generalized form of the Sallen-Key circuit, where generalized impedance terms, Z, are used for the passive filter components, and R3 and R4 set a non-frequency dependent gain.

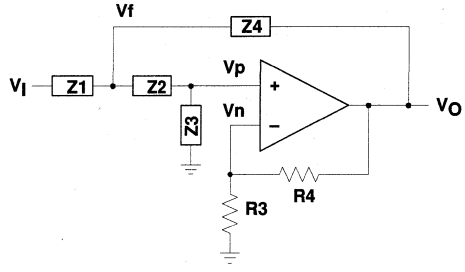


Figure 3. Generalized Sallen-Key Circuit

To find the circuit solution for this generalized circuit, find the mathematical relationships between Vi, Vo, Vp, and Vn, and construct a block diagram.

KCL at Vf:

$$Vf\left(\frac{1}{Z1}+\frac{1}{Z2}+\frac{1}{Z4}\right)=Vi\left(\frac{1}{Z1}\right)+Vp\left(\frac{1}{Z2}\right)+Vo\left(\frac{1}{Z4}\right) \tag{1}$$

KCL at Vp:

$$Vp\left(\frac{1}{Z2}+\frac{1}{Z3}\right)=Vf\left(\frac{1}{Z2}\right)\Rightarrow Vf=Vp\left(1+\frac{Z2}{Z3}\right) \tag{2}$$

Substitute Equation (2) into Equation (1) and solve for Vp:

$$Vp=Vi\left(\frac{Z2Z3Z4}{Z2Z3Z4+Z1Z2Z4+Z1Z2Z4+Z2Z2Z4+Z2Z2Z1}\right)+Vo\left(\frac{Z1Z2Z3}{Z2Z3Z4+Z1Z2Z4+Z1Z2Z4+Z2Z2Z4+Z2Z2Z1}\right) \tag{3}$$

KCL at Vn:

$$V\left(\frac{1}{R3}+\frac{1}{R4}\right)=Vo\left(\frac{1}{R4}\right)\Rightarrow Vn=Vo\left(\frac{R3}{R3+R4}\right) \tag{4}$$

2.1 Gain Block Diagram

By letting: a(f) = the open-loop gain of the amplifier, $b=\left(\frac{R3}{R3+R4}\right)$,

$c=\frac{Z2Z3Z4}{Z2Z3Z4+Z1Z2Z4+Z1Z2Z3+Z2Z2Z4+Z2Z2Z1}$,

$d=\frac{Z1Z2Z3}{Z2Z3Z4+Z1Z2Z4+Z1Z2Z3+Z2Z2Z4+Z2Z2Z1}$,

and Ve = Vp − Vn, the generalized Sallen-Key filter circuit is represented in gain-block form as shown in Figure 4.

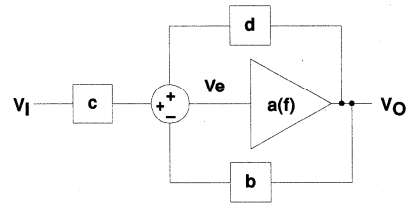


Figure 4. Gain-Block Diagram of the Generalized Sallen-Key Filter

From the gain-block diagram the transfer function can be solved easily by observing, Vo = a(f)Ve and Ve = cVi + dVo – bVo. Solving for the generalized transfer function from gain block analysis gives:

$$\frac{Vo}{Vi} = \left(\frac{c}{b}\right)\left[\frac{1}{1 + \frac{1}{a(f)b} - \frac{d}{b}}\right] \tag{5}$$

2.2 Ideal Transfer Function

Assuming a(f)b is very large over the frequency of operation, $\frac{1}{a(f)b} \approx 0$, the ideal transfer function from gain block analysis becomes:

$$\frac{Vo}{Vi} = \left(\frac{c}{b}\right)\left[\frac{1}{1 - \frac{d}{b}}\right] \tag{6}$$

By letting $\frac{1}{b} = K$, $c = \frac{N1}{D}$, and $d = \frac{N2}{D}$, where N1, N2, and D are the numerators and denominators shown above, the ideal equation can be rewritten as:

$\frac{Vo}{Vi} = \left[\frac{K}{\frac{D}{N1} - \frac{K \cdot N2}{N1}}\right]$. Plugging in the generalized impedance terms gives the ideal transfer function with impedance terms:

$$\frac{Vo}{Vi} = \frac{K}{\frac{Z1Z2}{Z3Z4} + \frac{Z1}{Z3} + \frac{Z2}{Z3} + \frac{Z1(1-K)}{Z4} + 1} \tag{7}$$

3 Low-Pass Circuit

The standard frequency domain equation for a second order low-pass filter is:

$$H_{LP} = \frac{K}{-\left(\frac{f}{fc}\right)^2 + \frac{jf}{Qfc} + 1} \tag{8}$$

Where fc is the corner frequency and Q is the quality factor. When f<<fc Equation (8) reduces to K, and the circuit passes signals multiplied by a gain factor K. When f=fc, Equation (8) reduces to –jKQ, and signals are enhanced by the factor Q. When f>>fc, Equation (8) reduces to $-K\left(\frac{fc}{f}\right)^2$, and signals are attenuated by the square of the frequency ratio. With attenuation at higher frequencies increasing by a power of 2, the formula describes a second order low-pass filter.

Figure 5 shows the Sallen-Key circuit configured for low-pass:

$Z1 = R1,\ Z2 = R2,\ Z3 = \frac{1}{sC1}$,

$Z4 = \frac{1}{sC2}$, and $K = 1 + \frac{R4}{R3}$.

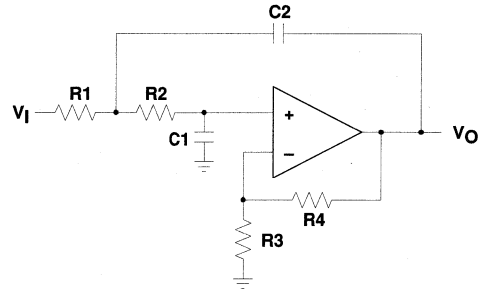


Figure 5. Low-Pass Sallen-Key Circuit

From Equation (7), the ideal low-pass Sallen-Key transfer function is:

$$\frac{Vo}{Vi}(lp) = \frac{K}{s^2(R1R2C1C2) + s(R1C1 + R2C1 + R1C2(1 - K)) + 1} \tag{9}$$

By letting

$s = j2\pi f,\ fc = \frac{1}{2\pi\sqrt{R1R2C1C2}}$, and $Q = \frac{\sqrt{R1R2C1C2}}{R1C1 + R2C1 + R1C2(1 - K)}$,

equation (9) follows the same form as Equation (8). With some simplifications, these equations can be dealt with efficiently; the following paragraphs discuss commonly used simplification methods.

3.1 Simplification 1: Set Filter Components as Ratios

Letting R1=mR, R2=R, C1=C, and C2=nC, results in: $fc = \frac{1}{2\pi RC\sqrt{mn}}$ and $Q = \frac{\sqrt{mn}}{m + 1 + mn(1 - K)}$. This simplifies things somewhat, but there is interaction between fc and Q. Design should start by setting the gain and Q based on m, n, and K, and then selecting C and calculating R to set fc.

Notice that $K = 1 + \frac{m + 1}{mn}$ results in $Q = \infty$. With larger values, Q becomes negative, that is, the poles move into the right half of the s-plane and the circuit oscillates. Most filters require low Q values so this should rarely be a design issue.

3.2 Simplification 2: Set Filter Components as Ratios and Gain = 1

Letting R1=mR, R2=R, C1=C, C2=nC, and K=1 results in: $fc = \frac{1}{2\pi RC\sqrt{mn}}$ and $Q = \frac{\sqrt{mn}}{m + 1}$. This keeps gain = 1 in the pass band, but again there is interaction between fc and Q. Design should start by choosing the ratios m and n to set Q, and then selecting C and calculating R to set fc.

3.3 Simplification 3: Set Resistors as Ratios and Capacitors Equal

Letting R1=mR, R2=R, and C1=C2=C, results in: $fc = \frac{1}{2\pi RC\sqrt{m}}$ and $Q = \frac{\sqrt{m}}{1 + 2m - mK}$. The reason for setting the capacitors equal is the limited selection of values in comparison with resistors.

There is interaction between setting fc and Q. Design should start with choosing m and K to set the gain and Q of the circuit, and then choosing C and calculating R to set fc.

3.4 Simplification 4: Set Filter Components Equal

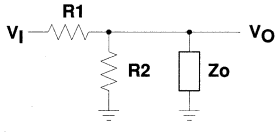
Letting R1=R2=R, and C1=C2=C, results in: $fc = \frac{1}{2\pi RC}$ and $Q = \frac{1}{3 - K}$. Now fc and Q are independent of one another, and design is greatly simplified although limited. The gain of the circuit now determines Q. RC sets fc—the capacitor chosen and the resistor calculated. One minor drawback is that since the gain controls the Q of the circuit, further gain or attenuation may be necessary to achieve the desired signal gain in the pass band.

Values of K very close to 3 result in high Qs that are sensitive to variations in the values of R3 and R4. For instance, setting K=2.9 results in a nominal Q of 10. Worst case analysis with 1% resistors results in Q=16. Whereas, setting K=2 for a Q of 1, worst case analysis with 1% resistors results in Q=1.02. Resistor values where K=3 leads to Q=∞, and with larger values, Q becomes negative, the poles move into the right half of the s-plane, and the circuit oscillates. The most frequently designed filters require low Q values and this should rarely be a design issue.

3.5 Nonideal Circuit Operation

The previous discussions and calculations assumed an ideal circuit, but there is a frequency where this is no longer a valid assumption. Logic says that the amplifier must be an active component at the frequencies of interest or else problems occur. But what problems?

As mentioned above there are three basic modes of operation: below cut-off, above cutoff, and in the area of cutoff. Assuming the amplifier has adequate frequency response beyond cut-off, the filter works as expected. At frequencies well above cut-off, the high frequency (HS) model shown in Figure 6 is used to show the expected circuit operation. The assumption made here is that C1 and C2 are effective shorts when compared to the impedance of R1 and R2 so that the amplifier's input is at ac ground. In response, the amplifier generates an ac ground at its output limited only by its output impedance, Zo. The formula shows the transfer function of this model.



$$\frac{Vo}{Vi} = \frac{1}{\frac{R1}{R2} + \frac{R1}{Zo} + 1}$$

Assuming Zo<<R1

$$\frac{Vo}{Vi} \approx \frac{Zo}{R1}$$

Figure 6. Nonideal Effect of Amplifier Output Impedance and Transfer Function

Zo is the closed-loop output impedance. It depends on the loop transmission and the open-loop output impedance, zo: $Zo = \frac{zo}{1 + a(f)b}$, where a(f)b is the loop transmission. The feedback factor, b, is constant—set by resistors R3 and R4—but the open loop gain, a(f), is dependant on frequency. With dominant pole compensation, the open-loop gain of the amplifier decreases by 20 dB/dec over the usable frequencies of operation. Assuming zo is mainly resistive (usually a valid assumption up to 100 MHz), Zo increases at a rate of 20 dB/dec. The transfer function appears to be a first order high-pass. At frequencies above 100 MHz (or so) the parasitic inductance in the output starts playing a role and the transfer function transitions to a second order high-pass. Because of stray capacitance in the circuit, at higher frequency the high-pass transfer function will also roll off.

3.6 Simulation and Lab Data

A Sallen-Key low-pass filter using the Texas Instruments THS3001 shows the effects described above. The THS3001 is a high-speed current-feedback amplifier with an advertised bandwidth of 420 MHz. No particular type of filter (i.e., Butterworth, Chebychev, Eliptic, etc.) was designed. Choosing Z1=Z2=1kΩ, Z3=Z4=1nF, R3=open, and R4=1kΩ results in a low-pass filter with fc=159 kHz, and Q=1/2.

Simulation using the spice model of the THS3001 (see the application note *Building a Simple SPICE Model for the THS3001*, SLOA018) is used to show the expected behavior of the circuit. Figure 7 shows the simulation circuits and the lab circuit tested. The results are plotted in Figure 8.

Figure 7 a) shows the simulation circuit with the spice model modified so that the output impedance is zero. Curve a) in Figure 8 shows the frequency response as simulated in spice. It shows that without the output impedance the attenuation of the signal continues to increase as frequency increases.

Figure 7 b) shows the high-frequency model shown in Figure 6 where the input is at ground and the output impedance controls the transfer function. The spice model used for the THS3001 includes the complex LRC network for the output impedance as described in the application note. Curve b) in Figure 8 shows the frequency response as simulated in spice. The magnitude of the signal at the output is seen to cross curve a) at about 7 MHz. Above this frequency the output impedance causes the switch in transfer function as described above.

Figure 7 c) shows the simulation circuit using the full spice model with the complex LCR output impedance. Curve c) in Figure 8 shows the frequency response. It shows that with the output impedance the attenuation caused by the circuit follows curve a) until it crosses curve b) at which point it follows curve b).

Figure 7 d) shows the circuit as tested in the lab, with curve d) in Figure 8 showing that the measured data agrees with the simulated data.

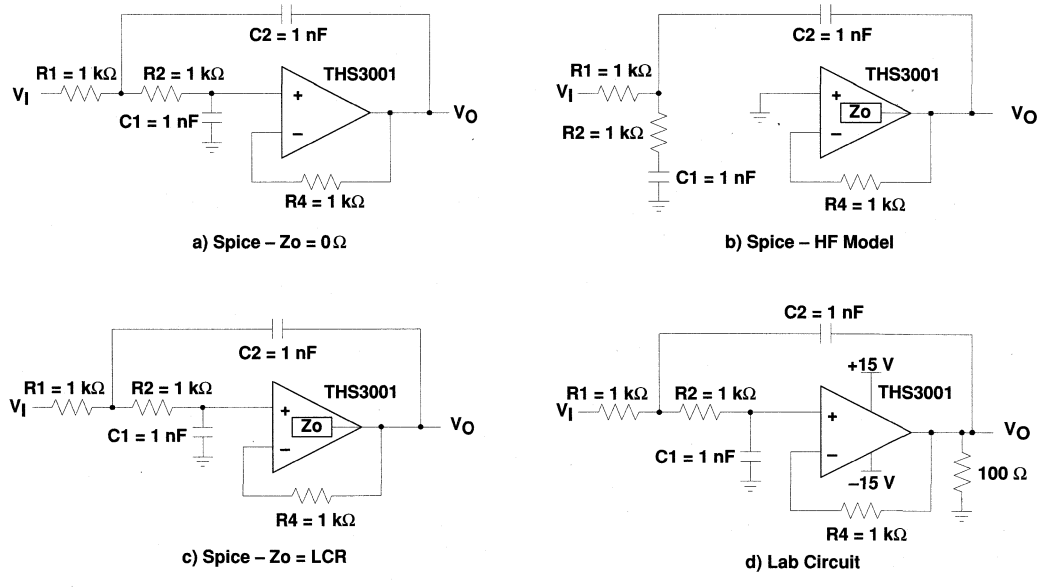


Figure 7. Test Circuits

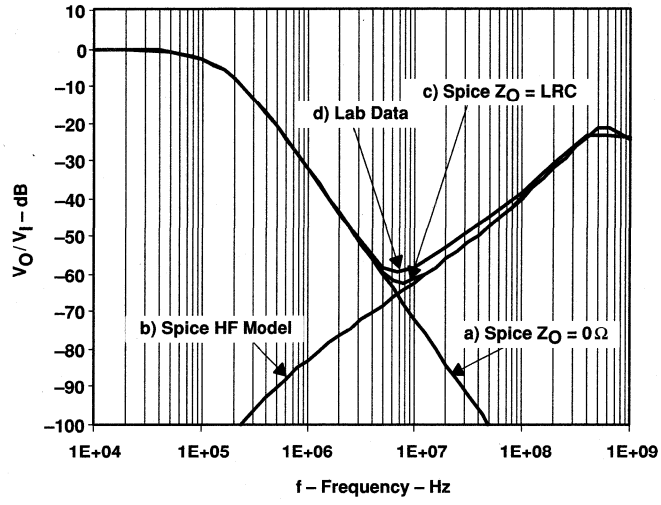


Figure 8. Effect of Output Impedance

4 High-Pass Circuit

The standard equation (in frequency domain) for a second order high-pass is:

$$H_{HP} = \frac{-K\left(\frac{f}{fc}\right)^2}{-\left(\frac{f}{fc}\right)^2 + \frac{jf}{Qfc} + 1} \tag{10}$$

When f<<fc, equation (10) reduces to $-K\left(\frac{f}{fc}\right)^2$. Below fc signals are attenuated by the square of the frequency ratio. When f=fc, equation (10) reduces to –jKQ, and signals are enhanced by the factor Q. When f>>fc, equation (10) reduces to K, and the circuit passes signals multiplied by the gain factor K. With attenuation at lower frequencies increasing by a power of 2, equation (10) describes a second order high-pass filter.

Figure 9 shows the Sallen-Key circuit configured for high-pass:

$Z2 = \frac{1}{sC2}$, $Z1 = \frac{1}{sC1}$, $Z3 = R1$, $Z4 = R2$, and $K = 1 + \frac{R4}{R3}$.

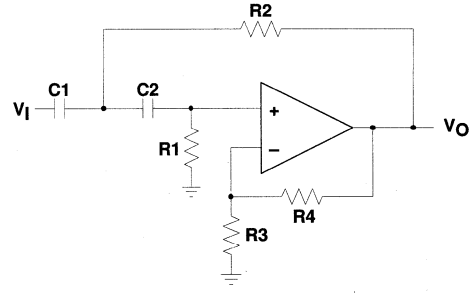


Figure 9. High-Pass Sallen-Key Circuit

From equation (7), the ideal high-pass transfer function is:

$$\frac{Vo}{Vi}(hp) = \frac{K}{\frac{1}{s^2(R1R2C1C2)} + \frac{1}{s}\left(\frac{1}{R1C1} + \frac{1}{R1C2} + \frac{(1-K)}{R2C1}\right) + 1}$$

with some manipulation this becomes

$$\frac{Vo}{Vi}(hp) = \frac{K(s^2(R1R2C1C2))}{s^2(R1R2C1C2) + s(R2C2 + R2C1 + R1C2(1 - K) + 1)} \tag{11}$$

By letting

$$s = j2\pi f,\ f_o = \frac{1}{2\pi\sqrt{R1R2C1C2}},\ \text{and}\ Q = \frac{\sqrt{R1R2C1C2}}{R2C2 + R2C1 + R1C2(1 - K)},$$

equation (11) follows the same form as equation (10). As above, simplifications make these equations much easier to deal with. The following are common simplifications used.

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Letting R1=mR, R2=R, C1=C, and C2=nC, results in:

$fc = \frac{1}{2\pi RC\sqrt{mn}}$ and $Q = \frac{\sqrt{mn}}{n + 1 + mn(1 - K)}$. This simplifies things somewhat, but there is interaction between fc and Q. To design a filter using this simplification, first set the gain and Q based on m, n, and K, and then select C and calculate R to set fc.

Notice that $K = 1 + \frac{n + 1}{mn}$ results in Q=∞. With larger values, Q becomes negative—that is the poles move into the right half of the s-plane and the circuit oscillates. The most frequently designed filters require low Q values and this should rarely be a design issue.

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Letting R1=mR, R2=R, C1=C, and C2=nC, and K=1 results in:

$fc = \frac{1}{2\pi RC\sqrt{mn}}$ and $Q = \frac{\sqrt{mn}}{n + 1}$. This keeps the gain=1 in the pass band, but again there is interaction between fc and Q. To design a filter using this simplification, first set Q by selecting the ratios m and n, and then select C and calculate R to set fc.

4.3 Simplification 3: Set Resistors as Ratios and Capacitors Equal

Letting R1=mR, R2=R, and C1=C2=C, results in:

$fc = \frac{1}{2\pi RC\sqrt{m}}$ and $Q = \frac{\sqrt{m}}{2 + m(1 - K)}$. The reason for setting the capacitors equal is the limited selection of values compared with resistors.

There is interaction between setting fc and Q. Start the design by choosing m and K to set the gain and Q of the circuit, and then choose C and calculating R to set fc.

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Letting R1=R2=R, and C1=C2=C, results in: $fc = \frac{1}{2\pi RC}$ and $Q = \frac{1}{3 - K}$. Now fc and Q are independent of one another, and design is greatly simplified. The gain of the circuit now determines Q. The choice of RC sets fc—the capacitor should chosen and the resistor calculated. One minor drawback is that since the gain controls the Q of the circuit, further gain or attenuation may be necessary to achieve the desired signal gain in the pass band.

Values of K very close to 3 result in high Qs that are sensitive to variations in the values of R3 and R4. For instance, setting K=2.9 results in a nominal Q of 10. Worst case analysis with 1% resistors results in Q=16. Whereas, setting K=2 for a Q of 1, worst case analysis with 1% resistors results in Q=1.02. Resistor values where K=3 leads to Q=∞, and with larger values, Q becomes negative. The most frequently designed filters require low Q values, and this should rarely be a design issue.

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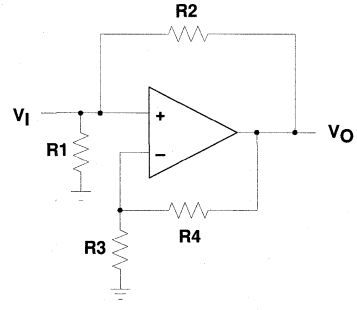
As mentioned above there are three basic modes of operation: below cut-off, above cutoff, and in the area of cut-off. Assuming the amplifier has adequate frequency response beyond cutoff, the filter works as expected. At frequencies well above cut-off, the high frequency (HS) model shown in Figure 10 is used to show the expected circuit operation. The assumption made here is that C1 and C2 are effective shorts when compared to the impedance of R1 and R2. The formula shows the transfer function of this model, where a(f) is the open loop gain of the amplifier and b is the feedback factor. The circuit operates as expected until $\frac{1}{a(f)b}$ is no longer much smaller than 1. After which the gain of the circuit falls off with the open loop gain of the amplifier. Because of practical limitations, designing a high-pass Sallen-Key filter results in a band-pass filter where the upper cutoff frequency is determined by the open loop response of the amplifier.



$$\frac{Vo}{Vi} = \frac{1}{b}\left[\frac{1}{1 + \frac{1}{a(f)b}}\right]$$

Figure 10. Model of High-Pass Sallen-Key Filter Above fc

4.6 Lab Data

A Sallen-Key high-pass filter using the Texas Instruments THS3001 shows the effects described above. The THS3001 is a high-speed current-feedback amplifier with an advertised bandwidth of 420 MHz. No particular type of filter (i.e., Butterworth, Chebychev, Eliptic, etc.) was designed. Choosing Z1=Z2=1kΩ, Z3=Z4=1nF, R3=open, and R4=1kΩ, results in a high-pass filter with fc=159 kHz, and Q=1/2. Figure 11 shows the circuit, and Figure 12 shows the lab results. As expected, the circuit attenuates signals below 159 kHz at a rate of 40dB/dec, and passes signals above 159 kHz with a gain of 1 until the amplifier's open loop gain falls to around unity between 300 MHz and 400 MHz. The slight increase in gain seen just before 300 MHz is due to gain peaking in the amplifier. Setting R4 to a higher value reduces this, but also reduces the overall bandwidth of the amplifier.

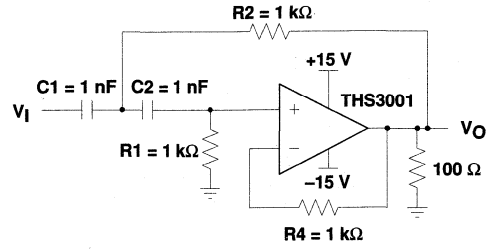


Figure 11. High-Pass Sallen-Key Filter Using THS3001

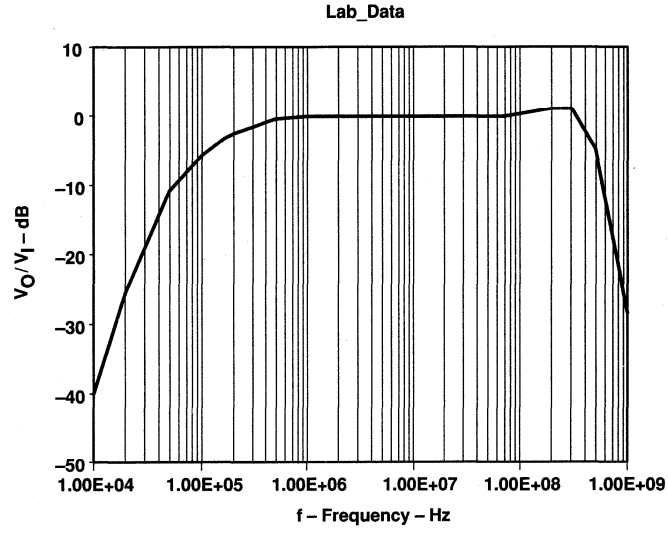


Figure 12. Frequency Response of High-Pass Sallen-Key Filter Using THS3001

5 Summary and Comments About Component Selection

Theoretically, any values of R and C that satisfy the equations may be used, but practical considerations call for component selection guidelines to be followed.

Given a specific corner frequency, the values of C and R are inversely proportional—as C is made larger, R becomes smaller and vice versa.

In the case of the low-pass Sallen-Key filter, the ratio between the output impedance of the amplifier and the value of filter component R sets the transfer functions seen at frequencies well above cut-off. The larger the value of R the lower the transmission of signals at high frequency. Making R too large has consequences in that C may become so small that the parasitic capacitors —including the input capacitance of the amplifier—cause errors.

For the high-pass filter, the amplifier's output impedance does not play a parasitic role in the transfer function, so that the choice of smaller or larger resistor values is not so obvious. Stray capacitance in the circuit, including the input capacitance of the amplifier, makes the choice of small capacitors, and thus large resistors, undesirable. Also, being a high-pass circuit, the bandwidth is potentially very large and resistor noise associated with increased values can become an issue. Then again, small resistors become a problem if the circuit impedance is too small for the amplifier to operate properly.

The best choice of component values depends on the particulars of your circuit and the tradeoffs you are willing to make. General recommendations are as follows:

- Capacitors
  - Avoid values less than 100 pF.
  - Use NPO if at all possible. X7R is OK in a pinch. Avoid Z5U and other low quality dielectrics. In critical applications, even higher quality dielectrics like polyester, polycarbonate, mylar, etc., may be required.
  - Use 1% tolerance components. 1%, 50V, NPO, SMD, ceramic caps in standard E12 series values are available from various sources.
  - Surface mount is preferred.
- Resistors
  - Values in the range of a few hundred ohms to a few thousand ohms are best.
  - Use metal film with low temperature coefficients.
  - Use 1% tolerance (or better).
  - Surface mount is preferred.

Building a Simple SPICE Model for the THS3001

James Karki

Literature Number: SLOA018
April 1999

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Contents

List of Figures

Building a Simple SPICE Model for the THS3001

James Karki

ABSTRACT

The application report *Voltage Feedback Versus Current Feedback Op Amps* SLVA051 outlines the basic operation of a current feedback operational amplifier (op amp) in relation to a voltage feedback op amp. One of the basic principles of a current feedback op amp is that its transfer function is a transimpedance equal to the output voltage divided by the current from the negative input terminal, i.e., $Zt = \frac{Vo}{Ie}$.

This application report describes how to construct a simple model that will simulate the frequency response of the THS3001 in SPICE. The laboratory setup to measure the basic parameters of the THS3001 is illustrated.

1 Introduction

This report highlights the basic functioning of the THS3001 op amp, and helps give insight to its proper use. Limitations of the device such as input common mode range, power supply range, CMRR, PSRR, output voltage swing, etc., are purposely left out . The model is simple and easy to understand, simulates fast, and gives good results.

Figure 1 is a basic current feedback op amp model. To transform this into a SPICE circuit model, *Zt*, *Zo*, and *Re* must be determined.

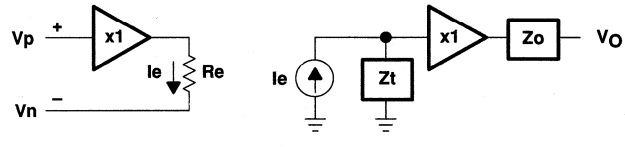
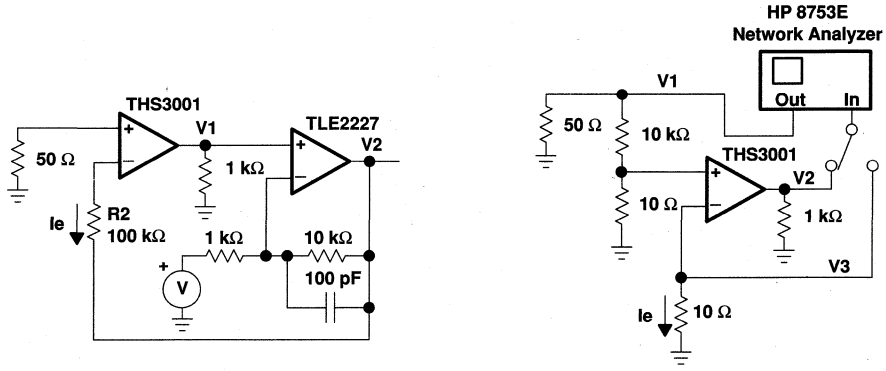


Figure 1. Basic CF Op Amp Model

2 Measuring *Zt*

A network analyzer is designed to measure the transfer function of a circuit. Therefore an HP8753E network analyzer is used to measure the transfer function of the THS3001. It has a lower frequency limit of 30 kHz. Below 30 kHz a servo-loop is used. Figure 2 shows the laboratory test setups. The servo-loop is on the left and the network analyzer is on the right.



(a) Servo-Loop, f < 30 kHz

(b) Network Analyzer, f ≥ 30 kHz

Figure 2. Test Setup

Solving the servo-loop circuit shown in Figure 2 (a), the transimpedance of the THS3001 is $Zt = -\frac{\Delta V1}{\Delta V2} \times R2$. The 100-pF capacitor limits the bandwidth to 159 kHz and the 1 kΩ provides a load.

Using the network analyzer as shown in Figure 2 (b), the transfer functions $\frac{V2}{V1}$ and $\frac{V3}{V1}$ are measured by switching the input between *V2* and *V3*. To compute $Zt = \frac{V2}{Ie}$, divide $\frac{V2}{V1}$ by $\frac{V3}{V1}$ to get $\frac{V2}{V3}$, then multiply by 10 Ω to get the transimpedance of the THS3001. By default the network analyzer displays the results in dB. Therefore, the mechanics of the transimpedance calculation are: $Zt\ (dB) = \frac{V2}{V1}(dB) - \frac{V3}{V1}(dB) + 20\ dB$.

Figure 3 is a plot of the THS3001 transimpedance magnitude and phase versus frequency from data collected using the test setups and methods described above. The simulation result of the SPICE model, constructed later, is also plotted.

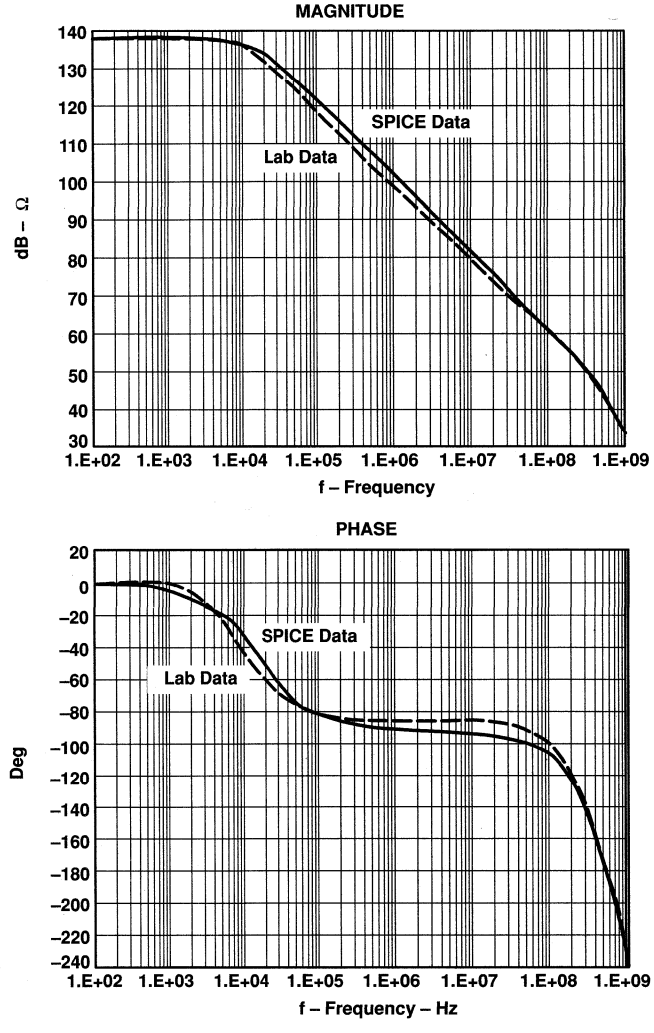


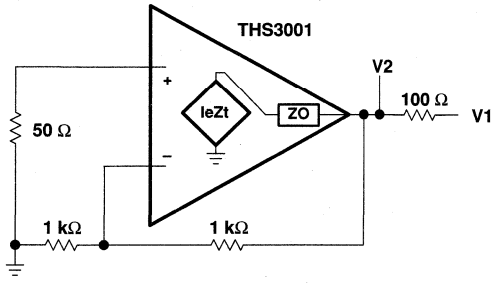
Figure 3. THS3001 Open Loop Transimpedance

Analyzing this information:

dc gain = 138.5 dB Ω = 8.5 MΩ
dominant pole near 10 kHz,
multiple upper frequency poles above 200 MHz

3 Measuring *Zo*

With the circuit shown in Figure 4, the amplifier tries to maintain 0 V at its output terminal. Because of the finite output impedance *zo*, there is a finite voltage at V2. By varying the voltage V1 and recording V2, the output impedance, Zo_{CL}, is calculated by the formula shown.



$$Zo_{CL} = 100 \times \left(\frac{1}{\frac{V1}{V2} - 1} \right)$$

Figure 4. Measuring *Zo*

In the closed loop situation shown, $Zo_{CL} \neq zo$, but it is related by the loop transmission as follows:

$$Zo_{CL} = zo \times \left(\frac{1}{1 + \frac{Zt}{1k}} \right)$$

At low frequencies Zo_{CL} is very low because Zt is very high, and decreases as frequency increases. The graph shown in Figure 5 shows the measured Zo_{CL} from 100 kHz to 1 GHz. The SPICE simulation of the output impedance model (developed below) configured the same as the test circuit in Figure 4 is also plotted.

Analyzing the graph in Figure 5: Zo_{CL} increases at approximately 20 dB/dec from 100 kHz to over 100 MHz; it peaks at 600 MHz, and falls at about 20 dB/dec to 1 GHz. Correlating Zo_{CL} to Zt, and the above equation: zo appears resistive up to about 100 MHz where $Zt = 1000$. After that zo appears reactive in nature.

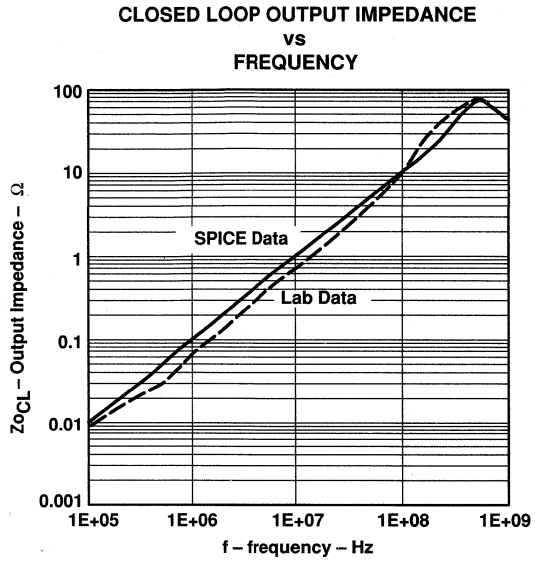
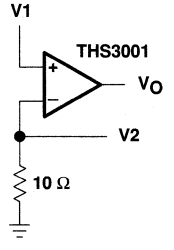


Figure 5. Zo_{CL} vs Frequency

4 Measuring *Re*

By measuring the transfer function $\frac{V2}{V1}$ in Figure 6, *Re* is approximated by the formula shown. At higher frequencies, parasitic inductance and capacitance modify the impedance, but for the most part, these effects are included in the measurement of *Zt*. So, for the purposes of this report, take *Re* = 25 Ω resistive.



$$Re = 10 \times \left(\frac{V1}{V2} - 1\right) = 25\Omega$$

Figure 6. Measuring *Re*

5 Constructing the Model

To build a SPICE model for the THS3001, use Figure 1 as a template, and use the data collected to compute component values. E and F devices are used to construct the SPICE model. An E device is a voltage-controlled voltage source and an F device is a current-controlled current source. Unity gain is used for these devices.

The input is modeled by an E device driving an F device. The current in the F device is set by *Re* between the negative input terminal and ground. The output of the F device emulates the error current *Ie*.

The output of the F device drives $Rt = 8.5\ M\Omega$ and $Cc = 1.25$ pF. The values are chosen to set the dc gain and dominant pole of *Zt*.

Trial and error reveals that an RC single pole at 1 GHz, and an LRC double pole at 800 MHz (Q = 1) shapes the upper frequency response close to the measured values. E1 – E3 provide buffering. R1 and C1 form the RC single pole, and L2, R2, and C2 form the LRC double pole.

The model shown in Figure 7 is proposed for *zo*.

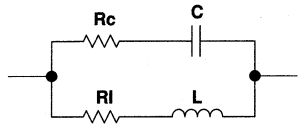


Figure 7. Model for *zo*

Select component values as follows:

1. Rl = Zo_{CL} divided by Zt/1000 at 100 kHz → Rl ≈ 7.7 Ω
2. sL = Rl at 100 MHz → L ≈ 11 nH
3. 1/sC = sL at 600 MHz → C ≈ 6.3 pF
4. $Rc = \sqrt{\dfrac{\left(Zo_{CL}Rl - \dfrac{L}{C}\right)^2 + \left(\dfrac{Rl}{sC}\right)^2}{\left(Rl - Zo_{CL}\right)^2 + (sL)^2}}$, *with* $s = 2\pi * 600\ MHz$, → $Rc \approx 18\Omega$

Figure 8 shows the SPICE model created. The simulated open loop transimpedance and closed loop output impedance are included in Figure 3 and Figure 5 to see the correlation between simulating this model and the lab data collected on the THS3001.

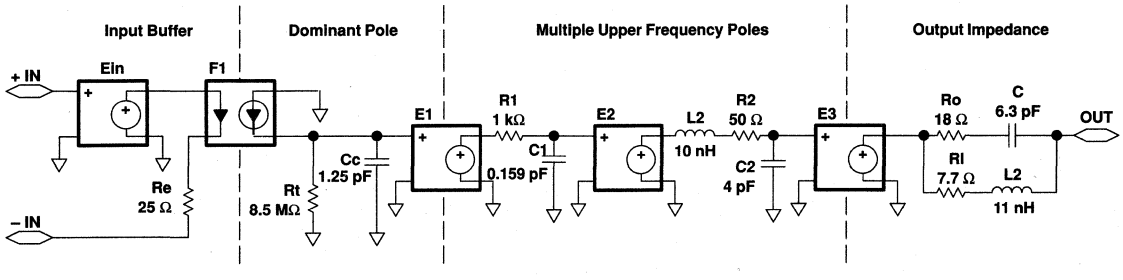


Figure 8. Simple THS3001 SPICE Model

To test the model further, SPICE simulations of circuits from the THS3001 data sheet, literature number SLOS217, is performed and compared to the data sheet graphs. The circuits and the results are shown in Figure 9 through Figure 11. Note that 1-pF capacitors are added to the output and negative input to simulate parasitic board capacitance. The data from the data sheet is prefaced by DS, followed by the circuit configuration. The data from the SPICE simulation is prefaced by SPICE, followed by the circuit configuration.

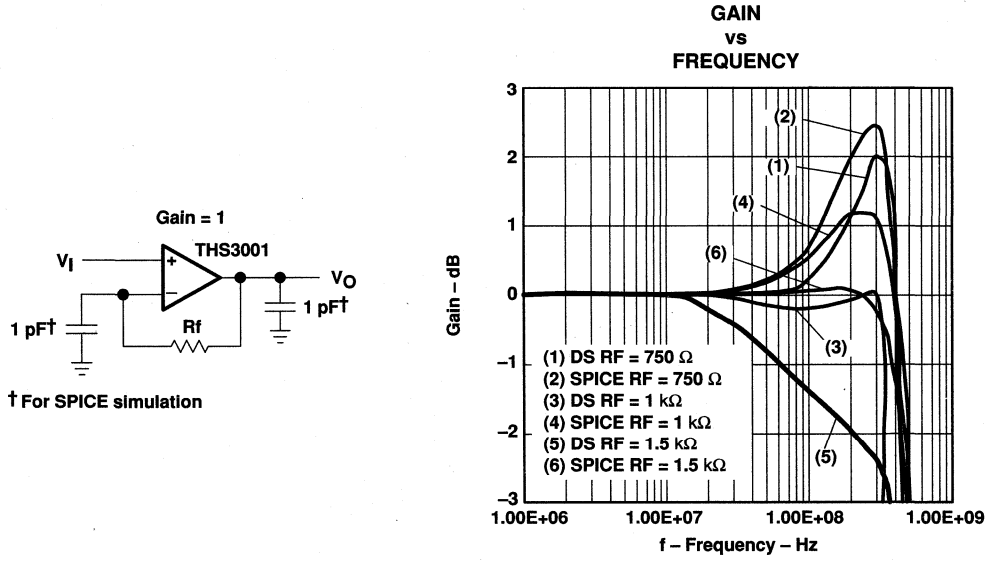


Figure 9. Comparison of Data Sheet and SPICE Model with Gain = 1

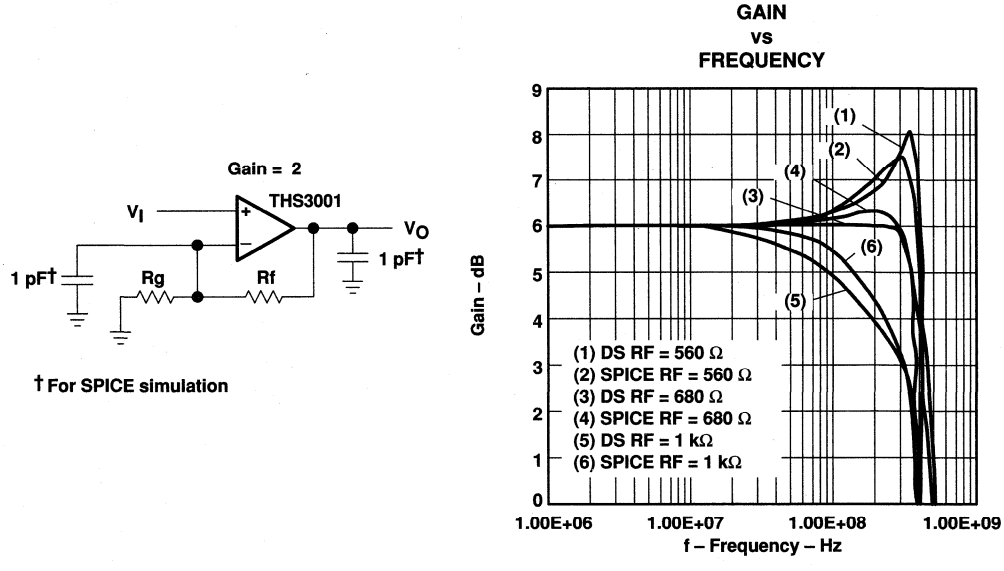


Figure 10. Comparison of Data Sheet and SPICE Model with Gain = 2

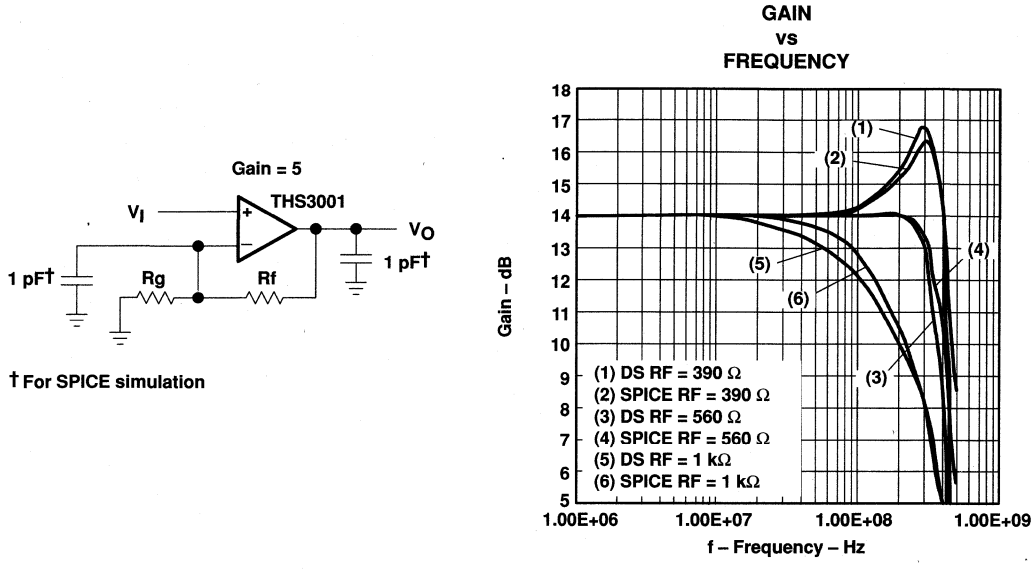


Figure 11. Comparison of Data Sheet and SPICE Model with Gain = 5

6 Summary

The simple model developed here is useful for simulating and understanding the basic operation of the THS3001. Hopefully this model will prove practical to you. Use it in good health.

Current Feedback Amplifier Analysis and Compensation

Application Report

Ronald Mancini

Literature Number: SLOA021
May 1999

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Contents

List of Figures

List of Tables

Current Feedback Amplifier Analysis and Compensation

Ron Mancini

ABSTRACT

Current feedback amplifiers have ideal closed loop gain equations identical to voltage feedback amplifiers, but the similarity ends there. The detailed gain equations for the current feedback amplifier are developed here for the inverting and noninverting circuits. This paper goes beyond the gain analysis as it develops the stability criteria and discusses compensation.

Introduction

Current feedback amplifiers (CFA) have sacrificed the dc precision of voltage feedback amplifiers (VFA) for speed. This tradeoff results in higher bandwidth that is relatively independent of closed loop gain and faster slew rate. Although CFAs do not have the precision of their VFA counterparts, they are precise enough to be dc coupled in video applications without sacrificing much dynamic range. CFAs have eliminated the ac coupling requirement that existed in previous high frequency amplifier designs; they operate in the GHz range while dc coupled. CFAs have much faster slew rates than VFAs, so they have faster rise/fall times and less intermodulation distortion. This application note assumes that the reader is familiar with feedback electronics and VFAs. Refer to Texas Instruments application note SLVA058 for basic feedback analysis tools. Texas Instruments application note SLOA020 covers VFA stability and theory.

The CFA model is shown in Figure 1. The noninverting input of a CFA connects to the input of a buffer (input buffer), so it has a very high impedance similar to a bipolar transistor VFA input. The inverting input connects to the input buffer's output, so the inverting input impedance is very low. Z_B models the input buffer's output impedance, and it is usually less than 50 ohms. The buffer gain, G_B, is as close to one as IC design methods can achieve, so it is neglected in the calculations.

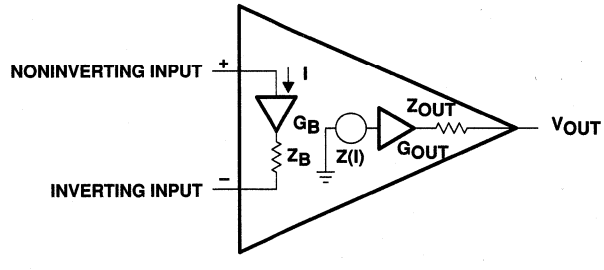

Figure 1. Current Feedback Amplifier Model

The output buffer provides a low output impedance for the amplifier. Again, the output buffer gain, G_{OUT}, is very close to one, so it is neglected in this analysis. The output impedance of the output buffer can be ignored except when driving very low impedance or capacitive loads. The input buffer's output impedance can not be ignored because it affects stability at high frequencies.

The current-controlled current source, Z, is a transimpedance. The transimpedance in a CFA serves the same function as the gain in a VFA. Usually the transimpedance is very high, in the megohm range, so the CFA obtains accuracy by closing a feedback loop in a manner similar to the VFA.

Development of the Stability Equation

The stability equation is developed with the aid of Figure 2. Remember, stability is independent of the input, and stability depends solely on the loop gain (Aβ). The stability equation is developed by breaking the loop at point X, inserting a test signal (V_{TI}), and calculating the return signal (V_{TO}). The circuit shown in Figure 3 has the model substituted for the CFA symbol. The input buffer gain, the output buffer gain, and output buffer output impedance have been left out of the circuit to simplify calculations. This approximation is valid for almost all applications.

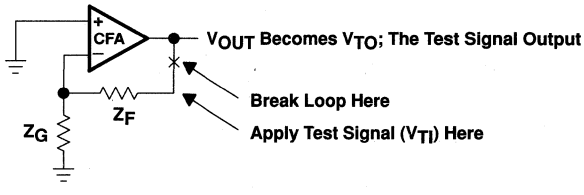

Figure 2. Stability Analysis Circuit

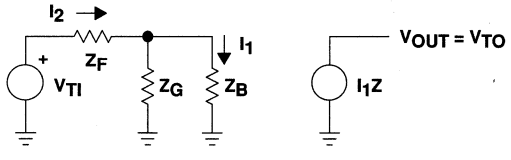

Figure 3. Stability Analysis Schematic

The transfer equation is given in equation 1, and Kirchoff's law is used to write equations 2 and 3.

$$V_{TO} = I_1 Z \tag{1}$$

$$V_{TI} = I_2(Z_F + Z_G \parallel Z_B) \tag{2}$$

$$I_2(Z_G \parallel Z_B) = I_1 Z_B \tag{3}$$

Equations 2 and 3 are combined to yield equation 4.

$$V_{TI} = I_1(Z_F + Z_G \parallel Z_B)\left(1 + \frac{Z_B}{Z_G}\right) = I_1 Z_F\left(1 + \frac{Z_B}{Z_F \parallel Z_G}\right) \tag{4}$$

Dividing equation 1 by equation 4 yields equation 5, which is the open loop transfer equation. This equation is commonly known as the loop gain.

$$A\beta = \frac{V_{TO}}{V_{TI}} = \frac{Z}{\left(Z_F\left(1 + \frac{Z_B}{Z_F \| Z_G}\right)\right)} \tag{5}$$

The Noninverting CFA

The closed loop gain equation for the noninverting CFA is developed with the aid of Figure 4 where external gain setting resistors have been added. The buffers are shown in Figure 4, but because their gains equal one, they do not enter into the calculations.

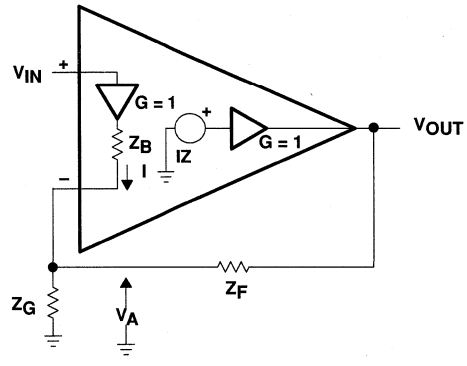

Figure 4. Noninverting CFA

Equation 6 is the transfer equation, equation 7 is the current equation at the inverting node, and equation 8 is the input loop equation. These equations are combined to yield equation 9, the closed loop gain equation.

$$V_{OUT} = IZ \tag{6}$$

$$I = \left(\frac{V_A}{Z_G}\right) - \left(\frac{V_{OUT} - V_A}{Z_F}\right) \tag{7}$$

$$V_A = V_{IN} - IZ_B \tag{8}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{Z\left(1 + \frac{Z_F}{Z_G}\right)}{Z_F\left(1 + \frac{Z_B}{Z_F \| Z_G}\right)}}{1 + \frac{Z}{Z_F\left(1 + \frac{Z_B}{A_F \| Z_G}\right)}} \tag{9}$$

When the input buffer output impedance (Z_B) approaches zero, equation 9 reduces to equation 10.

$$\frac{V_{OUT}}{V_{IN}} = \frac{\frac{Z\left(1+\frac{Z_F}{Z_G}\right)}{Z_F}}{1+\frac{Z}{Z_F}} = \frac{1+\frac{Z_F}{Z_G}}{1+\frac{Z_F}{Z}} \quad (10)$$

When the transimpedance (Z), is very high the term Z_F/Z in equation 10 approaches zero, and equation 10 reduces to equation 11 which is the ideal closed loop gain equation for the CFA. The ideal closed loop gain equations for the noninverting CFA and VFA op amps are identical, and the degree to which they depart from ideal is dependent on the validity of the assumptions. The VFA has one assumption: the direct gain is very high; while the CFA has two assumptions: the transimpedance is very high and the input buffer output impedance is very low. As would be expected, two assumptions are harder to meet than one; thus the CFA departs from the ideal more than the VFA does.

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{Z_F}{Z_G} \quad (11)$$

The Inverting CFA

The inverting CFA configuration is seldom used because the input impedance is very low ($Z_B||Z_F + Z_G$). When Z_G is selected as a high resistance to swamp out the effects of Z_B, Z_F must also be high to achieve at least unity gain. High values for Z_F result in poor bandwidth performance as seen in the next section. If Z_G is selected as a low value, Z_B, which is frequency sensitive, causes the gain to increase as frequency increases. These limitations restrict the applications of the inverting CFA.

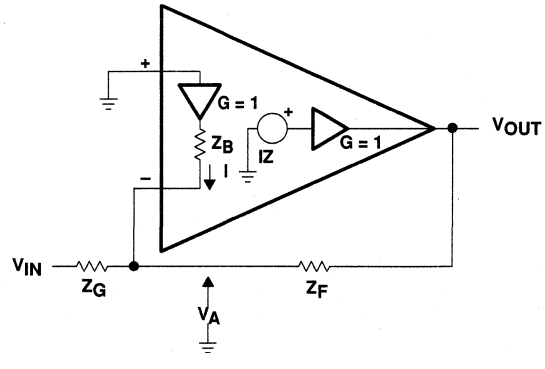

Figure 5. Inverting CFA

The current equation for the input node is written as equation 12. Equation 13 defines the dummy variable (V_A) and equation 14 is the transfer equation for the CFA. These equations are combined and simplified leading to equation 15, which is the closed loop gain equation for the inverting CFA.

$$I + \frac{V_{IN}-V_A}{Z_G} = \frac{V_A-V_{OUT}}{Z_F} \quad (12)$$

$$IZ_B = -V_A \tag{13}$$

$$IZ = V_{OUT} \tag{14}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{Z_G\left(1 + \frac{Z_B}{Z_F \| Z_G}\right)}{1 + \frac{Z}{Z_F\left(1 + \frac{Z_B}{Z_F \| Z_G}\right)}} \tag{15}$$

When Z_B approaches zero, equation 15 reduces to equation 16.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{\frac{1}{Z_G}}{\frac{1}{Z} + \frac{1}{Z_F}} \tag{16}$$

When Z is very large equation 16 becomes equation 17, which is the ideal closed loop gain equation for the inverting CFA.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{Z_F}{Z_G} \tag{17}$$

The ideal closed loop gain equations for the inverting VFA and CFA op amps are identical. Both configurations have lower input impedance than the noninverting configuration has, but the VFA has one assumption while the CFA has two assumptions. Again, as was the case with the noninverting counterparts, the CFA is less ideal than the VFA because of the two assumptions. The zero Z_B assumption always breaks down in bipolar-junction transistors, as is shown later. The differential amplifier configuration is almost never used with CFAs because of the gross input impedance mismatch.

Stability Analysis

The stability equation is repeated as equation 18.

$$A\beta = \frac{V_{TO}}{V_{TI}} = \frac{Z}{\left(Z_F\left(1 + \frac{Z_B}{Z_F \| Z_G}\right)\right)} \tag{18}$$

Comparing equations 9 and 15 to equation 18 shows that the inverting and noninverting CFA op amps have identical stability equations. This confirms the earlier statement that the op amp input has no bearing on stability. The two op amp parameters affecting stability are the transimpedance (Z) and the input buffer's output impedance (Z_B). The external components affecting stability are Z_G and Z_F. The external impedances are controlled by the designer, although stray capacitance, which is a part of the external impedance, sometimes appears uncontrollable. Z and Z_B are CFA op amp parameters, and they cannot be controlled by the circuit designer, so the designer must deal with them. We take the log of equation 18 prior to plotting the logs (equations 19 and 20) in Figure 6.

$$20\text{LOG}|A\beta| = 20\text{LOG}|Z| - 20\text{LOG}\left|Z_F\left(1 + \frac{Z_B}{Z_F \parallel Z_B}\right)\right| \quad (19)$$

$$\phi = \text{TANGET}^{-1}(A\beta) \quad (20)$$

The log plot, called a Bode plot, is named after H. W. Bode, who first developed it in the forties. It enables the designer to add and subtract components of the stability equation graphically.

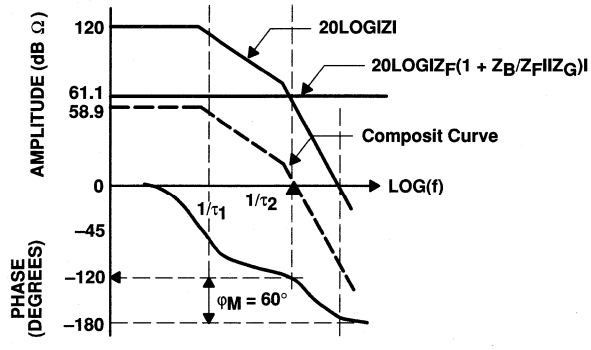

Figure 6. Bode Plot of Stability Equation

The plot in Figure 6 assumes typical values for the parameters:

$$Z = \frac{1M\Omega}{(1 + \tau_1 S)(1 + \tau_2 S)} \quad (21)$$

$$Z_B = 70\Omega \quad (22)$$

$$Z_G = Z_F = 1k\Omega \quad (23)$$

The transimpedance has two poles, and the plot shows that the op amp will be unstable without the addition of external components because 20LOG|Z| crosses the 0 dB axis after the phase shift equals 180°. The external components reduce the loop gain 61.1 dB, so the circuit is stable because it has 60° phase margin. Notice that the parallel combination of Z_F and Z_G contribute little to the phase margin because Z_B is so small.

When $Z_B = 0\ \Omega$ and $Z_F = R_F$ the loop gain equation is; $A\beta = Z/R_F$. Under these conditions, stability is determined by Z and R_F, and a value of R_F can always be found to stabilize the circuit. The transimpedance and feedback resistor have a major impact on stability, and the input buffer's output impedance has a minor effect on stability. Since Z_B increases with an increase in frequency, it tends to increase stability at higher frequencies. Equation 18 is rewritten as equation 24, but is has been manipulated so that the ideal closed loop gain is readily apparent.

$$A\beta = \frac{Z}{Z_F + Z_B\left(1 + \frac{R_F}{R_G}\right)} \quad (24)$$

The closed loop ideal gain equation (inverting and noninverting) shows up in the denominator of equation 24, thus the closed loop gain influences the stability of the op amp. When Z_B approaches zero the closed loop gain term also approaches zero, and the op amp becomes independent of the ideal closed loop gain. Under these conditions, R_F determines stability, and the bandwidth is independent of the closed loop gain. Many people claim that the CFA bandwidth is independent of the closed loop gain, and that claim's validity is dependent on the ratio of Z_B/Z_F being very low.

Z_B is important enough to warrant further investigation, so the equation for Z_B is given in equation 25.

$$Z_B \cong h_{ib} + \frac{R_B}{\beta_0 + 1}\left[\frac{1 + \frac{S\beta_0}{\varpi_T}}{1 + \frac{S\beta_0}{(\beta_0+1)\varpi_T}}\right] \tag{25}$$

At low frequencies $h_{ib} = 50\ \Omega$ and $R_B/(\beta_0+1) = 25\ \Omega$, so $Z_B = 75\ \Omega$. Z_B varies in accordance with equation 25 at high frequencies. The transistor parameters in equation 25 vary with transistor type, and these parameters are different for NPN and PNP transistors, thus Z_B is also dependent on the output polarity. Z_B is a small factor in the equation, but it adds a lot of variability to the current feedback op amp.

Stability and Input Capacitance

When stray capacitance forms on the inverting input node to ground, it causes the impedance Z_G to become reactive. The stability equation for this situation is given below.

$$Z_G = \frac{R_G}{1 + R_G C_G S} \tag{26}$$

$$A\beta = \frac{Z}{Z_B + \frac{Z_F}{A_G^2 + Z_B Z_G}} \tag{27}$$

$$A\beta = \frac{Z}{R_F}\left(1 + \frac{R_B}{R_F \parallel R_G}\right)\left(1 + R_B \parallel R_F \parallel R_G C_G S\right) \tag{28}$$

Equation 28 is the stability equation when Z_F is resistive, and there is stray capacitance between the inverting input node and ground. The stray capacitance, C_G, remains a fixed value because it is dependent on the circuit layout. The pole created by the stray capacitance is dependent on R_B because it dominates R_F and R_G. In addition, R_B fluctuates with manufacturing tolerances. As the $R_B C_G$ combination becomes larger, the pole moves towards the zero frequency axis. Eventually it interacts with the pole contained in Z, $1/\tau_2$, and instability results.

Stability and Feedback Capacitance

When a stray capacitor is formed across the feedback resistor, it adds a pole and zero to the stability equation as written in equations 29 and 30.

$$Z_F = \frac{R_F}{1 + R_F C_F S} \tag{29}$$

$$A\beta = \frac{Z(1 + R_F C_F S)}{R_F\left(1 + \frac{R_B}{R_F \| R_G}\right)(1 + R_B \| R_F \| R_G C_F S)} \tag{30}$$

This loop gain transfer function contains a pole and zero, thus, depending on the pole/zero placement, oscillation can result. The Bode plot for this case is shown in Figure 7. The original and composite curves cross the 0 dB axis with a slope of −40 dB/decade, so either curve can indicate instability. The composite curve crosses the 0 dB axis at a higher frequency than the original curve; hence, the stray capacitance has added more phase shift to the system. The composite curve is surely less stable than the original curve. Adding capacitance to the inverting input node or across the feedback resistor usually results in instability.

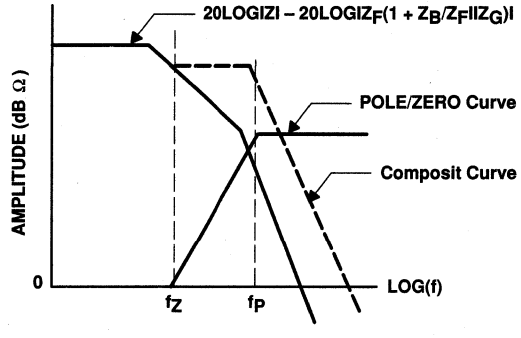

Figure 7. Bode Plot of CFA with Feedback Capacitor

Compensation of C_F and C_G

When C_F and C_G both are present in the circuit, they may be adjusted to cancel each other out. The stability equation is equation 31.

$$A\beta = \frac{Z(1 + R_F C_F S)}{R_F\left(1 + \frac{R_B}{R_F \| R_G}\right)\left(R_B \| R_F \| R_G (C_F + C_G) S + 1\right)} \tag{31}$$

If the zero and pole in equation 31 cancel each other, the only poles remaining are in Z. Setting the pole and zero in equation 31 equal yields equation 32 after some algebraic manipulation.

$$R_F C_F = C_G (R_G \| R_B) \tag{32}$$

R_B dominates the parallel combination of R_B and R_G, so equation 32 is reduced to equation 33.

$$R_F C_F = R_B C_G \tag{33}$$

R_B is an IC parameter, so it is dependent on the IC process. R_B it is an important IC parameter, but it is not important enough to be monitored as a control variable during the manufacturing process. R_B has widely spread, unspecified parameters, thus depending on R_B for compensation is risky.

Selection of the Feedback Resistor

The feedback resistor determines stability and it has an effect on closed loop bandwidth, so it must be selected very carefully. Most CFA IC manufacturers employ applications and product engineers who spend a great deal of time and effort selecting R_F. They measure each closed loop gain with several different feedback resistor values to gather data. Then they pick a compromise value of R_F that yields stable operation with low peaking, and that value of R_F is recommended on the data sheet for that specific gain. Generally this is done for several different gains in anticipation of the various gains their customer applications require (often G=1, 2, or 5).

When the circuit designer strays from the R_F value recommended on the data sheet, he gets into stability or low bandwidth problems. Lowering R_F decreases stability, and increasing R_F decreases bandwidth. What happens when the designer needs to operate at a gain not specified on the data sheet? The designer must select a new value of R_F for the new gain. Assume that $(A\beta)_1$ for a gain of one equals $(A\beta)_N$ for a gain of N, and that there is a linear relationship between stability and gain.

$$\frac{Z}{Z_{F1} + Z_B\left(1 + \frac{Z_{F1}}{Z_{G1}}\right)} = \frac{Z}{Z_{FN} + Z_B\left(1 + \frac{Z_{FN}}{Z_{GN}}\right)} \tag{34}$$

$$Z_{FN} = Z_{F1} + Z_B\left(\left(1 + \frac{Z_{F1}}{Z_{G1}}\right) - \left(1 + \frac{Z_{FN}}{Z_{GN}}\right)\right) \tag{35}$$

Equation 35 leads one to believe that a new value for Z_F can easily be chosen for each new gain. This is not the case in the real world; the assumptions don't hold up good enough to rely on them. When you change to a new gain not specified on the data sheet, equation 35 supplies a starting point for R_F, but you must test to determine the final value of R_F.

CFAs Versus VFAs

The equations for the CFA and the VFA are given in Table 1. The closed loop gain for both op amps is identical, but the remaining equations are different. This situation leads to the natural conclusion that ideal closed loop performance is identical as long as the approximations remain true. The approximations are true for frequencies much lower than the advertised −3 dB frequency, but they fall apart at the −3 dB frequency. Both types of op amps have particular niche markets.

VFAs dominate the precision and low voltage/low power markets. VFAs dominate the precision market because their differential amplifier input structure enables them to employ matching to eliminate offset voltages and currents. VFAs dominant the low voltage/power market because their circuit configuration enables them to operate in a rail-to-rail mode. VFAs have poor slew rate, and this limits their pulse handling capability.

CFAs have much higher bandwidth because the have much lower impedances in the inverting input circuit and the feedback circuit. The bandwidth stays high longer in CFAs; thus, a 50 MHz CFA is usable at much higher frequencies than a 50 MHz VFA. The CFA circuit topology enables them to supply slew current from the output structure; thus, they have much faster slew rates. The CFAs stability is determined by the value of the feedback resistor.

Table 1. Tabulation of Pertinent VFA and CFA Equations

CIRCUIT CONFIGURATION	CURRENT FEEDBACK AMPLIFIER	VOLTAGE FEEDBACK AMPLIFIER
NONINVERTING		
Direct gain	$\frac{Z(1 + Z_F/Z_G)}{Z_F(1 + Z_B/Z_F \parallel Z_G)}$	a
Loop gain	$Z/Z_F(1 + Z_B/Z_F \parallel Z_G)$	$aZ_F/(Z_G + Z_F)$
Closed loop gain	$1 + Z_F/Z_G$	$1 + Z_F/Z_G$
INVERTING		
Direct gain	$\frac{Z}{Z_G(1 + Z_B/Z_F \parallel Z_G)}$	$aZ_F/(Z_F + Z_G)$
Loop gain	$Z/Z_F(1 + Z_B/Z_F \parallel Z_G)$	$aZ_G/(Z_G + Z_F)$
Closed loop gain	Z_F/Z_G	Z_F/Z_G

Summary

The CFA is not limited by constant gain-bandwidth criteria, so the feedback resistor is adjusted for maximum performance. The stability is dependent on the feedback resistor; as R_F is decreased stability is decreased, and when R_F goes to zero, the circuit becomes unstable. As R_F is increased stability increases, but the bandwidth decreases.

The inverting input impedance is very high, but the noninverting input impedance is very low. This situation precludes CFAs from operation in the differential amplifier configuration. Stray capacitance on the inverting input node or across the feedback resistor always leads to peaking, usually to ringing, and sometimes to oscillations. A prudent circuit designer scans the PC board layout for stray capacitances and eliminates them. Breadboarding and lab testing are necessary with CFAs. The CFA performance can be improved immeasurably with a good layout, good decoupling capacitors, and low inductance components.

Driving Capacitance With the THS3001 Application Brief

Literature Number: SLOA014
April 1999

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Contents

List of Figures

Driving Capacitance With the THS3001

James Karki

ABSTRACT

Operational amplifiers (op amps) are often used to drive devices that present significant capacitance such as analog-to-digital converters, cables, MOSFETs, filter networks, etc. The effect of the added capacitance is to cause extra phase shift, which tends to erode the phase margin of the amplifier and may lead to instability. At high frequency, even a very small capacitance is detrimental.

This paper outlines an effective method for stabilizing the THS3001 while driving capacitive loads.

1 Introduction

A typical technique used to compensate for capacitance on the output is to isolate it with a resistor and provide phase lead compensation using a capacitor in the feedback path. This works well for voltage feedback op amps, even though it also tends to reduce bandwidth.

In the case of the THS3001, there are problems with adding capacitance in the feedback path. The THS3001 is a current feedback op amp and so has a minimum feedback impedance requirement. Adding a capacitor in the feedback path lowers the impedance at high frequency and leads to more instability: the opposite effect from what is desired.

Therefore, isolating the capacitance from the output of the THS3001 by inserting a resistor is the most practical means of maintaining stability. This report outlines the test set up and resistor values required to stabilize the THS3001 while driving capacitance.

2 Test

Figure 1 shows the test circuits that determine the minimum value of isolation resistance required for stable operation.

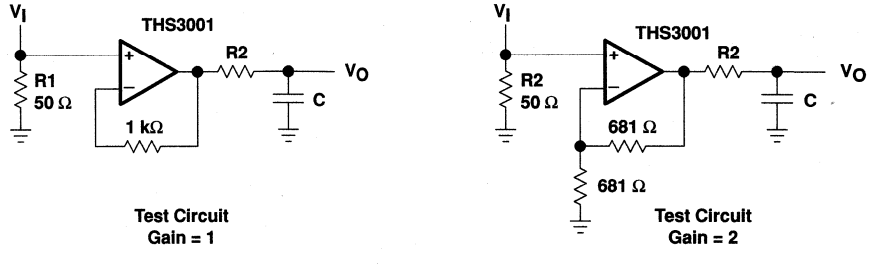

Figure 1. Test Circuits

The input signal is a square pulse with rise time and fall time of 5 ns and the amplitude adjusted for ±2 V on the output of the op amp. Gains of 1 and 2 show no significant difference. The power supply voltage is varied between ±5 V and ±15 V. The signal source is a LeCroy model 9210 pulse generator with a 9211 variable edge output module. The output signal is probed using a Tektronix P6217 4 GHz probe with input load of 0.4 pF and 100 kΩ. The signal is then displayed on a Tektronix TDS 794D oscilloscope.

The test circuit is built using the THS3001 EVM, #SLOP 130. The load capacitor is soldered across the terminal pins of output connector J2 on the solder side of the EVM. The circuit power is applied, the input signal is applied, and resistor (R2) adjusted until a square pulse with less than 1% overshoot and undershoot is obtained.

3 Data

Graph A in Figure 2 is a plot of resistor (R2) vs capacitance (C) and graph B is a plot of the rise time vs capacitance (C) (with R2). Graph A is plotted with log-log scales to show the log relationship of resistor (R2) to capacitor (C).

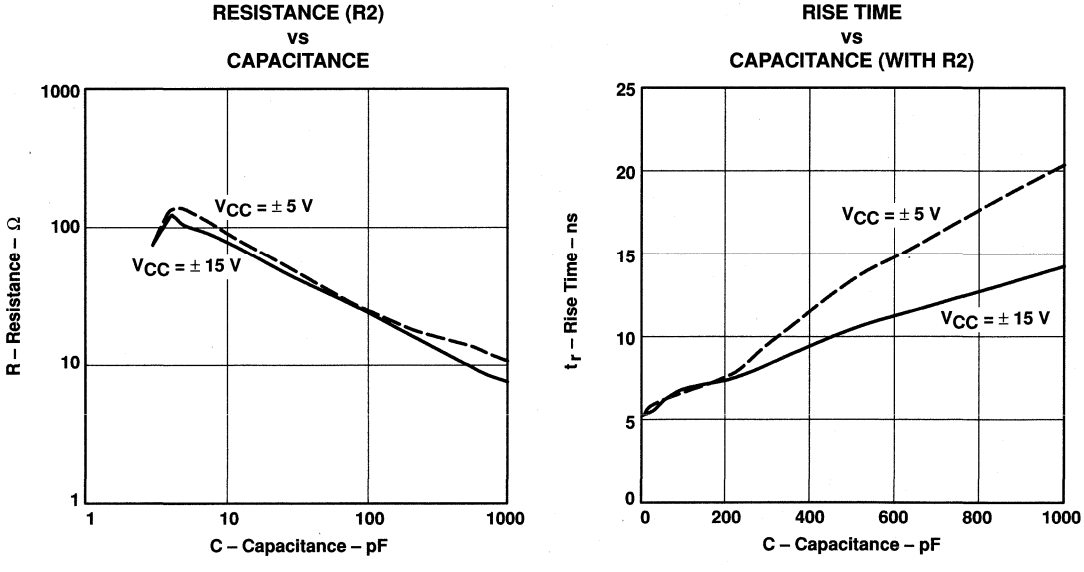

Figure 2. R2 and Rise Time vs Capacitance

With V_{CC} = ±5 V, slightly higher resistor values are required than with V_{CC} = ±15 V, and the rise time was significantly longer with C > 220 pF. A formula for estimating the required resistor value is found to be: $R = \frac{1}{\sqrt{C}} \times 300$, where C is in pF.

4 Summary

When driving load capacitance, insert a resistor in series with the output to isolate the load capacitance from the feedback path and maintain amplifier stability. A reasonable starting value for the isolation resistor is estimated by $R = \frac{1}{\sqrt{C}} \times 300$, where C is the load capacitance in pF. Final verification is achieved by constructing and testing the circuit.

Driving Capacitance With the THS4001 Application Brief

Literature Number: SLOA015
April 1999

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Contents

List of Figures

Driving Capacitance With the THS4001

James Karki

ABSTRACT

Operational amplifiers (op amps) are often used to drive devices that have significant input capacitance such as analog-to-digital converters, cables, MOSFETs, filter networks, etc. The effect of the capacitance is extra phase shift in the loop gain of the amplifier. This phase shift erodes the phase margin of the amplifier and may lead to instability. At high frequency, even a very small capacitance is detrimental.

This paper reports a simple method for restoring amplifier stability while driving capacitive loads with the THS4001.

1 Introduction

A typical technique used to compensate for output capacitance is to isolate it with a resistor. The question is, how much resistance to use.

This report outlines the test setup and resistor values required to stabilize the THS4001 while driving various load capacitors. Refer to application report *Effect of Parasitic Capacitance in Op Amp Circuits*, literature number SLOA013, for an in-depth presentation of the effects of output capacitance on circuit operation and compensation methods.

2 Test

Figure 1 shows the test circuits that determine the minimum value of isolation resistance required for stable operation.

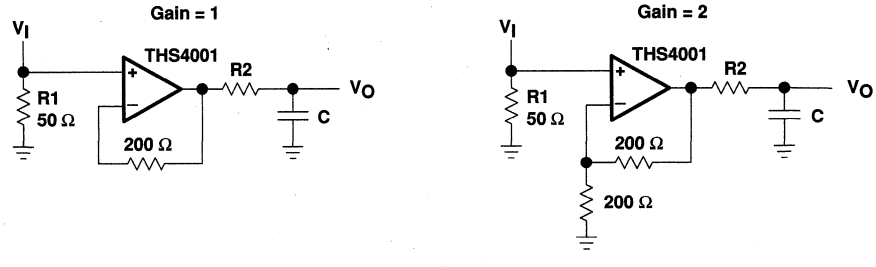

Figure 1. Test Circuits

The input signal is a square pulse with rise time and fall time of 10 ns, and the amplitude adjusted for ±2 V on the output of the op amp. The amplifier's power supply voltage is varied between ±5 V and ±15 V. The signal source is a LeCroy model 9210 pulse generator with the 9211 variable edge output module. The output signal is probed using a Tektronix P6217 4 GHz probe with input load of 0.4 pF and 100 kΩ. The signal is then displayed on a Tektronix TDS 794D oscilloscope.

The test circuit is built using the THS4001 EVM, #SLOP119. The load capacitor is soldered across the terminal pins of output connector, J2, on the solder side of the EVM. The circuit power is applied, the input signal is applied, and resistor (R2) adjusted until a square pulse with less than 2% overshoot and undershoot is obtained.

3 Data

Figure 2 shows the graphs of the required resistor values and the rise/fall time variations with the resistor and output capacitance for gain = 1 and gain = 2. Graph A is a plot of resistor (R2) vs capacitance (C), and graph B is a plot of the rise/fall time vs capacitance (C) (with R2). Graph A is plotted with log-log scales to show the log relationship of resistor (R2) to capacitor (C). Rise/fall time is the average of the rise time and the fall time.

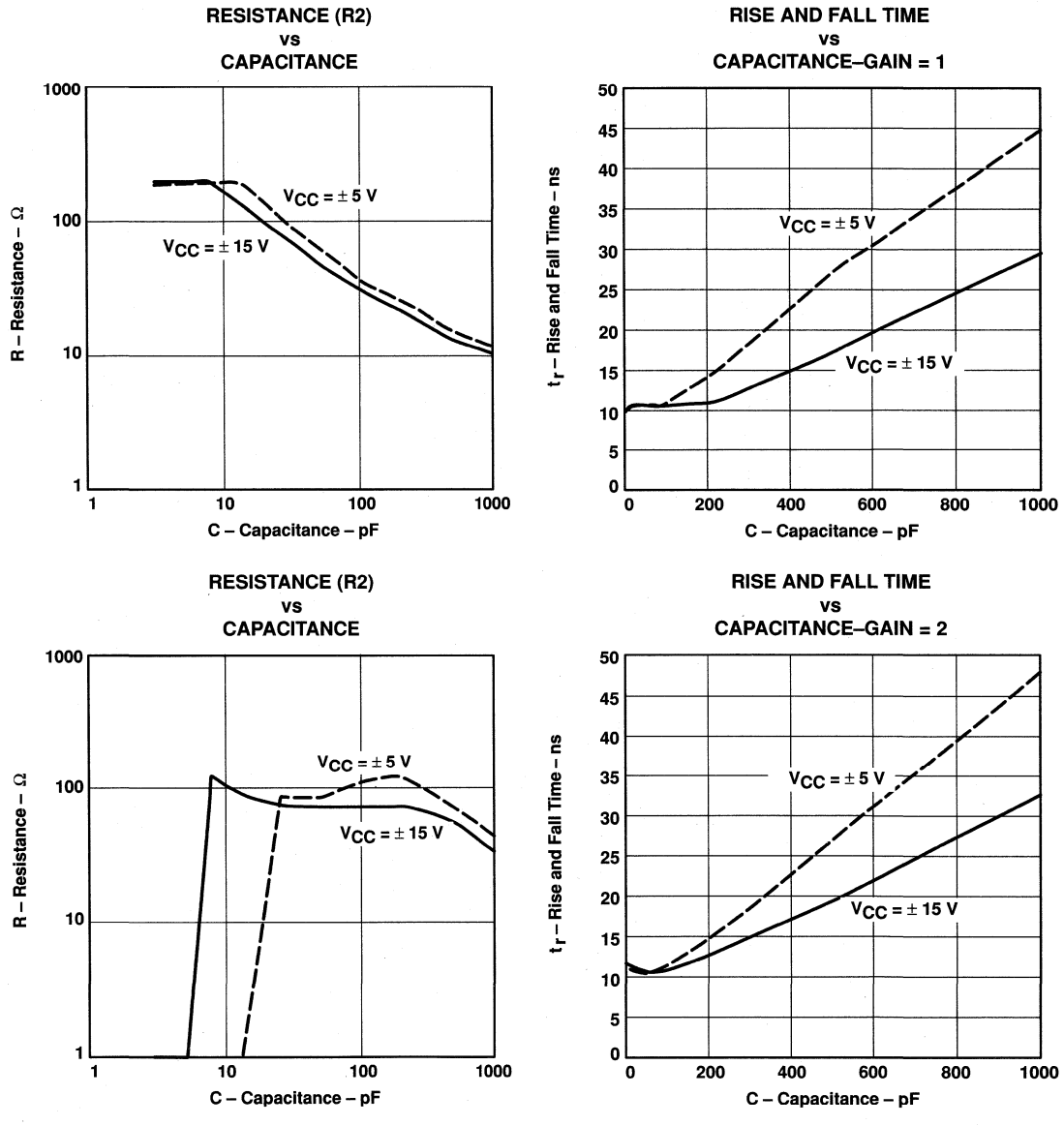

Figure 2. R2 and Rise Time vs Capacitance

4 Summary

In general with V_{CC} = ±5 V, slightly higher resistor values are required and the rise/fall time is longer.

Evaluating the data for the unity gain circuit and solving for a straight-line approximation, a formula for estimating the required resistor value for load capacitance above about 10 pF is found to be: $R = \frac{1}{\sqrt{C}} \times 450$, where C is the in pF.

With gain = 2, the required resistor value is approximately 20 Ω to 30 Ω across the range of load capacitance tested, except at the extremes.

Optimum performance is obtained from the THS4001 with V_{CC} = ±15 V. The output is much more distorted while driving capacitance greater than 200 pF with V_{CC} = ±5 V than with V_{CC} = ±15 V.

The data presented here is to help in estimating component values. The exact value of circuit components needs to be verified by the user during testing.

Effect of Parasitic Capacitance in Op Amp Circuits

Application Report

James Karki

Literature Number: SLOA013
February 1999

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Contents

List of Figures

List of Tables

Effect of Parasitic Capacitance in Op Amp Circuits

James Karki

ABSTRACT

Parasitic capacitors are formed during normal op amp circuit construction. Op amp design guidelines usually specify connecting a small 20-pF to 100-pF capacitor between the output and negative input, and isolating capacitive loads with a small, 20-Ω to 100-Ω resistor. This application report analyzes the effects of capacitance at the input and output pins of an op amp, and suggests means for computing appropriate values for specific applications. The inverting and noninverting amplifier configurations are used for demonstration purposes. Other circuit topologies can be analyzed in a similar manner.

1 Introduction

Two conductors, insulated from one another, carrying a charge, and having a voltage potential between them, form a capacitor. Capacitors are characterized by their charge-to-voltage ratio; $C = \frac{q}{V}$, where C is the capacitance in Farads, q is the charge in Coulombs, and V is the voltage in volts. In general, capacitance is a function of conductor area, distance between the conductors, and physical properties of the insulator. In the special case of two parallel plates separated by an insulator $C = \frac{\epsilon\epsilon_0 \times A}{d}$ where ϵ is the dielectric constant of the insulator, ϵ_0 is the permittivity of free space, A is the area of the plates, and d is the distance between the plates. Thus, in general:

- Capacitance is directly proportional to the dielectric constant of the insulating material and area of the conductors.
- Capacitance is inversely proportional to the distance separating the conductors.

Rarely are two parallel plates used to make a capacitor, but in the normal construction of electrical circuits, an unimaginable number of capacitors are formed. On circuit boards, capacitance is formed by parallel trace runs, or traces over a ground or power plane. In cables there is capacitance between wires, and from the wires to the shield.

- Circuit traces on a PCB with a ground and power plane will be about 1–3 pF/in.
- Low capacitance cables are about 20–30 pF/ft conductor to shield.

Therefore, with a few inches of circuit board trace and the terminal capacitance of the op amp, it is conceivable that there can be 15–20 pF on each op amp terminal. Also, cables as short as a few feet can present a significant capacitance to the op amp.

This report assumes that a voltage feedback op amp is being used.

2 Basic One-Pole Op Amp Model

The voltage feedback op amp is often designed using dominant pole compensation. This gives the op amp a one-pole transfer function over the normal frequencies of operation that can be approximated by the model shown in Figure 1 (a). This model is used throughout this report in the spice simulations with the following values: $gm = 0.1$, $Rc = 1\,M\Omega$ and $Cc = 159\,nF$. With these values, the model has the following characteristics: dc gain = 100 dB, dominant pole frequency = 10 Hz, and unity gain bandwidth = 1 MHz.

In the schematic drawings, the representation shown in Figure 1 (b) is used, where $a = gm \times \dfrac{R_c}{1 + sRcCc}$.

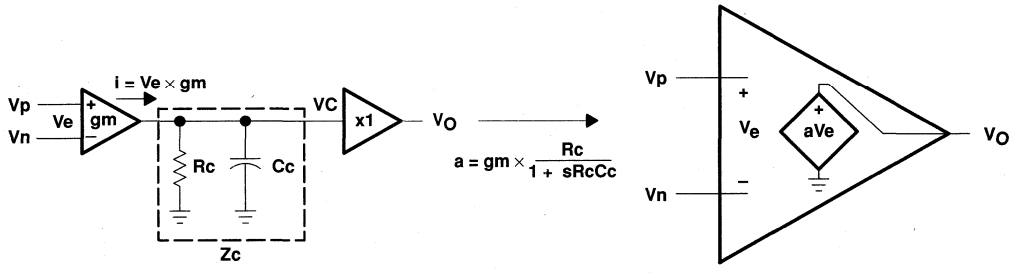


Figure 1. Basic Dominant Pole Op Amp Model

3 Basic Circuits and Analysis

Figure 2 (a) shows a noninverting amplifier and Figure 2 (b) shows an inverting amplifier. Both amplifier circuits are constructed by adding negative feedback to the basic op amp model.

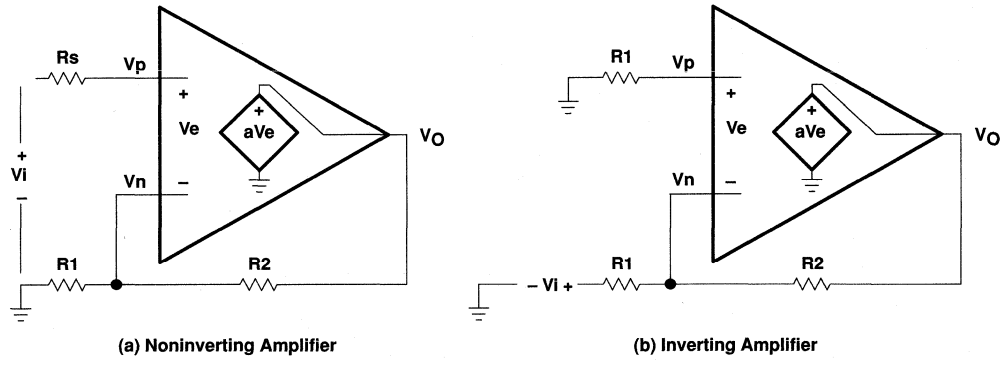


Figure 2. Amplifier Circuits Constructed with Negative Feedback

These circuits are represented in gain block diagram form as shown in Figure 3 (a) and (b). Gain block diagrams are a powerful tool in understanding gain and stability analysis.

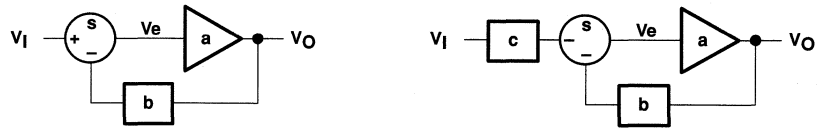


Figure 3. Gain-Block Diagrams

In the gain block diagrams:

$a = gm \times \frac{R_c}{1 + sRcCc}$, $b = \frac{R1}{R1 + R2}$, *and* $c = \frac{R2}{R1 + R2}$. Summing node *s* either inverts or passes unchanged each input—depending on the sign at the input—and adds the results together to produce the output.

3.1 Gain Analysis

In the gain block diagram of Figure 3 (a) (noninverting amplifier), Vo=aVe=a(Vi–bVo). Solving the transfer function:

$$\frac{V_O}{V_I} = \left(\frac{1}{b}\right)\left[\frac{1}{1 + \frac{1}{ab}}\right] = \left(\frac{R1 + R2}{R1}\right)\left[\frac{1}{1 + \left(\frac{1 + sRcCc}{gmRc}\right)\left(\frac{R1 + R2}{R1}\right)}\right] \quad (1)$$

This equation describes a single pole transfer function where $\frac{1}{b}$ is the dc gain and the pole is at the frequency where $\frac{1}{ab} = 1$

In the gain block diagram of Figure 3 (b) (inverting amplifier), $Vo = aVe = a(-cVi - bVo)$. Solving the transfer function:

$$\frac{V_O}{V_I} = -\left(\frac{c}{b}\right)\left[\frac{1}{1 + \frac{1}{ab}}\right] = \left(\frac{R2}{R1}\right)\left[\frac{1}{1 + \left(\frac{1 + sRcCc}{gmRc}\right)\left(\frac{R1 + R2}{R1}\right)}\right] \quad (2)$$

This equation describes a single pole transfer function where $-\frac{c}{b}$ is the dc gain and the pole is at the frequency where $\frac{1}{ab} = 1$.

Figure 4 shows the results of a spice simulation of the circuits with *R1* and *R2* = 100 kΩ, and *Rs* = 50 kΩ. As expected, the circuit gains are flat from dc to the point where $\frac{1}{ab} = 1$, and then roll-off at –20dB/dec. The open loop gain is plotted for reference.

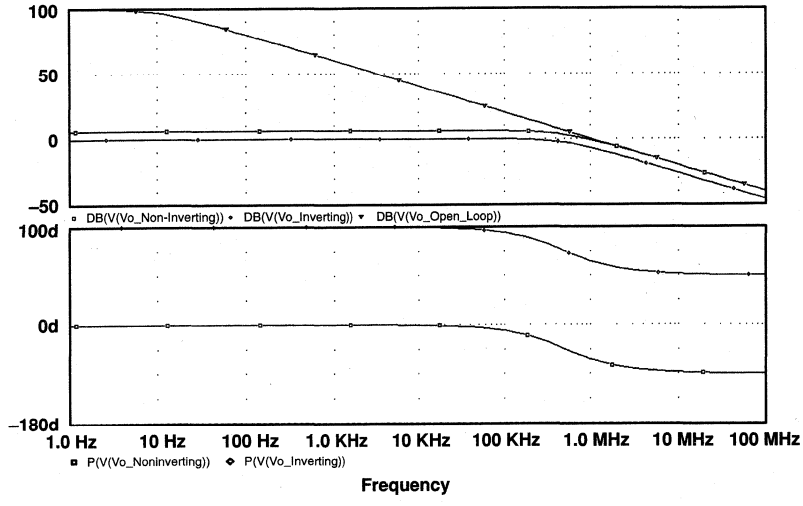


Figure 4. Spice Simulation of Noninverting and Inverting Amplifier

3.1.1 Stability Analysis

Using either gain block diagram, consider a signal traversing the loop from *Ve*, through the gain block *a,* to *Vo*, back through the gain block *b,* and the summing node *s* to *Ve*. If, while traversing this loop, the signal experiences a phase shift of 0°, or any integer multiple of 360°, and a gain equal to or greater than 1, it will reinforce itself causing the circuit to oscillate. Since there is a phase shift of 180° in the summing node *s,* this equates to:

$|ab| \geq 1 \& \angle ab = -180° \rightarrow$ *Oscillation.*

In reality, anything close to this usually causes unacceptable overshoot and ringing.

The product of the open loop gain of the op amp, *a*, and the feedback factor, *b,* is of special significance and is often termed the loop gain or the loop transmission. To determine the stability of an op amp circuit, consider the magnitude, $|ab|$, and phase, $\angle ab$.

Figure 5 shows dB $|a|$ and dB $\frac{1}{b}$ plotted along with $\angle ab$ for the one-pole op amp model in either amplifier circuit with purely resistive feedback (R1=R2=100K). It is obvious that, since the maximum phase shift in $\angle ab$ is –90°, the circuits are stable.

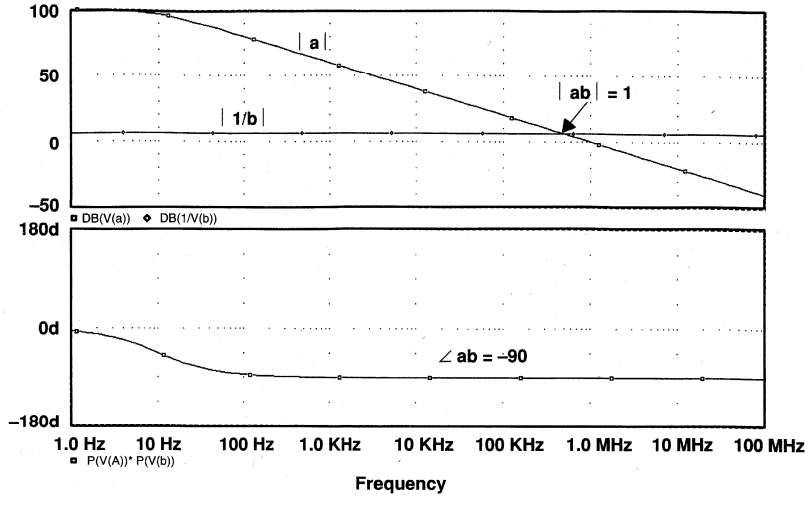


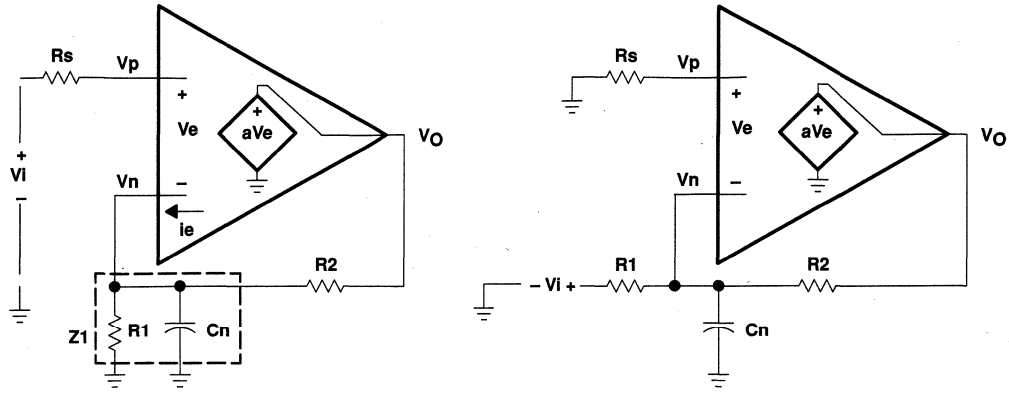
Figure 5. Loop Gain Magnitude and Phase Plot

At the point where dB $|a|$ and dB $\left|\frac{1}{b}\right|$ intersect, dB $|a|$ – dB $\left|\frac{1}{b}\right| = 0$. This is the same as *log* $|a|$ + *log* $|b| = 0$, and taking the anti-log; $|ab| = 1$.

The slope of dB $|a|$ or dB $\left|\frac{1}{b}\right|$ indicates their phase: −40 dB/dec = −180°, −20 dB/dec = −90°, 0 dB/dec = 0°, 20 dB/dec = 90°, 40 dB/dec = 180°, etc. Since $\left|\frac{1}{b}\right|$ is the inverse of $|b|$, the sign of its phase is opposite, i.e., if $\angle b$=−90° then $\angle \frac{1}{b} = 90°$. Therefore a rate of closure = 40 dB/dec between dB $|a|$ and dB $\left|\frac{1}{b}\right|$ indicates $\angle ab$=−180° and the circuit is normally unstable. Plotting dB $|a|$ and dB $\left|\frac{1}{b}\right|$ on a log scale gives a visual indication of the stability of the circuit.

4 Capacitance at the Inverting Input

Figure 6 (a) and (b) show adding *Cn* to the noninverting and inverting amplifier circuits.



(a) Noninverting Amplifier (b) Inverting Amplifier

Figure 6. Adding *Cn* to Amplifier Circuits

4.1 Gain Analysis with *Cn*

Making use of the block diagrams and their related circuit solutions, determine how *Cn* has modified the gain block values and substitute as required.

For the noninverting amplifier shown in Figure 6 (a):

$$Vn = Vo\frac{Z1}{Z1 + R2}$$

where $Z1 = \dfrac{R1}{1 + sR1Cn}$.

Solving for the modified feedback factor:

$$b = \frac{Z1}{Z1 + R2} = \left(\frac{R1}{1 + sR1Cn}\right)\left[\frac{1}{\left(\frac{R1}{1+sR1Cn}\right) + R2}\right] = \frac{1}{\frac{R1+R2}{R1} + sR2Cn} \qquad (3)$$

For the inverting amplifier shown in Figure 6 (b) writing the node equation at *Vn* results in:

$$\frac{Vn-Vi}{R1} + Vn \times sCn + \frac{Vn-Vo}{R2} = 0.$$

Therefore,

$$Vn = Vi\left(\frac{R2}{R1 + R2 + sCnR1R2}\right) + \left(\frac{Vo(R1)}{R1 + R2 + sCnR1R2}\right)$$

$$= Vi\left[\frac{1}{\frac{R1+R2}{R2} + sCnR1}\right] + Vo\left[\frac{1}{\frac{R1+R2}{R1} + sCnR2}\right]$$

As above:

$$b = \frac{1}{\frac{R1+R2}{R1} + sR2Cn}, \text{ and } c = \frac{1}{\frac{R1+R2}{R2} + sR2Cn}$$

Using these values in the solutions to the gain block diagrams of Figure 3, the noninverting amplifier's gain, with *Cn* added to the circuit, is:

$$\frac{Vo}{Vi} = \left(\frac{1}{b}\right)\left[\frac{1}{1 + \frac{1}{ab}}\right] = \left(\frac{R1 + R2}{R1} + sR2Cn\right)\left[\frac{1}{1 + \left(\frac{1+sRcCc}{gmRc}\right)\left(\frac{R1+R2}{R1} + sR2Cn\right)}\right] \quad (4)$$

and the inverting amplifier's gain, with *Cn* added to the circuit, is:

$$\frac{Vo}{Vi} = -\left(\frac{c}{b}\right)\left[\frac{1}{1 + \frac{1}{ab}}\right] = -\left[\frac{\frac{R1+R2}{R1} + sR2Cn}{\frac{R1}{\frac{R1+R2}{R2} + sR1Cn}}\right]\left[\frac{1}{1 + \left(\frac{1+sRcCc}{gmRc}\right)\left(\frac{R1+R2}{R1} + sR2Cn\right)}\right] \quad (5)$$

$$= -\left(\frac{R2}{R1}\right)\left[\frac{\frac{R1+R2}{R2} + sR1Cn}{\frac{R1+R2}{R2} + sR1Cn}\right]\left[\frac{1}{1 + \left(\frac{1}{a}\right)\left(\frac{R1+R2}{R1} + sR2Cn\right)}\right]$$

$$= -\left(\frac{R2}{R1}\right)\left[\frac{1}{1 + \left(\frac{1+sRcCc}{gmRc}\right)\left(\frac{R1+R2}{R1} + sR2Cn\right)}\right]$$

Figure 7 shows the results of a spice simulation of both amplifiers with *Cn* = 15.9 nF, resistors *R1* and *R2* = 100 kΩ, and *Rs* = 50 kΩ. Refer to it while taking a closer look at Equations 4 and 5.

In Equation 4, the first term

$$\left(\frac{R1 + R2}{R1} + sR2Cn\right)$$

contains a zero at

$$f_z = \frac{R1 + R2}{2\pi R1R2Cn}.$$

In the spice simulation we see effects of this zero as the gain begins to increase at around 200 Hz. In the second term of Equation 4, substitute

$Rm = \frac{1}{gm}$, to get

$$\left[\frac{1}{1 + \left(\frac{Rm}{Rc} + sRmCc\right)\left(\frac{R1 + R2}{R1} + sR2Cn\right)}\right]$$

$$= \frac{1}{s^2(RmCcR2Cn) + s\left(R2Cn\frac{Rm}{Rc} + RmCc\frac{R1 + R2}{R1}\right) + 1 + \left(\frac{Rm}{Rc}\right)\left(\frac{R1 + R2}{R1}\right)}$$

Solving the characteristic equation for s^2 in the denominator we find that the transfer function has a complex conjugate pole at $s_{1,2} = -660 \pm j62890$. Taking only the dominant terms in the equation, the double pole can be approximated in the frequency domain at:

$$P_{1,2} = \frac{1}{2\pi\sqrt{RmCcR2Cn}} = 10\ kHz,$$

with the model values as simulated. At this frequency the denominator tends to zero and the gain theoretically increases toward infinity. What we see on the simulation results is peaking in the gain plot and a rapid 180° phase shift in the phase plot at 10 kHz. The circuit is unstable.

In Equation 5, notice that the frequency effects of the capacitor cancel out of the first term of the transfer function. The simulation results show the gain is flat until the second term, which is identical to Equation 4, causes peaking in the gain plot, and a rapid 180° phase shift in the phase plot at 10 kHz. This circuit is also unstable.

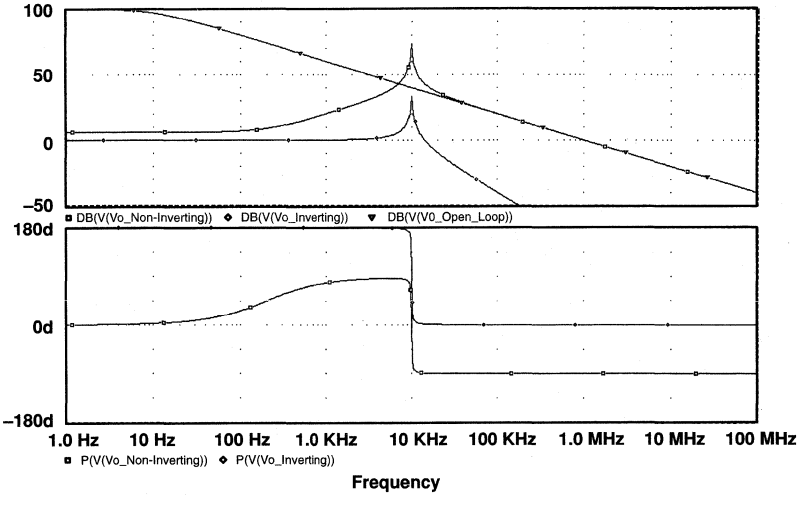


Figure 7. Spice Simulation of *Cn* in Noninverting and Inverting Amplifiers

4.1.1 Stability Analysis with Cn

To analyze stability with *Cn* added to the amplifier circuit, use the modified feedback factor,

$$b = \frac{1}{\frac{R1 + R2}{R1} + sR2Cn}$$

At low frequencies where

$$\frac{R1 + R2}{R1} >> 2\pi fR2Cn, \frac{1}{b} \cong \frac{R1 + R2}{R1}$$

and the plot is flat ($\angle b = 0°$). As frequency increases, eventually $\frac{R1 + R2}{R1} = 2\pi fR2Cn$. At this frequency $\left|\frac{1}{b}\right| = \left(\frac{R1 + R2}{R1}\right)(\sqrt{2})$ ($\angle b = -45°$). Above this frequency $\left|\frac{1}{b}\right|$ increases at 20dB/dec ($\angle b = -90°$). Depending on the value of *Cn*, there are two possible scenarios:

5. The break frequency is below the frequency where $\left|\frac{1}{b}\right|$ and $|a|$ intersect. This causes the rate of closure between $\left|\frac{1}{b}\right|$ and $|a|$ to be 40dB/dec. This is an unstable situation and will cause oscillations (or peaking) near this frequency. Reference $\frac{1}{b1}$ in Figure 8 and the results of the spice simulation shown in Figure 7.
6. The break frequency is above the frequency where $\left|\frac{1}{b}\right|$ and $|a|$ intersect. There is no effect in the pass band of the amplifier. Reference $\frac{1}{b2}$ in Figure 8.

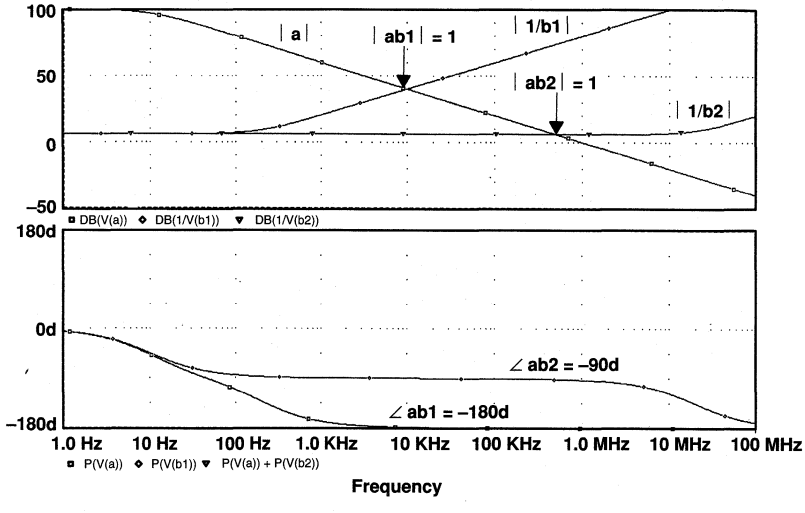


Figure 8. Loop Gain Magnitude and Phase Asymptote Plots with *Cn*

4.1.2 Compensating for the Effects of Cn

1. Reduce the value of *Cn* by removing ground or power plane around the circuit trace to the inverting input.
2. Reduce the value of *R2*.
3. For noninverting amplifier, place a capacitor $C2 = Cn\frac{R1}{R2}$ in parallel with *R2*.
4. For inverting amplifier, place a capacitor $C2 = Cn\frac{R1}{R2}$ in parallel with *R2*, and place a capacitor *C1=Cn* in parallel with *R1*.

Methods 1 and 2 attempt to move the effect of *Cn* to a higher frequency where it does not interfere with normal operation.

Method 3 is used for the noninverting amplifier. It cancels the effect of *Cn*.

To solve the modified transfer function with *C2* in parallel with *R2*, substitute *Z2* for *R2*, where $Z2 = \frac{R2}{1 + sR2C2}$, in the derivation of *b* so that:

(6)

$$b = \frac{Vn}{Vo} = \frac{Z1}{Z1 + Z2} = \left[\frac{\left(\frac{R1}{1+sR1Cn}\right)}{\left(\frac{R1}{1+sR1Cn}\right) + \left(\frac{R2}{1+sR2C2}\right)}\right] = \frac{1}{1 + \left(\frac{R2}{R1}\right)\left(\frac{1+sR1Cn}{1+sR2C2}\right)}$$

By setting $C2 = Cn\frac{R1}{R2}$, Equation 6 becomes:

$$b = \frac{1}{1 + \left(\frac{R2}{R1}\right)\left(\frac{1+sR1Cn}{1+sR1Cn}\right)} = \frac{1}{\left(\frac{R1+R2}{R1}\right)} = \left(\frac{R1}{R1 + R2}\right).$$

Therefore, with the proper value of *C2* the effect of *Cn* is cancelled and the feedback factor looks purely resistive.

This works so well for the noninverting amplifier, let's investigate doing the same thing with the inverting amplifier. Placing $C2 = Cn\frac{R1}{R2}$ across *R2* will cancel the effect of *Cn* so that *b* is purely resistive as shown above, but it causes another problem. Recalculating *c* with *C2* added we find:

$$c = \frac{Z2}{R1 + Z2} \text{ where } Z2 = \frac{R2}{1 + sR2C2||Cn} = \frac{1}{\frac{1}{R2} + sCx} \text{ where } Cx = C2||Cn.$$

In the transfer function, $\frac{Vo}{Vi} = -\left(\frac{c}{b}\right)\left[\frac{1}{1 + \frac{1}{ab}}\right]$, the second term is fine, but expanding out the first term we find:

$$\left(\frac{c}{b}\right) = \left(\frac{R2}{1 + sR2Cx}\right)\left[\frac{1}{R1 + \frac{R2}{1+sR2Cx}}\right]\left(\frac{R1 + R2}{R1}\right) = \left(\frac{R2}{R1}\right)\left[\frac{1}{1 + \frac{sR1R2Cx}{R1+R2}}\right]$$

Obviously we now have a pole in the transfer function at $f_p = 2\pi Cx\left(\frac{R1 + R2}{R1R2}\right)$ that limits the circuit's bandwidth. To cancel this pole, a zero needs to be added to the transfer function. Placing a capacitor, *C1*, across *R1* will create a zero in the transfer function.

Again c and b need to be recalculated. We already have the solution in the form of Equation 6, and by proper substitution:

$$b = \frac{Vn}{Vo} = \left[\frac{\left(\frac{R1}{1+sR1Cn||C1}\right)}{\left(\frac{R1}{1+sR1Cn||C1}\right) + \left(\frac{R2}{1+sR2C2}\right)}\right] = \frac{1}{1 + \left(\frac{R2}{R1}\right)\left(\frac{1+sR1Cn||C1}{1+sR2C2}\right)} \quad (7)$$

$$c = \frac{Vn}{Vi} = \left[\frac{\left(\frac{R2}{1+sR2Cn||C2}\right)}{\left(\frac{R2}{1+sR2Cn||C2}\right) + \left(\frac{R1}{1+sR1C1}\right)}\right] = \frac{1}{1 + \left(\frac{R1}{R2}\right)\left(\frac{1+sR2Cn||C2}{1+sR1C1}\right)}$$

$$\left(\frac{c}{b}\right) = \frac{1 + \left(\frac{R2}{R1}\right)\left(\frac{1+sR1Cn||C1}{1+sR2C2}\right)}{1 + \left(\frac{R1}{R2}\right)\left(\frac{1+sR2Cn||C2}{1+sR1C1}\right)}$$

Setting $C2 = (Cn||C1)\frac{R1}{R2}$ in the numerator, simultaneously with setting $C1 = (Cn||C2)\frac{R2}{R1}$ in the denominator, results in cancellation. The problem is that this cannot be simultaneously achieved.

To arrive at a suitable compromise, assume that placing $C2 = Cn\frac{R1}{R2}$ across *R2* cancels the effect of *Cn* in the feedback path as described above. Then, isolate the signal path between *Vi* and *Vn* by assuming *R2* is open. With this scenario, *Cn* is acting with *R1* to create a pole in the input signal path and placing an equal value capacitor in parallel with *R1* will create a zero to cancel its effect.

Figure 9 shows the results of a spice simulation where methods 3 and 4 are used to compensate for *Cn* = 15.9 nF. *C2* = 15.9 F in the noninverting amplifier and *C1* = *C2* = 15.9 F in the inverting amplifier. In both amplifier circuits, resistors *R1* and *R2* = 100 kΩ, and *Rs* = 50 kΩ. The plots show excellent results.

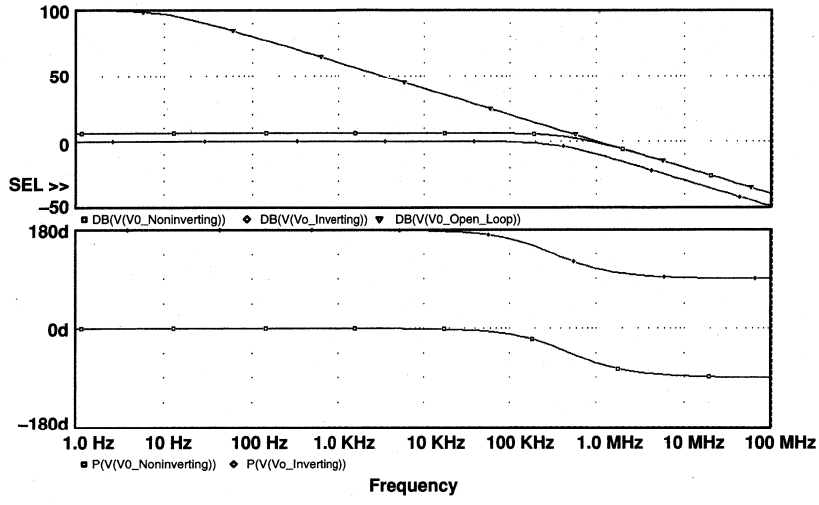


Figure 9. Simulation Results with C1 and C2 Added to Compensate for *Cn*

The action of any op amp operated with negative feedback is such that it tries to maintain 0 V across the input terminals. In the inverting amplifier, the op amp works to keep 0V (and thus 0 charge) across *Cn*. Because capacitance is the ratio of charge to potential, the effective capacitance of *Cn* is greatly reduced. In the noninverting amplifier *Cn* is charged and discharged in response to *Vi*. Thus the impact of *Cn* depends on topology. Lab results verify that, in inverting amplifier topologies, the effective value of *Cn* will be reduced by the action of the op amp, and tends to be less problematic than in noninverting topologies. Figure 10 shows that the effects of adding *Cn* to a noninverting amplifier are much worse than adding 10 times the same amount to an inverting amplifier with similar circuit components.

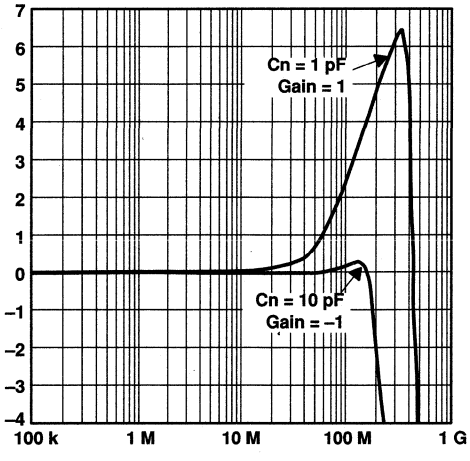


Figure 10. Effect of *Cn* in Inverting and Noninverting Amplifier

5 Capacitance at the Noninverting Input

In Figure 11 *Cp* is added to the amplifier circuits.

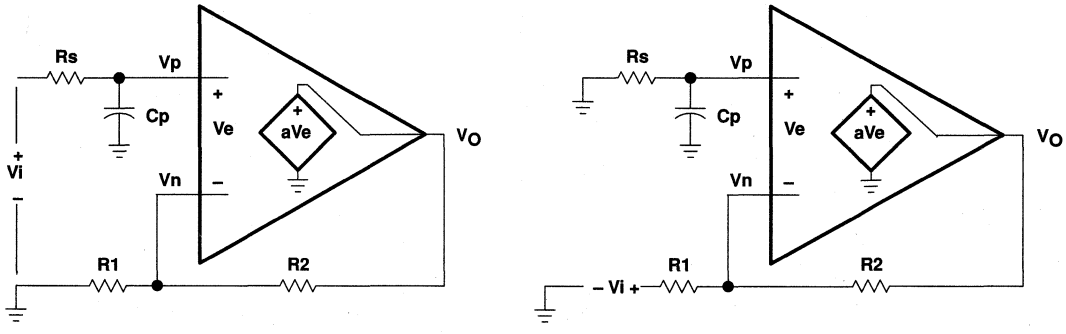


Figure 11. Adding *Cp* to Amplifier Circuits

5.1 Gain Analysis with *Cp*

In the case of the noninverting amplifier, the voltage seen at the noninverting input is modified so that $Vp = Vi\left(\frac{1}{1 + sRsCp}\right)$. Thus there is a pole in the input signal path before the signal reaches the input of the op amp. *Rs* and *Cp* form a low pass filter between *Vi* and *Vp*. If the break frequency is above the frequency at which $\left|\frac{1}{b}\right|$ intersects $|a|$, there is no effect on the operation of the circuit in the normal frequencies of operation.

The gain of the inverting amplifier is not affected by adding *Cp* to the circuit.

Figure 14 shows the results of a spice simulation where *Cp* = 15.9 nF. In both amplifier circuits, resistors *R1* and *R2* = 100 kΩ, and *Rs* = 50 kΩ. The plot shows a pole in the transfer function of the noninverting amplifier, whereas the inverting amplifier is unaffected.

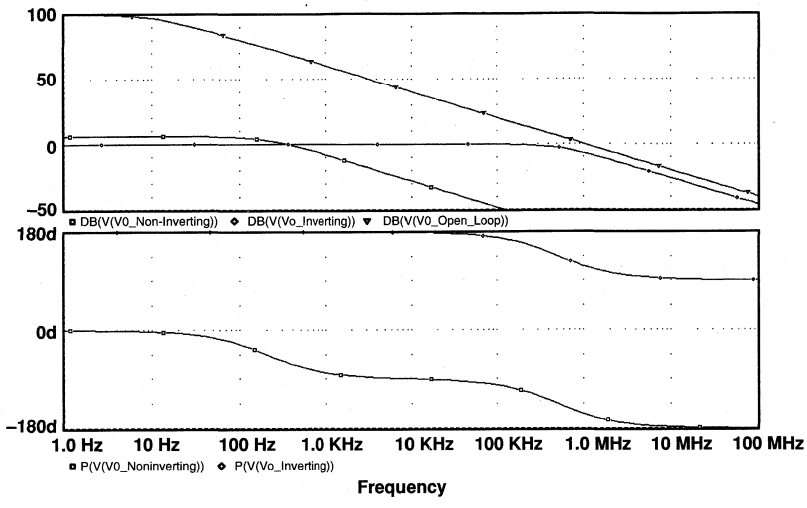


Figure 12. Spice Simulation with *Cp* in Noninverting and Inverting Amplifier Circuits

5.2 Stability Analysis with *Cp*

There is no change in the loop gain and thus no effect on stability for either amplifier circuit.

5.3 Compensating for the Effects of *Cp*

To compensate for the effect of capacitance at the noninverting input:

1. Reduce the value of *Cp* by removing ground or power plane around the circuit trace to the noninverting input.
2. Reduce the value of *Rs*.
3. Place a capacitor, *Cs,* in parallel with *Rs* so that *Cs>>Cp*.

Methods 1 and 2 attempt to move the effect of *Cp* to a higher frequency where it does not affect transmission of signals in the pass band of the amplifier.

Method 3 tries to cancel the effect of *Cp*. The modified transfer function with *Cs* in parallel with *Rs* is:

$$\frac{Vp}{Vi} = \left(\frac{1 + sRsCs}{1 + sRs(Cp + Cs)}\right) \tag{8}$$

If $Cs>>Cp$, then $\left(\frac{1 + sRsCs}{1 + sRs(Cp + Cs)}\right) \cong 1$ *and* $Vp \cong Vi$.

Figure 13 shows the results of a spice simulation of the previous noninverting amplifier circuit where a 159-nF and a 1.59-μF capacitor is placed in parallel with *Rs* to compensate for *Cp* = 15.9 nf. The plot shows that a 10:1 ratio is good—loss of 1 db in gain at higher frequencies, but with a 100:1 ratio the effects of *Cp* are undetectable.

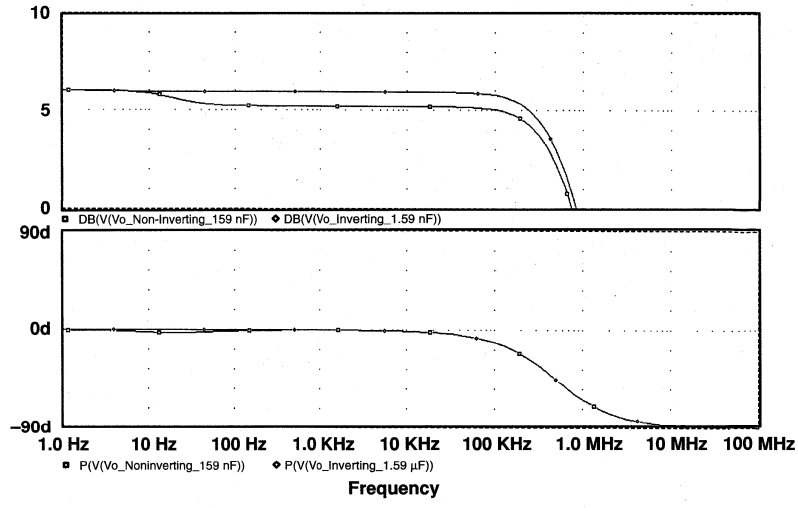
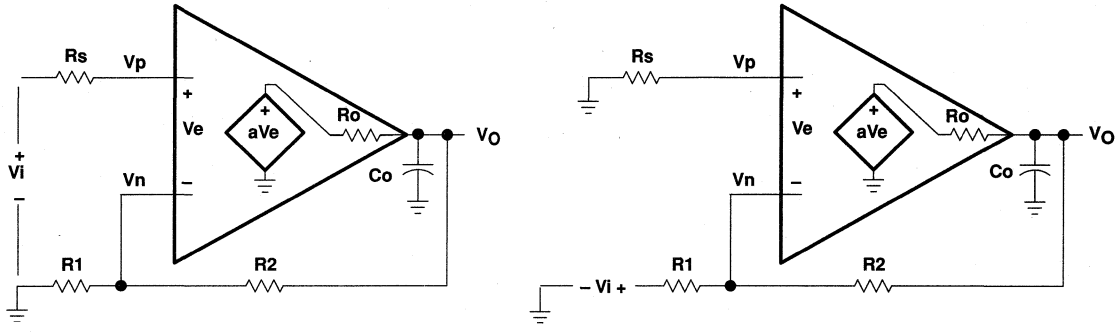


Figure 13. Spice Simulation with *Cs* Added to Compensate for *Cp* in Noninverting Amplifier

6 Output Resistance and Capacitance

Figure 14 shows *Ro* and *Co* added to the amplifier circuits. *Ro* represent the output resistance of the op amp and *Co* represents the capacitance of the load.



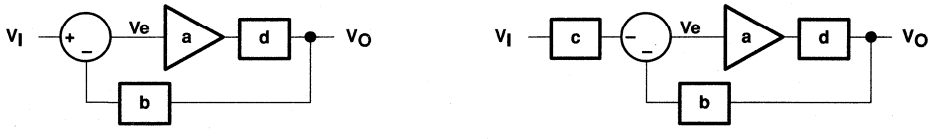
(a) Noninverting Amplifier (b) Inverting Amplifier

Figure 14. *Ro* and *Co* Added to Amplifiers

6.1 Gain Analysis with *Ro* and *Co*

Assuming that the impedance of *R2* is much higher than the impedance of *Ro* and *Co*, the gain block diagrams for the amplifiers are modified to those shown in Figure 15 where:

$$d = \frac{Vo}{aVe} = \frac{1}{1 + sRoCo}.$$



(a) Noninverting Amplifier (b) Inverting Amplifier

Figure 15. Gain Block Diagrams with *Ro* and *Co*

Using Figure 15 (a), we calculate the transfer function of the noninverting amplifier:

$$\frac{Vo}{Vi} = \frac{1}{b}\left[\frac{1}{1 + \frac{1}{abd}}\right] = \left(\frac{R1 + R2}{R1}\right)\left[\frac{1}{1 + \left(\frac{1 + sRcCc}{gmRc}\right)\left(\frac{R1 + R2}{R1}\right)(1 + sRoCo)}\right] \quad (9)$$

Using Figure 15 (b), we calculate the transfer function of the inverting amplifier:

$$\frac{Vo}{Vi} = -\left(\frac{c}{b}\right)\left[\frac{1}{1 + \frac{1}{abd}}\right] = -\left(\frac{R2}{R1}\right)\left[\frac{1}{1 + \left(\frac{1 + sRcCc}{gmRc}\right)\left(\frac{R1 + R2}{R1}\right)(1 + sRoCo)}\right] \quad (10)$$

Figure 16 shows the results of a spice simulation with Ro = 100 Ω and Co = 159 µF. Resistors $R1$ and $R2$ = 100 kΩ, and Rs = 50 kΩ. Refer to the simulation results while taking a closer look at the second term of Equations 9 and 10. Expanding the denominator of second term with $Rm = \frac{1}{gm}$ and collecting s terms:

$$s^2(RmCcRoCo)\left(\frac{R1 + R2}{R1}\right) + s\left(RoCo\left(\frac{Rm}{Rc}\right) + RmCc\right)\left(\frac{R1 + R2}{R1}\right) + 1 + \left(\frac{Rm}{Rc}\right)\left(\frac{R1 + R2}{R1}\right)$$

Solving the characteristic equation for s^2, the transfer function has a complex conjugate pole at $s_{1,2} = -63 + j14{,}063$. Taking only the dominant terms in the equation, the double pole can be approximated in the frequency domain at:

$$f_{p1,2} \cong \frac{1}{2\pi\sqrt{RmCcRoCo\left(\frac{R1 + R2}{R1}\right)}} = 2.2\ kHz,$$

with the model values as simulated. At this frequency the second term's denominator tends to zero and the gain theoretically increases to infinity. What we see on the simulation results at 2.2 kHz is significant peaking in the gain, and a rapid 180° phase shift. The circuit is unstable.

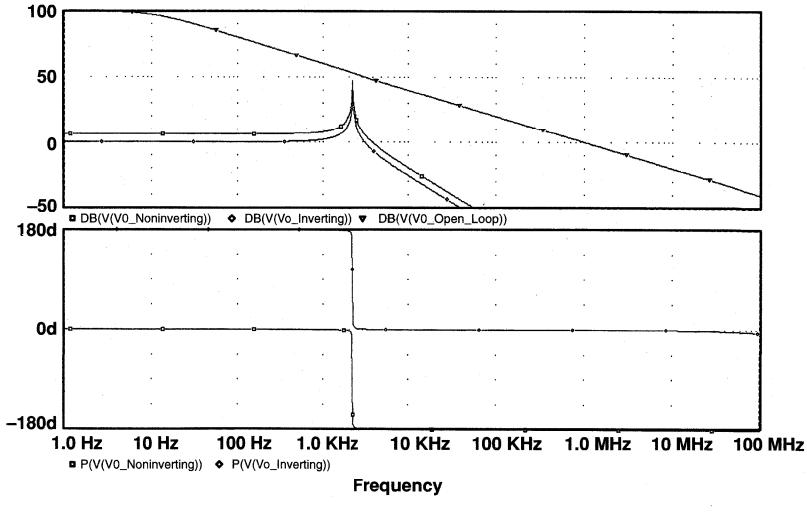


Figure 16. Spice Simulation with *Ro* and *Co*

6.2 Stability Analysis with *Ro* and *Co*

By the gain block diagrams shown in Figure 15 (a) and (b), the loop gain is now = abd for both circuits. Since gain blocks a and b are not changed, to determine the stability of the circuit, the effect of gain block d is analyzed.

As noted above, $d = \frac{Vo}{aVe} = \frac{1}{1 + sRoCo}$. At low frequencies where $1 >> 2\pi fRoCo, \frac{1}{d} \cong 1$ and the plot is flat ($\angle d = 0°$). As frequency increases, eventually $2\pi fRoCo = 1$. At this frequency $\left|\frac{1}{d}\right| = \left(\sqrt{2}\right)$, and $\angle d = -45°$. Above this frequency $\left|\frac{1}{d}\right|$ increases at 20dB/dec , and $\angle d = -90°$. Depending on the value of *Ro* and *Co,* there are two possible scenarios:

1. The break frequency is below the frequency where $\left|\frac{1}{bd}\right|$ and $|a|$ intersect. This causes the rate of closure to be 40dB/dec. This is an unstable situation and will cause oscillations (or peaking) near this frequency. Reference $\left|\frac{1}{bd1}\right|$ in Figure 17 and the results of the spice simulation shown in Figure 16.
2. The break frequency is above the frequency where $\left|\frac{1}{bd}\right|$ and $|a|$ intersect. There is no effect in the pass band of the amplifier. Reference $\left|\frac{1}{bd2}\right|$ in Figure 17.

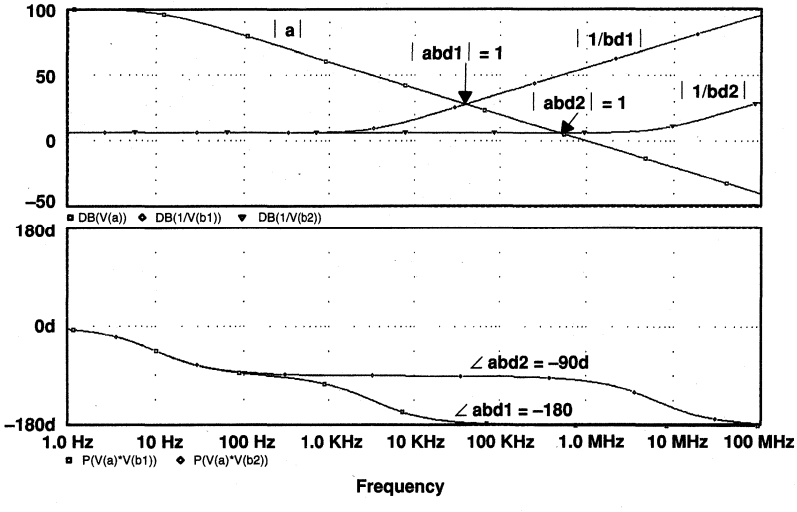


Figure 17. Loop Gain Magnitude and Phase with *Ro* and *Co*

6.3 Compensation for *Ro* and *Co*

To compensate for the effect of capacitance at the output:

1. Reduce the value of *Co* by removing ground or power plane around the circuit trace to the output.
2. Reduce the value of *Co* by minimizing the length of output cables.
3. Isolate the output pin from *Co* with a series resistor.
4. Isolate the output pin from *Co* with a series resistor, and provide phase lead compensation with a capacitor across *R2*.

Methods 1 and 2 seek to minimize the value of *Co* and thus its effects, but there is a limit to what can be done. In some cases, you will still be left with a capacitance that is too large for the amplifier to drive. Then method 3 or 4 can be used depending on your requirements.

Method 3 can be used if the resistive load is insignificant, or it is known and constant. Figure 18 shows the circuit modified with *Ri* added to isolate *Co*. By observation, adding Ri increases the phase shift seen at *Vo*, but now the feedback is taken from node *Vfb*.

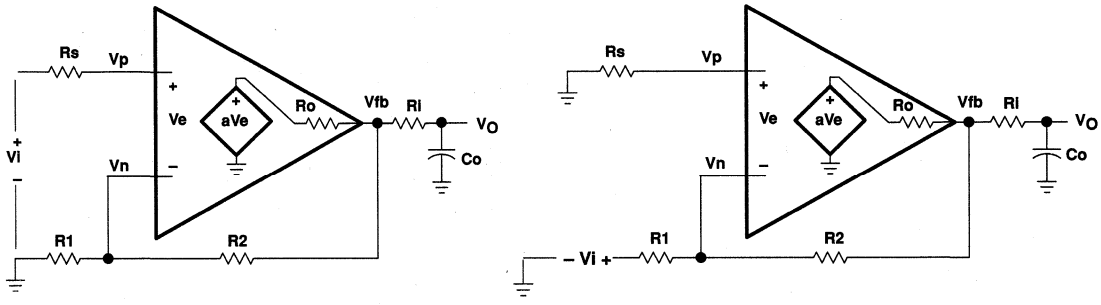


Figure 18. Isolation Resistor Added to Isolate the Feedback Loop from Effects of *Ro*

This modifies the gain block *d*. Making the assumption that the impedance of *Ro*, *Ri*, and *Co* is small compared to *R2* then:

$$d = \frac{Vfb}{aVe} = \left[\frac{Ri + \frac{1}{sCo}}{Ro + Ri + \frac{1}{sCo}}\right] = \frac{1}{\frac{Ro}{Ri} + 1 + \frac{1}{sRiCo}} + \frac{1}{1 + sCo(Ri + Ro)}.$$

Letting $z = \frac{1}{\frac{Ro}{Ri} + 1 + \frac{1}{sRiCo}}$ and $p = \frac{1}{1 + sCo(Ri + Ro)}$: $d = z + p$. z is a zero and p is a pole. Both have the same corner frequency; $f_{z,p} = \frac{1}{2\pi Co(Ri + Ro)}$. When $f << f_{z,p}$, or when $f >> f_{z,p}$ the phase is zero. The ratio of *Ri:Ro* determines the maximum phase shift near $f_{z,p}$.

Figure 19 shows a plot of the phase shift of $\frac{Vfb}{aVe}$ versus frequency with various ratios of *Ri:Ro* and Figure 20 plots the maximum phase shift vs. the ratio of *Ri:Ro*. Depending on how much the phase margin can be eroded, a ratio can be chosen to suit. Note that the amount of phase shift depends only on the resistor ratio, not the resistor or capacitor values (these set the frequency $f_{z,p}$).

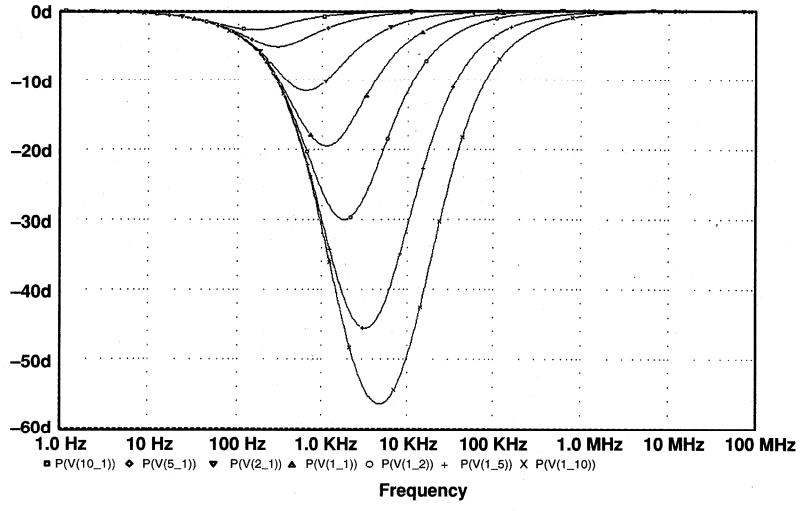


Figure 19. Phase Shift in $\frac{Vfb}{aVe}$ vs the Ratio *Ri:Ro*

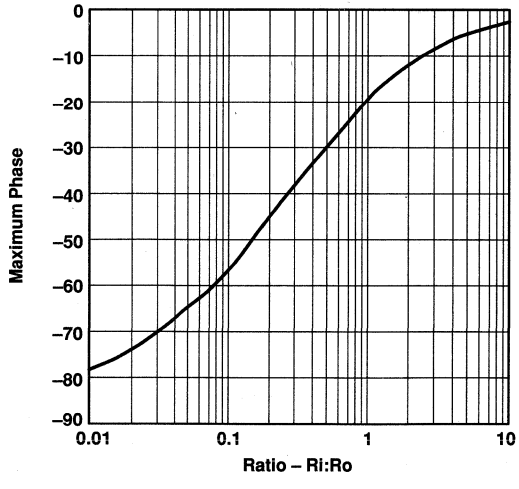


Figure 20. Maximum Phase Shift in $\frac{Vfb}{aVe}$ vs the Ratio *Ri:Ro*

Figure 21 shows simulation results with the same circuits as used for Figure 16 ($Ro = 100\ \Omega$ and $Co = 159\ \mu F$), but with $Ri = 100\ \Omega$ added to the circuit. The circuits are stable.

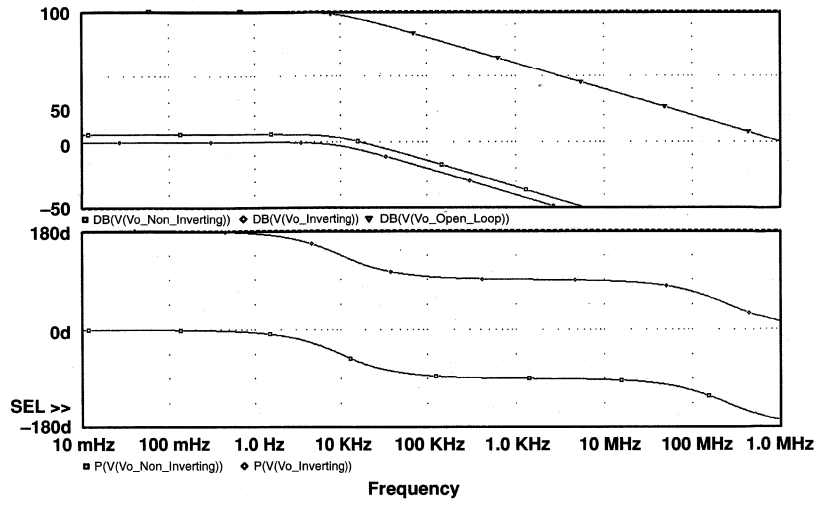


Figure 21. Spice Simulation Results with *Ri* Added to Compensate for *Ro* and *Co*

A common use of an isolation resistor is shown in Figure 22 where a video buffer circuit is drawn. To avoid line reflections, the signal is delivered to the transmission line through a 75-Ω resistor, and the transmission line is terminated at the far end with a 75-Ω resistor. To compensate for the voltage divider, the gain of the op amp is 2.

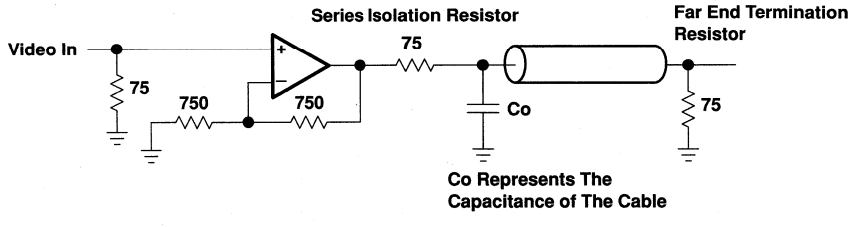
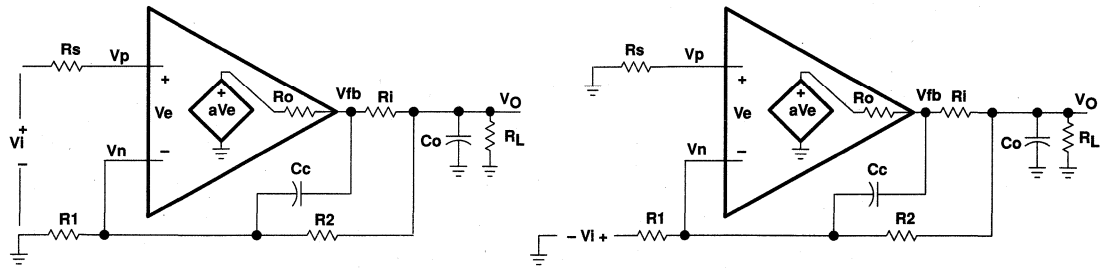


Figure 22. Video Buffer Application

If the load is unknown or dynamic in nature, method 3 is not satisfactory. Then method 4, the configuration shown in Figure 23, is used with better results. At low frequencies, the impedance of *Cc* is high in comparison with *R2*, and the feedback path is primarily from *Vo* restoring the dc and low frequency response. At higher frequencies, the impedance of *Cc* is low compared with *R2,* and the feedback path is primarily from *Vfb*, where the phase shift, due to *Co*, is buffered by *Ri*.

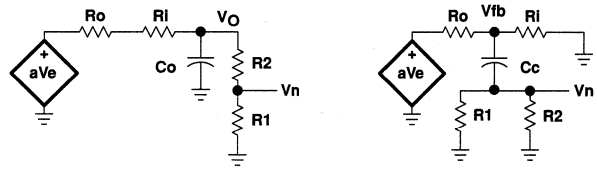


(a) Noninverting Amplifier (b) Inverting Amplifier

Figure 23. *Ri* and *Cc* Added to Compensate for Effects of *Ro* and *Co*

To solve these circuits analytically is quite cumbersome. By making some simplifications, the basic operation is more easily seen. The transfer function of interest is $\frac{Vn}{aVe}$.

Assume the impedance of *R1* and *R2* is much higher than the impedance of *Ri, Ro* and *Co*, and *Cc* << *Co*. At low frequencies, *Cc* looks like an open and the circuit can be represented as shown in Figure 24 (a). At higher frequencies *Cc* becomes active, *Co* is essentially a short, and the circuit can be represented as shown in Figure 24 (b).



(a) Low Frequency Model (a) High Frequency Model

Figure 24. Simplified Feedback Models

This breaks the feedback into low and high frequency circuits:

At low frequency: $\frac{Vn}{aVe}\left(f_{low}\right) = \left(\frac{R1}{R1 + R2}\right)\left(\frac{1}{1 + sCo(Ro + Ri)}\right)$.

At high frequency: $\frac{Vn}{aVe}\left(f_{high}\right) = \left(\frac{Ri}{Ri + Ro}\right)\left[\frac{1}{1 + \frac{1}{sCc(R1||R2)}}\right]$.

The overall feedback factor is a combination of the two so that:

$$\frac{Vn}{aVe} = \left(\frac{R1}{R1 + R2}\right)\left(\frac{1}{1 + sCo(Ro + Ri)}\right) + \left(\frac{Ri}{Ri + Ro}\right)\left[\frac{1}{1 + \frac{1}{sCc(Ro + Ri)}}\right]$$

This formula contains a pole and a zero. Choosing the value of the components so that the pole and zero are at the same frequency by setting $Cc = Co\frac{Ro + Ri}{R1||R2}$ results in the feedback path switching from *Vo* to *Vfb* as the phase shift due to *Co(Ri+Ro)* transitions to −90°.

Figure 24 shows the simulation results of adding *Cc* = 636 nf with isolation resistor, *Ri* = 100 Ω, to the feedback path (as indicated in Figure 23). The circuit is no longer unstable and the low frequency load independence of the output is restored. Simulation of the circuit shows similar results as those depicted in Figure 21, and is not shown.

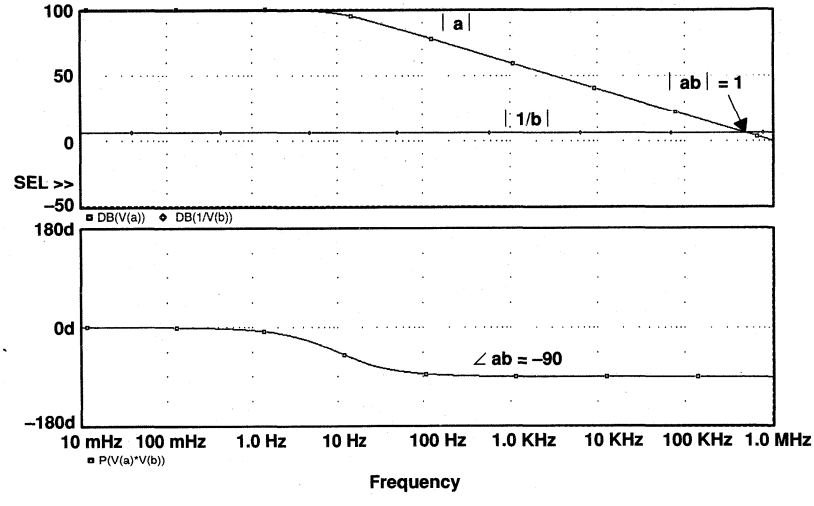


Figure 25. Simulation of Feedback Using *Ri* and *Cc* to Compensate for *Ro* and *Co*

7 Summary

The techniques described herein show means for analyzing and compensating for known component values. In circuit application, the value of parasitic components is not always known. Thus the ubiquitous rule of thumb comes into play:

1. Always connect a small, 20-pF to 100-pF, capacitor between the output and the negative input.
2. If the op amp has to drive a significant capacitance, isolate the output with a small, 20-Ω to 100-Ω, resistor.

Table 1. Noninverting Amplifier: Capacitor Location, Effect, and Compensation Summary

Topology: Noninverting Amplifier		
Capacitor Location	**Effect**	**Compensation**
All places	Various	Reduce capacitance and/or associated resistance.
Negative input, *Cn*	Gain peaking or oscillation	Compensate with $C2 = Cn\frac{R1}{R2}$ across $R2$.
Positive input, *Cp*	Reduced Bandwidth	Compensate with $C1 >> Cn$ across $R1$.
Output, *Co*	Gain peaking or oscillation	1. If load is known, isolate with resistor, $Ri = Ro$. This causes load dependence. 2. If load is unknown, isolate with resistor, $Ri = Ro$ and provide ac feedback from isolated point with $Cc = Co\frac{Ro + Ri}{R1 \| R2}$. Provide dc feedback from Vo.

Table 2. Inverting Amplifier: Capacitor Location, Effect, and Compensation Summary

Topology: Inverting Amplifier		
Capacitor Location	**Effect**	**Compensation**
All places	Various	Reduce capacitance and/or associated resistance.
Negative input, *Cn*	Gain peaking or oscillation	Compensate with $C2 = Cn\frac{R1}{R2}$ across $R2$, and $C1 = Cn$ across $R1$.
Positive input, *Cp*	None	None
Output, *Co*	Gain peaking or oscillation	1. If load is known, isolate with resistor, $Ri = Ro$. This causes load dependence. 2. If load is unknown, isolate with resistor, $Ri = Ro$ and provide ac feedback from isolated point with $Cc = Co\frac{Ro + Ri}{R1 \| R2}$. Provide dc feedback from Vo.

8 References

1. Paul R. Gray and Robert G. Meyer. *Analysis and Design of Analog Integrated Circuits.* 2d ed., John Wiley & sons, Inc., 1984.
2. Sergio Franco. *Design with Operational Amplifiers and Analog Integrated Circuits.* McGrawHill, Inc., 1988.
3. Jiri Dostal. *Operational Amplifiers.* Elsevier Scientific Publishing Co., 1981.

Electrostatic Discharge (ESD)

Application Report

Literature Number: SSYA008
May 1999

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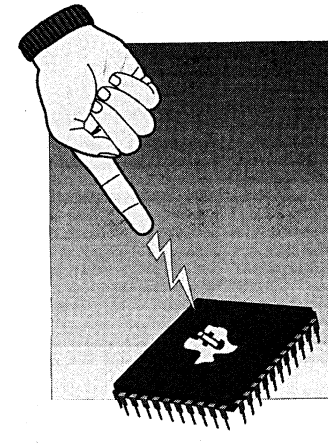
Electrostatic Discharge (ESD)

Introduction

In recent years, the semiconductor industry has made great strides in developing faster, lower-powered, and smaller devices. During the 1990s, many devices are produced with minimum structure feature size on the silicon chip of 0.25 micron. To put this size in perspective, a typical human hair is about 75 microns in diameter. However, as feature sizes get smaller and smaller, the ESD sensitivity (voltage level at which the device sustains damage) gets lower. Therefore, ESD protection and ESD handling procedures are becoming even more important in preventing ESD damage.



All semiconductor devices have an ESD voltage threshold above which they sustain damage. While circuit designers can provide some on-circuit ESD protection (typically in the 2,000 V to 4,000 V range for the human body model and in the 200 V to 300 V range for the machine model), this is well below the static voltage levels found in work areas without ESD protection. Proper ESD handling and packaging procedures must be used throughout the processing, handling, and storing of unmounted integrated circuits (ICs) and ICs mounted on circuit boards.

What is ESD and How Does It Occur?

A static charge is an unbalanced electrical charge at rest. A static discharge is created when insulator surfaces rub together or pull apart. One surface gains electrons while the other surface loses electrons. This results in an unbalanced electrical condition recognized as static charge.

When a static charge moves from one surface to another, it is called ESD. ESD is a miniature lightning bolt of static charge that moves between two surfaces that have different potentials. ESD only occurs when the voltage differential between the two surfaces is sufficiently high to break down the dielectric strength of the medium separating the two surfaces. When a static charge moves, it becomes a current that damages or destroys oxides, metalizations, and junctions. ESD can occur in one of four different ways: a charged

body can touch an IC, a charged IC can touch a grounded surface, a charged machine can touch an IC, or an electrostatic field can induce a voltage across a dielectric that is sufficient to break it down.

Latent Defects

Devices with latent ESD defects are devices that have been degraded by ESD but not destroyed. This occurs when an ESD pulse is not strong enough to destroy a device but causes damage. Often, the device suffers junction degradation through increased leakage or a decreased reverse breakdown, but the device still functions and is still within data-sheet limits. A device can be subjected to numerous weak ESD pulses, with each one further degrading a device before it finally becomes a catastrophic failure. There is no known practical screen for devices with latent ESD defects. To avoid this type of damage, devices must be continually provided with ESD protection as outlined later.

What Voltage Levels of ESD are Possible?

It has been shown that human beings can be charged up to 38,000 volts just by walking across a rug on a low-humidity day. In order for an ESD pulse to be seen, felt, or heard, it must be in the range of 3000–4000 volts. Many devices can be damaged well below this threshold. ESD damage can be seen in the failure analysis photographs shown in Figure 1.

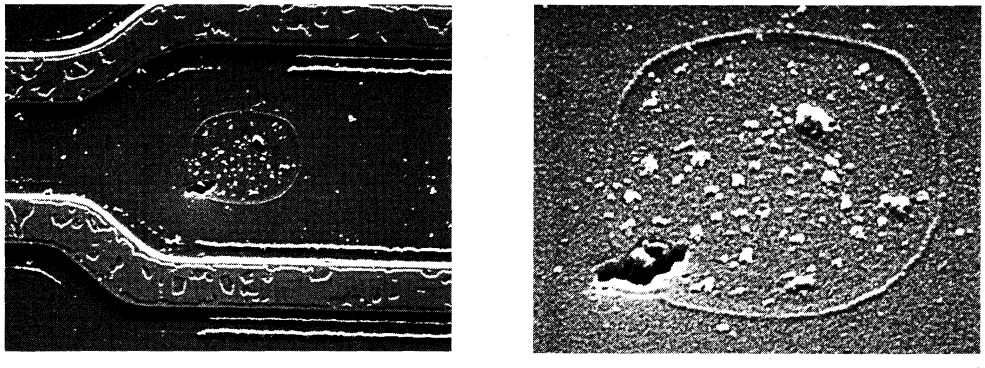


Figure 1. Punctured Barrier Junction After ESD Test at 4000 V

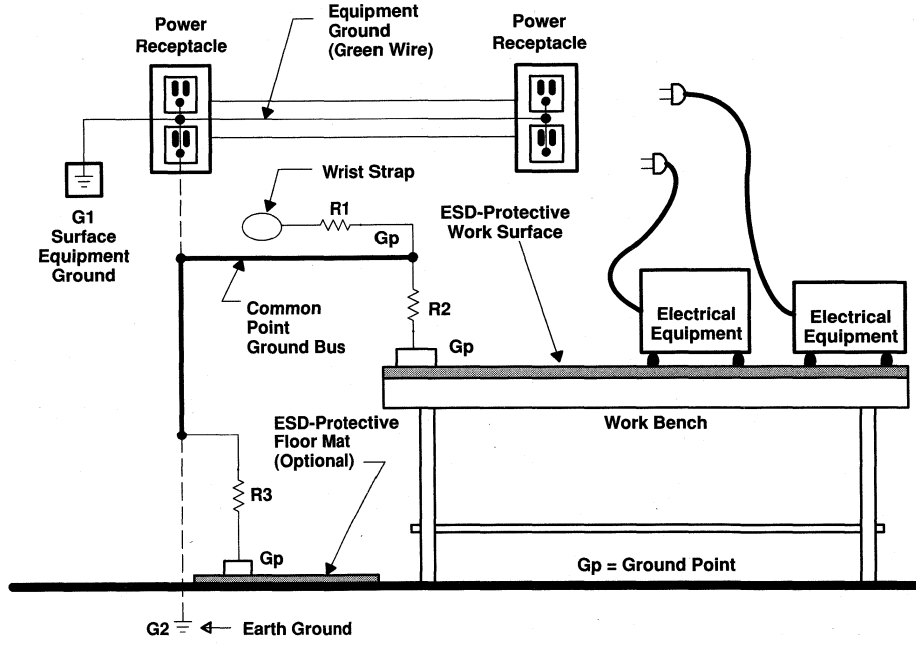
How to Avoid ESD Damage to ICs

The best way to avoid ESD damage is to keep ICs at the same potential as their surroundings. The logical reference potential is ESD ground. The first and most important rule in avoiding ESD damage is to keep ICs and everything that comes in close proximity to them at ESD ground potential. There are four supplementary rules that support this first rule.

- Any person handling the ICs should be grounded either with a wrist strap or ESD-protective footwear used in conjunction with a conductive or static-dissipative floor or floor mat.
- The work surface where devices are placed for handling, processing, testing, etc., must, be made of static-dissipative material and be grounded to ESD ground.

- All insulator materials must either be removed from the work area or must be neutralized with an ionizer. Static-generating clothing must be covered with an ESD-protective smock.
- When ICs are being stored, transferred between operations or workstations, or shipped, they must be kept in a Faraday shield container with inside surfaces (surfaces touching the ICs) that are static-dissipative.

Figure 2 shows an ESD-protected workstation.



NOTES: A. G1 (surface equipment ground) or G2 (earth ground) is acceptable for ESD ground. Where both grounds are used, they are connected (bonded) together.
B. R1 is mandatory for all wrist straps.
C. R2 (for static-dissipative work surfaces) and R3 (for ESD-protective floor mats) are optional. ESD-protective flooring are connected directly to the ESD ground without R3.
D. This ESD-protected workstation complies with JEDEC Standard No. 42.

Figure 2. ESD-Protected Workstation (Side View)

Humidity

Humidity is a very important factor in the generation of static electricity. This is especially true when insulators are present. Humidity affects the surface resistivity of insulator materials. As humidity increases, the surface resistivity decreases. This means that insulator materials rubbed together or pulled apart in a humid environment generate lower static charges than the same materials rubbed together or pulled apart in a dry environment. It is recommended that relative humidity be maintained between 40% and 60%. Humidity

above 60% is uncomfortable for humans. Humidity below 40% increases the risks of static generation from insulators. Humidity is a supplementary control and is not sufficient by itself to reduce static voltages to safe levels.

Training

All personnel who must come in close proximity to ESD-sensitive ICs must have received ESD training. These personnel should be retrained at least once per year. No ESD program can be successful unless the people who handle the ICs understand the need for ESD controls.

ESD Specification

Each area handling ESD-sensitive devices is operated in accordance with the established ESD Handling Procedure. The latest version of this controlled document is maintained in each area and is accessible to all area personnel.

ESD Coordinator

The ESD coordinator has overall responsibility for the ESD program. The ESD coordinator is responsible for ESD training, material evaluation, and writing and updating of the ESD Handling Procedure.

Audits

Periodic audits ranging from daily to yearly are held to ensure that all ESD handling procedures are being followed and that all ESD materials (wrist straps, heel straps, ionizers, table mats, floor mats, etc.) are functioning properly.

TI ESD Handling Procedure

The TI Worldwide ESD Handling Procedure is available to customers upon request.

Feedback Amplifier Analysis Tools Application Report

Ronald Mancini

Literature Number: SLOA017
April 1999

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Contents

List of Figures

Feedback Amplifier Analysis Tools

Ronald Mancini

ABSTRACT

This paper gives the reader a command of the simplest set of tools required to analyze and design feedback amplifiers. These tools are fundamental, and they form the basis of feedback analysis and design.

1 Introduction

Analysis tools have something in common with medicine because they both can be distasteful but necessary. Medicine often tastes bad or has undesirable side effects, and analysis tools involve lots of hard learning work before they can be applied to yield results. Medicine assists the body in fighting an illness; analysis tools assist the brain in learning/designing feedback circuits.

The analysis tools given here are a synopsis of salient points; thus they are detailed enough to get you where you are going without any extras. The references, along with thousands of their counterparts, must be consulted when making an in-depth study of the field. Aspirin, home remedies, and good health practice handle the majority of health problems, and these analysis tools solve the majority of circuit problems.

I have little patience; therefore I would not study these tools in detail prior to reading an application note. A little advanced study however, pays off for those who have patience.

2 Block Diagram Math and Manipulations

Electronic systems and circuits are often represented by block diagrams, and block diagrams have a unique algebra and set of transformations.[1] The block diagrams are used because they are a shorthand pictorial representation of the cause-and-effect relationship between the input and output in a real system. They are a convenient method for characterizing the functional relationships between components. It is not necessary to understand the functional details of a block to manipulate a block diagram.

The input impedance of each block is assumed to be infinite to preclude loading. Also, the output impedance of each block is assumed to be zero to enable high fan-out. The systems designer sets the actual impedance levels, but the fan-out assumption is valid because the block designers adhere to the system designer's specifications. All blocks multiply the input times the block quantity (see Figure 1) unless otherwise specified within the block. The quantity within the block can be a constant as shown in Figure 1(c), or it can be a complex math function involving Laplace transforms. The blocks can perform time-based operations such as differentiation and integration.

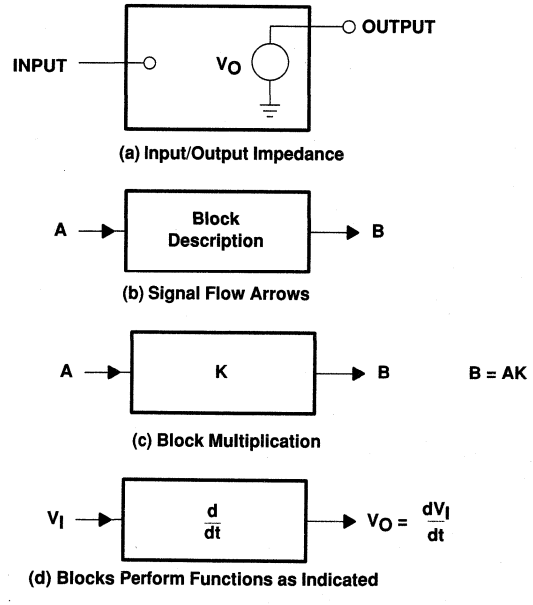

Figure 1. Definition of Blocks

Adding and subtracting are done in special blocks called summing points. Figure 2 gives several examples of summing points. Summing points can have unlimited inputs, can add or subtract, and can have mixed signs yielding addition and subtraction within a single summing point. Figure 3 defines the terms in a typical control system, and Figure 4 defines the terms in a typical electronic feedback system. Multiloop feedback systems (Figure 5) are intimidating, but they can be reduced to a single loop feedback system, as shown in the figure, by writing equations and solving for V_{OUT}/V_{IN}. An easier method for reducing multiloop feedback systems to single loop feedback systems is to follow the rules and use the transforms given in Figure 6.

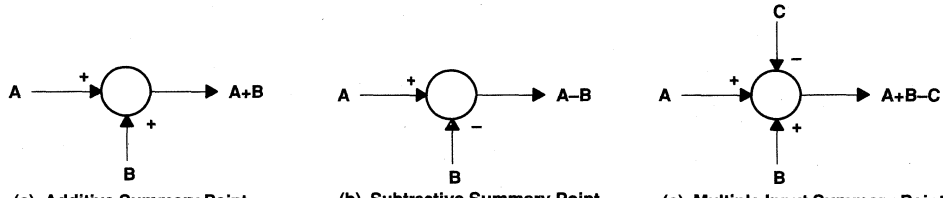

Figure 2. Summary Points

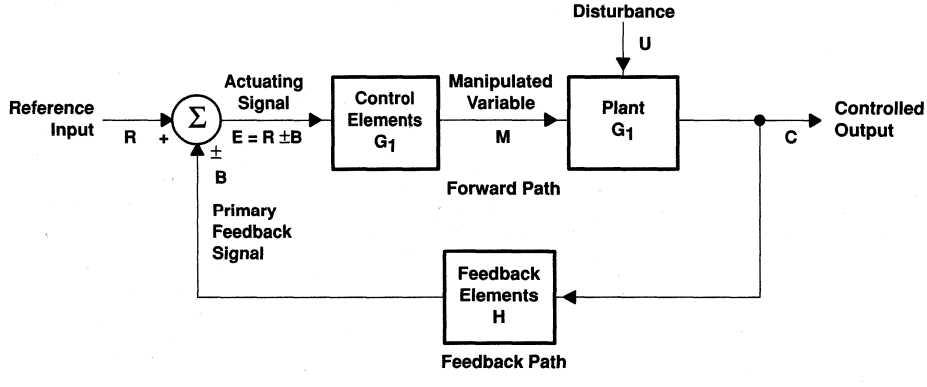

Figure 3. Definition of Control System Terms

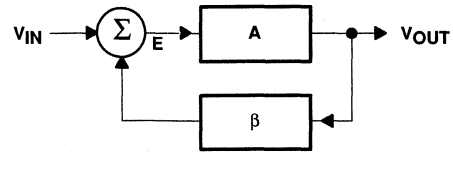

Figure 4. Definition of an Electronic Feedback Circuit

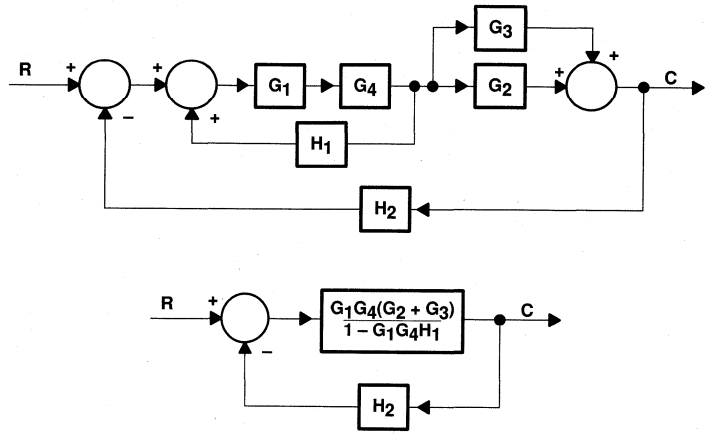

Figure 5. Multiloop Feedback System

Block diagram reduction rules:

- Combine cascade blocks.
- Combine parallel blocks.
- Eliminate interior feedback loops.
- Shift summing points to the left.
- Shift takeoff points to the right.
- Repeat until canonical form is obtained.

Figure 6 gives the block diagram transforms. The idea is to reduce the diagram to its canonical form because the canonical feedback loop is the simplest form of a feedback loop, and its analysis is well documented. All feedback systems can be reduced to the canonical form, so all feedback systems can be analyzed with the same math. A canonical loop exists for each input to a feedback system; although the stability dynamics are independent of the input, the output results are input dependent. The response of each input of a multiple input feedback system can be analyzed separately and added through superposition.

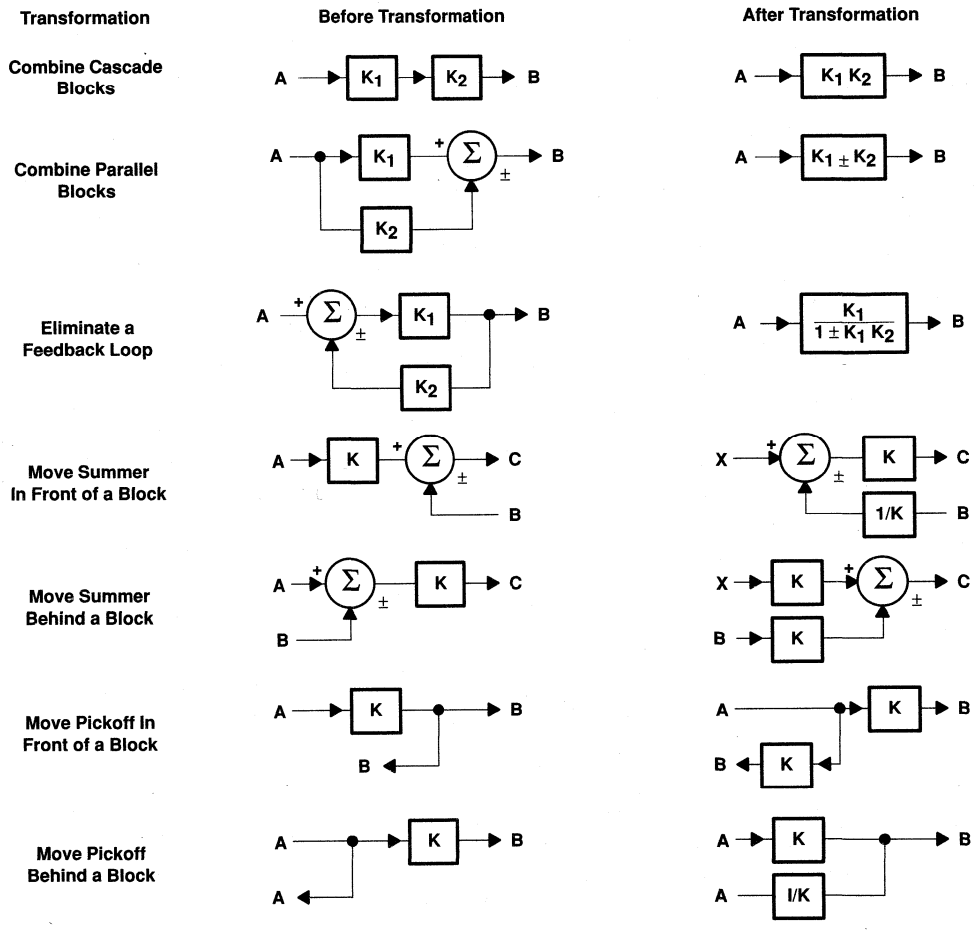

Figure 6. Block Diagram Transforms

3 Feedback Equation and Stability

Figure 7 shows the canonical form of a feedback loop with control system and electronic system terms. The terms make no difference except that they have meaning to the system engineers, but the math does have meaning, and it is identical for both types of terms. The electronic terms and negative feedback sign are used in this analysis, because subsequent application notes deal with electronic applications. The output equation is written in equation (1).

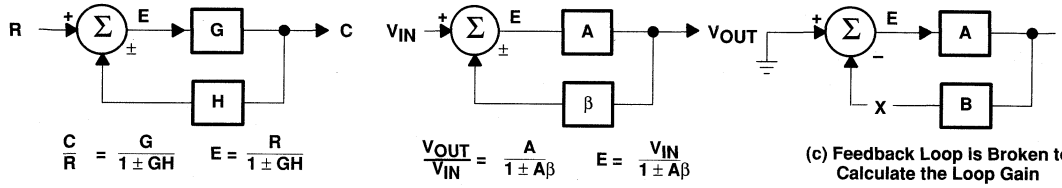

Figure 7. Commercial Feedback System

$$V_{OUT} = EA \tag{1}$$

The error equation is written in equation (2).

$$E = V_{IN} - \beta V_{OUT} \tag{2}$$

Combining equations (1) and (2) yields equation (3).

$$\frac{V_{OUT}}{A} = V_{IN} - \beta V_{OUT} \tag{3}$$

Collecting terms yields equation (4).

$$V_{OUT}\left(\frac{1}{A} + \beta\right) = V_{IN} \tag{4}$$

Rearranging terms yields the classic form of the feedback equation (5).

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \tag{5}$$

Notice that when $A\beta$ in equation (5) becomes very large with respect to one the one can be neglected, and equation (5) reduces to equation (6) which is the ideal feedback equation. Under the conditions that $A\beta >> 1$, the system gain is determined by the feedback factor β. Stable passive circuit components are used to implement the feedback factor, thus in the ideal situation, the closed loop gain is predictable and stable because β is stable and predictable.

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{\beta} \tag{6}$$

The quantity Aβ is so important that it has been given a special name: loop gain. In Figure 7, when the voltage inputs are grounded (current inputs are opened) and the loop is broken, the calculated gain is the loop gain, Aβ. Now, keep in mind that we are using complex numbers which have magnitude and direction. When the loop gain approaches minus one, or to express it mathematically $1\angle 180°$, equation (5) approaches $1/0 = \infty$. The circuit output heads for infinity as fast as it can using the equation of a straight line. If the output were not energy limited, the circuit would explode the world, but happily, it is energy limited, so somewhere it comes up against the limit.

Active devices in electronic circuits exhibit nonlinear phenomena when their output approaches a power supply rail, and the nonlinearity reduces the gain to the point where the loop gain no longer equals $1\angle 180°$. Now the circuit can do two things: first it can become stable at the power supply limit, or second, it can reverse direction (because stored charge keeps the output voltage changing) and head for the negative power supply rail.

The first state where the circuit becomes stable at a power supply limit is named lockup; the circuit will remain in the locked up state until power is removed and reapplied. The second state where the circuit bounces between power supply limits is named oscillatory. Remember, the loop gain, Aβ, is the sole factor determining stability of the circuit or system. Inputs are grounded or disconnected, so they have no bearing on stability. The loop gain criteria is analyzed in depth in the section 6.

Equations (1) and (2) are combined and rearranged to yield equation (7) which gives an indication of the system or circuit error.

$$E = \frac{V_{IN}}{1 + A\beta} \tag{7}$$

First, notice that the error is proportional to the input signal. This is the expected result because a bigger input signal results in a bigger output signal, and bigger output signals require more drive voltage. As the loop gain increases, the error decreases, thus large loop gains are attractive for minimizing errors.

4 Bode Analysis of Feedback Circuits

H. W. Bode developed a quick, accurate, and easy method of analyzing feedback amplifiers, and he published a book about his techniques in 1945.[2] Operational amplifiers had not been developed when Bode published his book, but they fall under the general classification of feedback amplifiers, so they are easily analyzed with Bode techniques. The mathematical manipulations required to analyze a feedback circuit are complicated because they involve multiplication and division. Bode developed the Bode plot which simplifies the analysis through the use of graphical techniques.

The Bode equations are log equations which take the form 20LOG(F(t)) = 20LOG(|F(t)|) + phase angle. The terms that are normally multiplied and divided can now be added and subtracted because they are log equations. The addition and subtraction is done graphically, thus easing the calculations and giving the designer a pictorial representation of circuit performance. Equation (8) is written for the low pass filter shown in Figure 8.

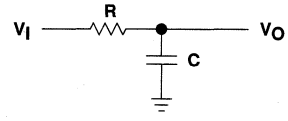

Figure 8. Low-Pass Filter

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 + RCs} = \frac{1}{1 + \tau s} \tag{8}$$

Where:

$s = j\omega$, $j = \sqrt{(-1)}$, and $RC = \tau$

The magnitude of this transfer function is $|V_{OUT}/V_{IN}| = 1/\sqrt{(1 + (\tau\omega))^2}$. This magnitude, $|V_{OUT}/V_{IN}| \cong 1$ when $\omega = 0.1/\tau$, it equals 0.707 when $\omega = 1/\tau$, and it is approximately = 0.1 when $\omega = 10/\tau$. These points are plotted in Figure 9 using straight line approximations. The negative slope is –20 dB/decade or –6 dB/octave. The magnitude curve is plotted as a horizontal line until it intersects the breakpoint where $\omega = 1/\tau$. The negative slope begins at the breakpoint because the magnitude decreases rapidly at that point. The gain is equal to 1 or 0 dB at very low frequencies, equal to 0.707 or –3 dB at the break frequency, and it keeps falling with a –20 dB/decade slope for higher frequencies.

The phase shift for the low pass filter or any other transfer function is calculated with the aid of equation (9).

$$\phi = \text{tangent}^{-1}\left(\frac{1}{\omega\tau}\right) \tag{9}$$

The phase shift is much harder to approximate because the tangent function is nonlinear. Normally the phase information is only required around the 0 dB intercept point for an active circuit, so the calculations are minimized. The phase is shown in Figure 9, and it is approximated by remembering that the tangent of 90° is 1, the tangent of 60° is $\sqrt{3}$, and the tangent of 30° is $\sqrt{3}/3$.

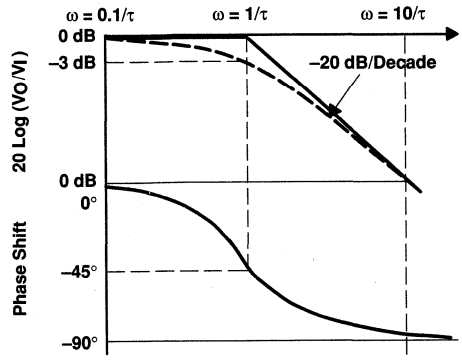

Figure 9. Bode Plot of Low-Pass Filter Transfer Function

A breakpoint occurring in the denominator is called a pole, and it slopes down. Conversely, a breakpoint occurring in the numerator is called a zero, and it slopes up. When the transfer function has multiple poles and zeros, each pole or zero is plotted independently, and the individual poles/zeros are added graphically. If multiple poles, zeros, or a pole/zero combination have the same breakpoint, they are plotted on top of each other. Multiple poles or zeros cause the slope to change by more than 20 dB/decade.

An example of a transfer function with multiple poles and zeros is a band reject filter (see Figure 10). The transfer function of the band reject filter is given in equation (10).

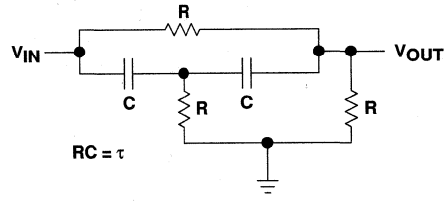

Figure 10. Band Reject Filter

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{(1 + \tau s)(1 + \tau s)}{2\left(1 + \frac{\tau s}{0.44}\right)\left(1 + \frac{\tau s}{4.56}\right)} \qquad (10)$$

The pole zero plot for each individual pole and zero is shown in Figure 11, and the combined pole zero plot is shown in Figure 12.

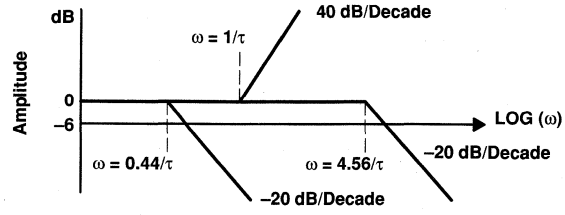

Figure 11. Individual Pole Zero Plot of Band Reject Filter

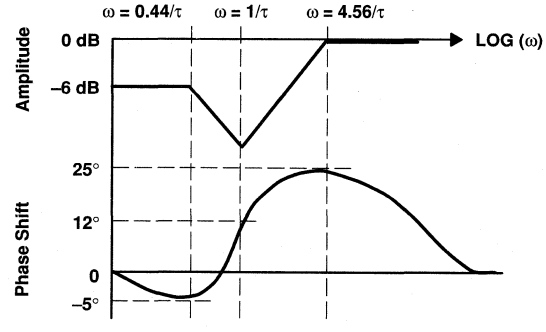

Figure 12. Combined Pole Zero Plot of Band Reject Filter

The individual pole zero plots show the dc gain of 1/2 plotting as a straight line from the –6 dB intercept. The two zeros occur at the same break frequency, thus they have a 40 dB/decade slope. The two poles are plotted at their breakpoints of
$\omega = 0.44/\tau$ and $\omega = 4.56/\tau$. The combined amplitude plot intercepts the axis at –6 dB because of the dc gain, and then breaks down at the first pole. When the amplitude function gets to the double zero, the first zero cancels out the pole, and the second zero breaks up. The upward slope continues until the second pole cancels out the second zero, and the amplitude is flat from that point out in frequency.

When the separation between all the poles and zeros is great, a decade or more in frequency, it is easy to draw the Bode plot. As the poles and zeros get closer the plot gets harder to make. The phase is especially hard to plot because of the tangent function, but picking a few salient points and sketching them in first gets a pretty good approximation.[3] The Bode plot enables the designer to get a good idea of pole zero placement, and it is valuable for fast evaluation of possible compensation techniques. When the situation gets critical, accurate calculations must be made and plotted to get an accurate result.

Consider equation (11).

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \tag{11}$$

Taking the log of equation (11) yields equation (12)

$$20\text{Log}\left(\frac{V_{OUT}}{V_{IN}}\right) = 20\text{Log}(A) - 20\text{Log}(1 + A\beta) \qquad (12)$$

If A and β do not contain any poles or zeros there will be no break points. Then the Bode plot of equation (12) looks like that shown in Figure 13, and because there are no poles to contribute negative phase shift, the circuit cannot oscillate.

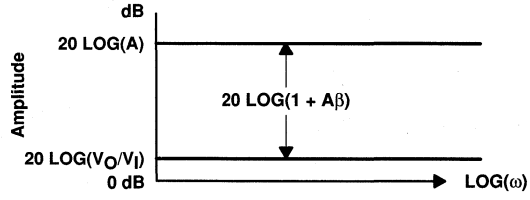

Figure 13. When No Pole Exists in Equation (12)

All real amplifiers have many poles, but they are normally internally compensated so that they appear to have a single pole. Such an amplifier would have an equation similar to that given in equation (13).

$$A = \frac{a}{1 + j\frac{\omega}{\omega_a}} \qquad (13)$$

The plot for the single pole amplifier is shown in Figure 14.

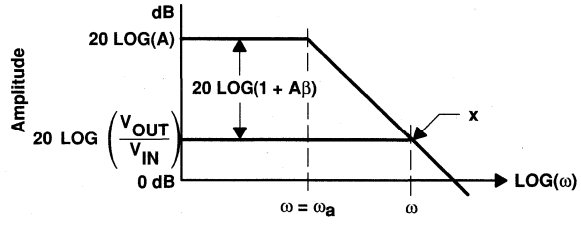

Figure 14. When Equation (12) has a Single Pole

The amplifier gain, A, intercepts the amplitude axis at 20Log(A), and it breaks down at a slope of –20 dB/decade at $\omega = \omega_a$. The negative slope continues for all frequencies greater than the breakpoint, $\omega = \omega_a$. The closed loop circuit gain intercepts the axis at $20\text{Log}(V_{OUT}/V_{IN})$, and because β does not have any poles or zeros, it is constant until its projection intersects the amplifier gain at point X. After intersection with the amplifier gain curve, the closed loop gain follows the amplifier gain because the amplifier becomes the controlling factor.

Actually, the closed loop gain starts to roll off earlier, and it is down 3 dB at point X. At point X the difference between the closed loop gain and the amplifier gain is –3 dB, thus according to equation (12) the term $-20\text{Log}(1+A\beta) = -3$ dB. The magnitude of 3 dB is $\sqrt{2}$, hence $\sqrt{1 + (A\beta)^2} = \sqrt{2}$, and elimination of the radicals shows that $A\beta = 1$. There is a method [4] of relating phase shift and stability to the slope of the closed loop gain curves, but only the Bode method is covered here. An excellent discussion of poles, zeros, and their interaction is given by M. E Van Valkenberg,[5] and he also includes some excellent prose to liven the discussion.

5 Loop Gain Plots are the Key to Understanding Stability

Stability is determined by the loop gain, and when $A\beta = -1 = |1| \angle 180°$ instability or oscillation occurs. If the magnitude of the gain exceeds one, it is usually reduced to one by circuit nonlinearities, so oscillation generally results for situations where the gain magnitude exceeds one.

Consider oscillator design which depends on nonlinearities to decrease the gain magnitude; if the engineer designed for a gain magnitude of one at nominal circuit conditions, the gain magnitude would fall below one under worst case circuit conditions causing oscillation to cease. Thus, the prudent engineer designs for a gain magnitude of one under worst case conditions knowing that the gain magnitude is much more than one under optimistic conditions. The prudent engineer depends on circuit nonlinearities to reduce the gain magnitude to the appropriate value, but this same engineer pays a price of poorer distortion performance. Sometimes a design compromise is reached by putting a nonlinear component, such as a lamp, in the feedback loop to control the gain without introducing distortion.

Some high gain control systems always have a gain magnitude greater than one, but they avoid oscillation by manipulating the phase shift. The amplifier designer who pushes the amplifier for superior frequency performance has to be careful not to let the loop gain phase shift accumulate to 180°. Problems with overshoot and ringing pop up before the loop gain reaches 180° phase shift, thus the amplifier designer must keep a close eye on loop dynamics. Ringing and overshoot are handled in the next section, so preventing oscillation is emphasized in this section. Equation (14) has the form of many loop gain transfer functions or circuits, so it is analyzed in detail.

$$(A)\beta = \frac{(K)}{\left(1 + \tau_1(s)\right)\left(1 + \tau_2(s)\right)} \tag{14}$$

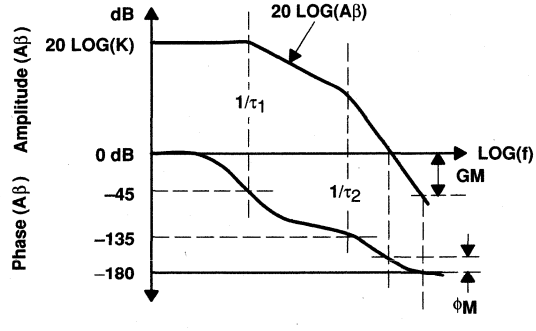

Figure 15. Magnitude and Phase Plot of Equation (14)

The quantity, K, is the dc gain, and it plots as a straight line with an intercept of 20Log(K). The Bode plot of equation (14) is shown in Figure 15. The two break points, $\omega = \omega_1 = 1/\tau_1$ and $\omega = \omega_2 = 1/\tau_2$, are plotted in the Bode plot. Each breakpoint adds –20 dB/decade slope to the plot, and 45° phase shift accumulates at each breakpoint. This transfer function is referred to as a two slope because of the two breakpoints. The slope of the curve when it crosses the 0 dB intercept indicates phase shift and the ability to oscillate. Notice that a one slope can only accumulate 90° phase shift, so when a transfer function passes through 0 dB with a one slope, it cannot oscillate. Furthermore, a two-slope system can accumulate 180° phase shift, therefore a transfer function with a two or greater slope is capable of oscillation.

A one slope crossing the 0 dB intercept is stable, whereas a two or greater slope crossing the 0 dB intercept may be stable or unstable depending upon the accumulated phase shift. Figure 15 defines two stability terms; the phase margin, ϕ_M, and the gain margin, G_M. Of these two terms the phase margin is much more popular because phase shift is critical for stability. Phase margin is a measure of the difference in the actual phase shift and the theoretical 180° required for oscillation, and the phase margin measurement or calculation is made at the 0 dB crossover point. The gain margin is measured or calculated at the 180° phase crossover point. Phase margin is expressed mathematically in equation (15).

$$\phi_M = 180 - \text{tangent}^{-1}(A\beta) \qquad (15)$$

The phase margin in Figure 15 is very small, 20°, so it is hard to measure or predict from the Bode plot. A designer probably doesn't want a 20° phase margin because the system overshoots and rings badly, but this case points out the need to calculate small phase margins carefully. The circuit is stable, and it does not oscillate because the phase margin is positive. Also, the circuit with the smallest phase margin has the highest frequency response and bandwidth.

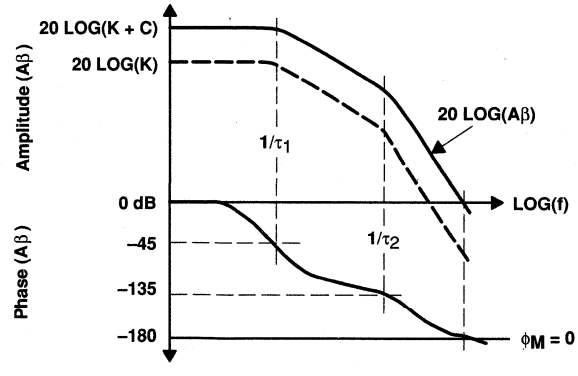

Figure 16. Magnitude and Phase Plot of the Loop Gain Increased to (K+C)

Increasing the loop gain to (K+C) as shown in Figure 16 shifts the magnitude plot up. If the pole locations are kept constant, the phase margin reduces to zero as shown, and the circuit will oscillate. The circuit is not good for much in this condition because production tolerances and worst case conditions insure that the circuit will oscillate when you want it to amplify, and vice versa.

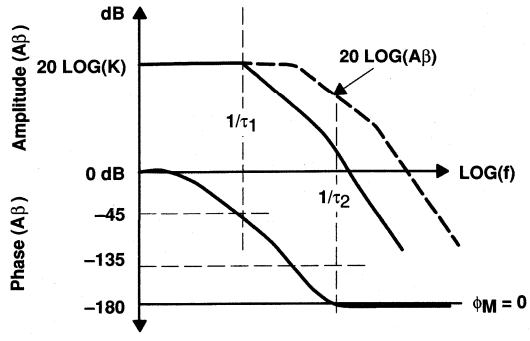

Figure 17. Magnitude and Phase Plot of the Loop Gain With Pole Spacing Reduced

The circuit poles are spaced closer in Figure 17, and this results in a faster accumulation of phase shift. The phase margin is zero because the loop gain phase shift reaches 180° before the magnitude passes through 0 dB. This circuit oscillates, but it is not a very stable oscillator because the transition to 180° phase shift is very slow. Stable oscillators have a very sharp transition through 180°.

When the closed loop gain is increased the feedback factor, β, is decreased because $V_{OUT}/V_{IN} = 1/\beta$ for the ideal case. This in turn decreases the loop gain, Aβ, thus the stability increases. In other words, increasing the closed loop gain makes the circuit more stable. Stability is not important except to oscillator designers because overshoot and ringing become intolerable to linear amplifiers long before oscillation occurs. The overshoot and ringing situation is investigated in the next section.

6 The Second Order Equation and Ringing/Overshoot Predictions

The second order equation is a common approximation used for feedback system analysis because it describes a two-pole circuit which is the most common approximation used. All real circuits are more complex than two poles, but except for a small fraction, they can be represented by a two-pole equivalent. The second order equation is extensively described in electronic and control literature[6].

$$(1 + A\beta) = 1 + \frac{K}{(1 + \tau_1 s)(1 + \tau_2 s)} \tag{16}$$

After algebraic manipulation equation (16) is presented in the form of equation (17).

$$s^2 + \frac{\tau_1 + \tau_2}{\tau_1 \tau_2} + \frac{1 + K}{\tau_1 \tau_2} = 0 \tag{17}$$

Equation (17) is compared to the second order control equation (18), and the damping ratio, z, and natural frequency, w_N are obtained through like term comparisons.

$$s^2 + 2\xi\omega_N s + \omega_N^2 \tag{18}$$

Comparing these equations yields formulas for the phase margin and per cent overshoot as a function of damping ratio.

$$\omega_N = \sqrt{\frac{1 + K}{\tau_1 \tau_2}} \tag{19}$$

$$\xi = \frac{\tau_1 + \tau_2}{2\omega_N \tau_1 \tau_2} \tag{20}$$

When the two poles are well separated, equation (21) is valid.

$$\phi_M = \text{tangent}^{-1}(2\xi) \tag{21}$$

The salient equations are plotted in Figure 18 which enables a designer to determine the phase margin and overshoot when the gain and pole locations are known.

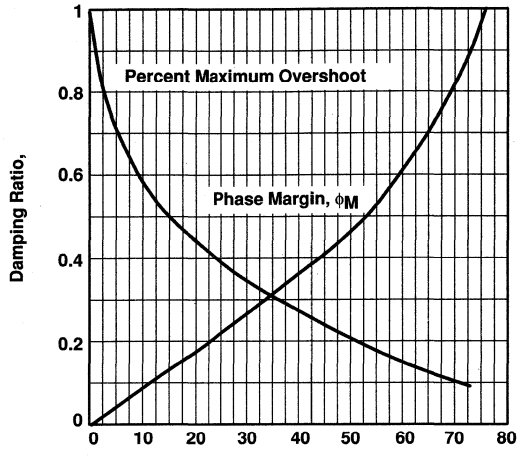

Figure 18. Phase Margin and Overshoot vs Damping Ratio

Enter Figure 18 at the calculated damping ratio, say 0.4, and read the overshoot at 25% and the phase margin at 42°. If a designer had a circuit specification of 5% maximum overshoot, then the damping ratio must be 0.78 with a phase margin of 62°.

7 Summary

These equations and examples are adequate to get designers started in the design and analysis of feedback circuits. When the engineers reach the point where the examples and equations given here are inadequate, they must go to the references for more information. If the engineers find themselves digging through the references on a regular basis, they should consider becoming analog design engineers.

8 References

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Gain Block Analysis for the THS3001

James Karki

Literature Number: SLOA019
March 1999

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Contents

List of Figures

Gain Block Analysis for the THS3001

James Karki

ABSTRACT

This report describes how to construct a gain block diagram for a current feedback op amp and relates the diagram to stability and gain analysis using parameters of the THS3001 op amp.

1 Introduction

The application report *Voltage Feedback vs Current Feedback Op Amps,* SLVA051, outlines the operation of a current feedback op amp in relation to a voltage feedback op amp. The basic difference between a current feedback op amp and a voltage feedback op amp is that its transfer function is a transimpedance equal to the output voltage divided by the input current at the negative input, i.e., $Zt = \frac{Vo}{Ie}$.

When constructing a gain block diagram, this basic difference in operation changes the mathematical functions represented by the gain blocks. By using the same methods that are used to construct a gain block diagram for a voltage feedback op amp, a gain block diagram can also be constructed for a current feedback op amp. Once constructed, the gain block diagram can be manipulated using standard techniques.

2 Gain Block Diagram Basics

Figure 1 shows a basic current feedback op amp model configured as a noninverting amplifier by using feedback resistor *R2* and gain setting resistor *R1*.

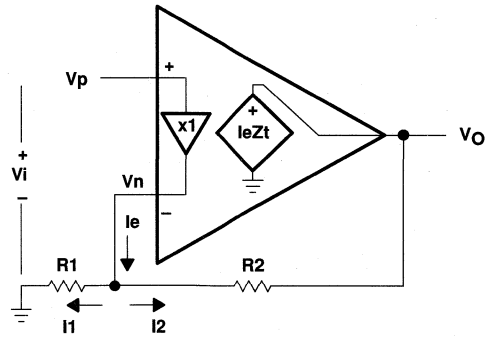

Figure 1. Noninverting Amplifier Using Current Feedback Model

Referring to Figure 1:

By observation, $Vo = IeZt$ and $Vn = Vp = Vi$. Summing the currents at node Vn: $Ie = I1 + I2$. Substituting and rearranging:

$$Ie = Vi\left(\frac{1}{R1} + \frac{1}{R2}\right) - Vo\left(\frac{1}{R2}\right) = (Vi \times c) - (Vo \times b) \text{ where } c = \left(\frac{1}{R1} + \frac{1}{R2}\right) \text{ and}$$

$b = \left(\frac{1}{R2}\right)$. Using these mathematical relationships, the block diagram shown in Figure 2 is constructed. Refer to Appendix A for the gain block diagram for an inverting amplifier.

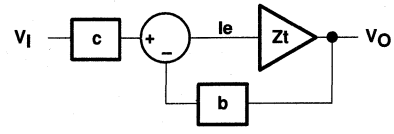

Figure 2. Block Diagram

2.1 Gain Analysis

Using the block diagram, the transfer function for the amplifier circuit is computed by:

$$\frac{Vo}{Vi} = \frac{c}{b}\left[\frac{1}{1+\frac{1}{Zt \times b}}\right] \text{ substituting for c and b, } \frac{Vo}{Vi} = \left(1+\frac{R1}{R2}\right)\left[\frac{1}{1+\frac{R2}{Zt}}\right]$$

The above equation describes a transfer function where the gain is equal to $\frac{c}{b}$ as long as $Zt \times b >> 1$. The frequency at which $|Zt \times b| = 1$ determines the bandwidth.

2.2 Stability Analysis

The loop transmission, $T = Zt \times b$, is used for stability analysis. $\angle T$ at the frequency where $|T| = 1$ determines the stability of the circuit.

Normally it is desired to have $\angle T \leq -115°$ when $|T| = 1$.

3 Application to THS3001

Figure 3 is a plot of the THS3001's open loop transimpedance magnitude and phase vs frequency. The magnitude plot is in dB ohms[1]. Assuming a purely resistive feedback network, plotting a horizontal line that intersects $|Zt|$ where the $\angle Zt$ is approximately −115°, determines the value of $\frac{1}{b}$ required for a phase margin of 65°. Doing this results in $\frac{1}{b} \approx 60$ *dB ohms*. Using $b = \frac{1}{R2}$ and converting to ohms, results in the minimum value of R2 = 1 kΩ for a phase margin of 65°. R2 = 1 kΩ is the value recommended in the data sheet for the feedback resistor when using the THS3001 as a unity gain amplifier. Values greater than 1 kΩ reduce the bandwidth and increase stability. Reference the THS3001 data sheet, literature number SLOS217.

[1] $dB\ ohms = 20log_{10}\left(\frac{V}{1} \times \frac{1}{1\Omega}\right)$

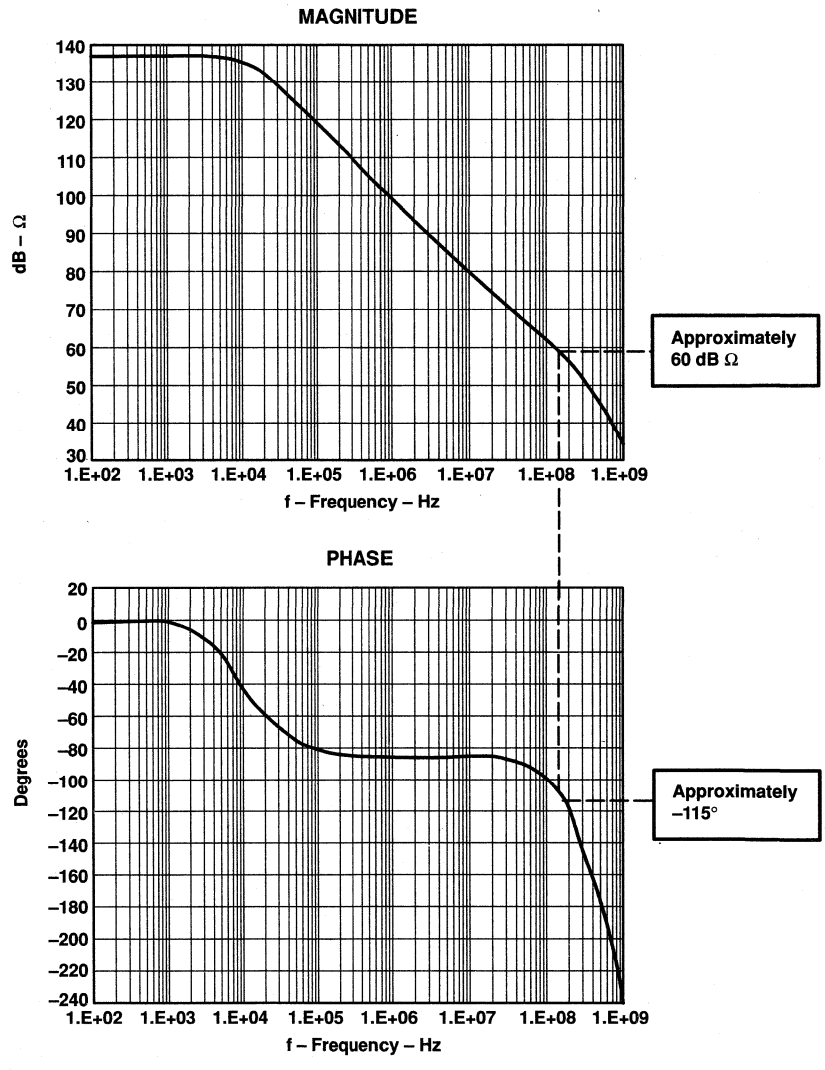

Figure 3. THS3001 Open Loop Transimpedance

Using feedback components that reduce the impedance or that cause additional phase shift in the feedback path will erode the phase margin, and possibly lead to unstable operation. This is why using capacitance in the feedback path is not recommended and why parasitic capacitance at the negative input must be minimized when using the THS3001.

In the discussion above it is assumed that the widest possible bandwidth is desired. This may not be the case. The resistance of R2 can be chosen to set the bandwidth to whatever is desired. Simply convert $|Zt|$ (in dB ohms) at the bandwidth desired into ohms, and use this value for R2.

Example: set bandwidth to 10 MHz.

Solution: $|Zt|$ =80 dB ohms at 10 MHz, therefore $R2 = 10^{\left(\frac{80}{20}\right)} \times \frac{1\Omega}{1} = 10\,k\Omega$.

As would be expected, variations in Zt, second order effects due to the finite output and input impedances that are not included here, and parasitic elements are more influential at higher frequencies. All these things combine so that the above calculation serves as a good approximation or starting point, but the intended circuit needs to be built and tested to confirm the desired frequency response given a specific configuration.

4 Summary

Gain block diagrams are widely used to simplify gain and stability analysis in voltage feedback op amp circuits. By analyzing the circuit so that the mathematical relationships between the nodes are found, the gain block diagram is constructed for a current feedback op amp. With the gain block diagram in place, the wealth of information available on manipulating such diagrams can be tapped and used to advantage without regard to the source circuit.

The gain block diagram developed here and the transfer function data provides the basic tools for gain and stability analysis of circuits using the THS3001.

Appendix A shows how to develop a gain block diagram for an inverting current feedback amplifier. The techniques can be applied to other circuits as well to develop the required diagram for analysis.

Appendix A Gain Block Diagram for Inverting Current Feedback Amplifier

A.1 Introduction

Figure A–1 (a) shows the circuit model for an inverting current feedback amplifier. By observation, $Vo = IeZt$ and $Vn = Vp = 0$. Summing the currents at Vn: $Ie = I1 + I2$. Substituting and rearranging:

$Ie = -Vi\left(\frac{1}{R1}\right) - Vo\left(\frac{1}{R2}\right) = (Vi \times c) - (Vo \times b)$ where $c = -\left(\frac{1}{R1}\right)$ and $b = -\left(\frac{1}{R2}\right)$.

Using these relationships, the block diagram shown in Figure A–1 (b) can be drawn.

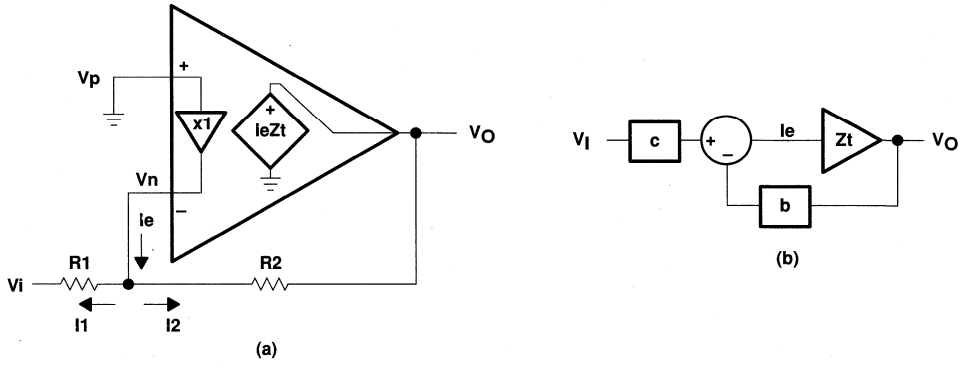

Figure A–1. (a) Inverting Current Feedback Amplifier, (b) Gain Block Diagram

A.2 Gain Analysis

Using the block diagram, the transfer function for the amplifier circuit is computed by: $\frac{Vo}{Vi} = \frac{c}{b}\left[\frac{1}{1 + \frac{1}{Zt \times b}}\right]$ substituting for c and b, $\frac{Vo}{Vi} = -\left(\frac{R1}{R2}\right)\left[\frac{1}{1 + \frac{R2}{Zt}}\right]$

This equation describes a transfer function where the gain is equal to $\frac{c}{b}$ as long as $Zt \times b >> 1$. The frequency at which $|Zt \times b| = 1$ determines the bandwidth.

A.3 Stability Analysis

The loop transmission, $T = Zt \times b$, is used for stability analysis. $\angle T$ at the frequency where $|T| = 1$ determines the stability of the circuit. As $\angle T$ approaches −180° when $|T| = 1$, the circuit becomes unstable.

Noise Analysis in Operational Amplifier Circuits

Literature Number: SLOA019
March 1999

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Contents

List of Figures

List of Tables

Noise Analysis in Operational Amplifier Circuits

ABSTRACT

This application report uses standard circuit theory and noise models to calculate noise in op amp circuits. Example analysis of the inverting, noninverting, and differential-amplifier circuits shows how calculations are performed. Characteristics of noise sources are presented to help the designer make informed decisions when designing for noise.

Introduction

"Statistical fluctuation of electric charge exists in all conductors, producing random variation of potential between the ends of the conductor. The electric charges in a conductor are found to be in a state of thermal agitation, in thermodynamic equilibrium with the heat motion of the atoms of the conductor. The manifestation of the phenomenon is a fluctuation of potential difference between the terminals of the conductor" – J.B. Johnson[1]

"The term spontaneous fluctuations, although, perhaps, theoretically the most appropriate, is not commonly used in practice; usually it is simply called noise" – Aldert van der Ziel[2]

Early investigators of noise likened spontaneous fluctuations of current and voltage in electric circuits to Brownian motion. In 1928 Johnson[1] showed that electrical noise was a significant problem for electrical engineers designing sensitive amplifiers. The limit to the sensitivity of an electrical circuit is set by the point at which the signal-to-noise ratio drops below acceptable limits.

Notational Conventions

In the calculations throughout this report, lower case letters *e* and *i* indicate independent voltage and current noise sources; upper case letters *E* and *I* indicate combinations or amplified versions of the independent sources.

Spectral Density

A spectral density is a noise voltage or noise current per root hertz, i.e. $V/\sqrt{Hz}$ or $A/\sqrt{Hz}$. Spectral densities are commonly used to specify noise parameters. The characteristic equations that identify noise sources are always integrated over frequency, indicating that spectral density is the natural form for expressing noise sources. To avoid confusion in the following analyses, spectral densities are identified, when used, by stating them as volts or amps per root hertz.

Types of Noise

In electrical circuits there are 5 common noise sources:

- Shot noise
- Thermal noise
- Flicker noise
- Burst noise
- Avalanche noise

In op amp circuits, burst noise and avalanche noise are normally not problems, or they can be eliminated if present. They are mentioned here for completeness, but are not considered in the noise analysis.

Shot Noise

Shot noise is always associated with current flow. Shot noise results whenever charges cross a potential barrier, like a pn junction. Crossing the potential barrier is a purely random event. Thus the instantaneous current, i, is composed of a large number of random, independent current pulses with an average value, i_D. Shot noise is generally specified in terms of its mean-square variation about the average value. This is written as $\overline{i_n^2}$, where :

$$\overline{i_n^2} = \overline{(i - i_D)^2} = \int 2qi_D df \tag{1}$$

Where q is the electron charge (1.62×10^{-19} C) and df is differential frequency.

Shot noise is spectrally flat or has a uniform power density, meaning that when plotted versus frequency, it has a constant value. Shot noise is independent of temperature.

The term qi_D is a current power density having units A^2/Hz.

Thermal Noise

Thermal noise is caused by the thermal agitation of charge carriers (electrons or holes) in a conductor. This noise is present in all passive resistive elements.

Like shot noise, thermal noise is spectrally flat or has a uniform power density, but thermal noise is independent of current flow.

Thermal noise in a conductor can be modeled as voltage or current. When modeled as a voltage it is placed in series with an otherwise noiseless resistor. When modeled as a current it is placed in parallel with an otherwise noiseless resistor. The average mean-square value of the voltage noise source or current noise source is calculated by:

$$\overline{e^2} = \int 4kTRdf \text{ or } \overline{i^2} = \int (4kT / R)df \tag{2}$$

Where k is Boltzmann's constant (1.38×10^{-23} j/K), T is absolute temperature in Kelvin (K), R is the resistance of the conductor in ohms (Ω) and df is differential frequency.

The terms *4kTR* and *4kT/R* are voltage and current power densities having units of V^2/Hz and A^2/Hz.

Flicker Noise

Flicker noise is also called *1/f* noise. It is present in all active devices and has various origins. Flicker noise is always associated with a dc current, and its average mean-square value is of the form:

$$\overline{e^2} = \int \left(K_e^2 / f \right) df \text{ or } \overline{i^2} = \int \left(K_i^2 / f \right) df \qquad (3)$$

Where K_e and K_i are the appropriate device constants (in volts or amps), f is frequency, and df is differential frequency.

Flicker noise is also found in carbon composition resistors where it is often referred to as excess noise because it appears in addition to the thermal noise. Other types of resistors also exhibit flicker noise to varying degrees, with wire wound showing the least. Since flicker noise is proportional to the dc current in the device, if the current is kept low enough, thermal noise will predominate and the type of resistor used will not change the noise in the circuit.

The terms K_e^2/f and K_i^2/f are voltage and current power densities having units of V^2/Hz and A^2/Hz.

Burst Noise

Burst noise, also called popcorn noise, appears to be related to imperfections in semiconductor material and heavy ion implants. Burst noise makes a popping sound at rates below 100 Hz when played through a speaker. Low burst noise is achieved by using clean device processing.

Avalanche Noise

Avalanche noise is created when a pn junction is operated in the reverse breakdown mode. Under the influence of a strong reverse electric field within the junction's depletion region, electrons have enough kinetic energy that, when they collide with the atoms of the crystal lattice, additional electron-hole pairs are formed. These collisions are purely random and produce random current pulses similar to shot noise, but much more intense.

Noise Characteristics

Since noise sources have amplitudes that vary randomly with time, they can only be specified by a probability density function. Thermal noise and shot noise have Gaussian probability density functions. The other forms of noise noted do not. If δ is the standard deviation of the Gaussian distribution, then the instantaneous value lies between the average value of the signal and $\pm\delta$ 68% of the time. By definition, δ^2 (variance) is the average mean-square variation about the average value. This means that in noise signals having Gaussian distributions of amplitude, the average mean-square variation about the average value, $\overline{i^2}$ or $\overline{e^2}$, is the variance δ^2, and the rms value is the standard deviation δ.

Theoretically the noise amplitude can have values approaching infinity. However, the probability falls off rapidly as amplitude increases. An effective limit is $\pm 3\delta$, since the noise amplitude is within these limits 99.7% of the time. Figure 1 shows graphically how the probability of the amplitude relates to the rms value.

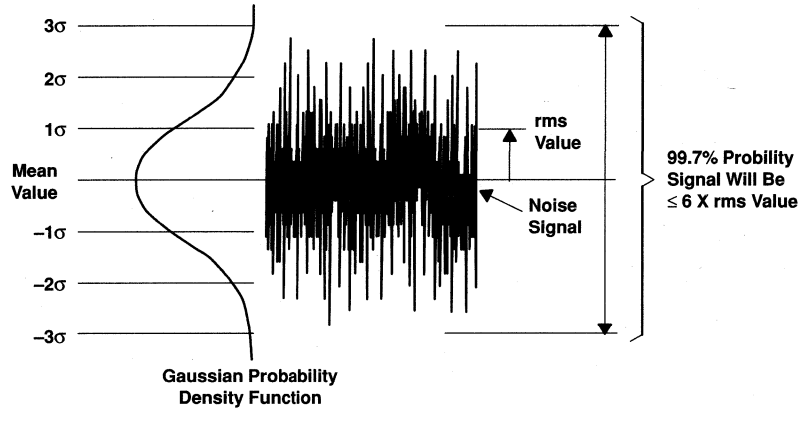


Figure 1. Gaussian Distribution of Noise Amplitude

Since the rms value of a noise source is equal to δ, to assure that a signal is within peak-to-peak limits 99.7% of the time, multiply the rms value by 6(+3δ–(–3δ)): *Erms* × *6* = *Epp*. For more or less assurance, use values between 4(95.4%) and 6.8(99.94%).

Adding Noise Sources

With multiple noise sources in a circuit, the signals must be combined properly to obtain the overall noise signal.

Consider the example of two resistors, R_1 and R_2, connected in series. Each resistor has a noise generator associated with it as shown in Figure 2 where

$$\overline{e_1^2} = \int 4kTR_1 df \quad \text{and} \quad \overline{e_2^2} = \int 4kTR_2 df .$$

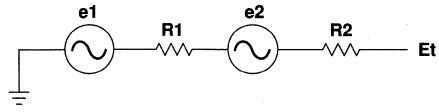


Figure 2. R1 and R2 Noise Model

To calculate the average mean square voltage, $\overline{E_t^2}$, across the two resistors, let $E_t(t) = e_1(t) + e_2(t)$ be the instantaneous values. Then

$$\overline{E_t(t)^2} = \overline{\left[e_1(t) + e_2(t)\right]^2} = \overline{e_1(t)^2} + \overline{e_2(t)^2} + \overline{2e_1(t)e_2(t)} \tag{4}$$

Since the noise voltages, $e_1(t)$ and $e_2(t)$, arise from separate resistors, they are independent, and the average of their product is zero:

$$\overline{2e_1(t)e_2(t)} = 0 \tag{5}$$

This results in

$$\overline{E_t^2} = \overline{e_1^2} + \overline{e_2^2}. \tag{6}$$

Therefore, as long as the noise sources arise from separate mechanisms and are independent, which is usually the case, the average mean square value of a sum of separate independent noise sources is the sum of the individual average mean square values. Thus in our example $\overline{E_t^2} = \int 4kT(R_1 + R_2)df$, which is what would be expected. This is derived using voltage sources, but also is true for current sources. The same result can be shown to be true when considering two independent sine wave sources.

Noise Spectra

A pure sine wave has power at only one frequency. Noise power, on the other hand, is spread over the frequency spectrum. Voltage noise power density, $\overline{e^2}/Hz$, and current noise power density, $\overline{i^2}/Hz$ are often used in noise calculations. To calculate the mean-square value, the power density is integrated over the frequency of operation. This application report deals with noise that is constant over frequency, and noise that is proportional to 1/f.

Spectrally flat noise is referred to as white noise. When plotted vs frequency, white noise is a horizontal line of constant value.

Flicker noise is 1/f noise and is stated in equation form as:

$$\overline{e^2} = \int \left(K_e^2/f\right) df \quad or \quad \overline{i^2} = \int \left(K_i^2/f\right) df$$

See equation (3). When plotted vs frequency on log-log scales, 1/f noise is a line with constant slope. If the power density V^2/Hz is plotted, the slope is –1 decade per decade. If the square root of the power density, $V_{rms}/\sqrt{Hz}$, is plotted, the slope is –0.5 decade per decade.

Figure 3 shows the spectra of 1/f and white noise per root hertz.

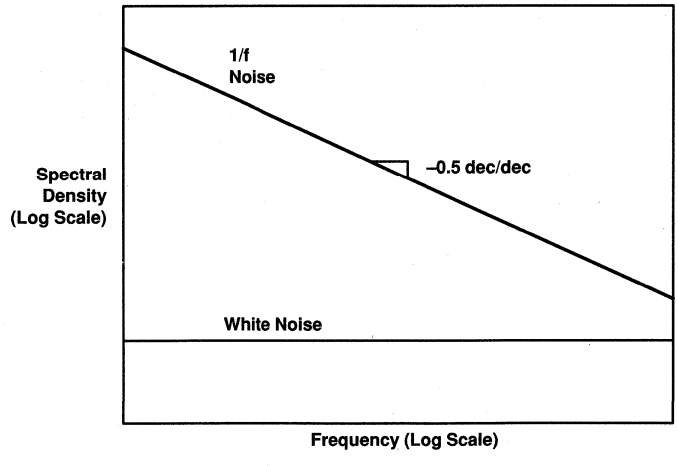


Figure 3. 1/f and White Noise Spectra

Integrating Noise

To determine the noise or current voltage over a given frequency band, the beginning and ending frequencies are used as the *f* integration limits and the integral evaluated. The following analysis uses voltages; the same is true for currents.

Given a white or constant voltage noise versus frequency source then:

$$\overline{e^2} = \int_{f_L}^{f_H} C\ df = C\left(f_H - f_L\right) \tag{7}$$

where $\overline{e^2}$ is the average mean-square voltage, C is the spectral power density per hertz (constant), f_L is the lowest frequency, and f_H is the highest frequency.

Given a 1/f voltage noise versus frequency source then:

$$\overline{e^2} = \int_{f_L}^{f_H} \frac{K^2}{f}\ df = K^2\ ln\ \frac{f_H}{f_L} \tag{8}$$

where $\overline{e^2}$ is the average mean-square voltage, K is the appropriate device constant in volts, f_L is the lowest frequency, and f_H is the highest frequency.

The input noise of an op amp contains both 1/f noise and white noise. The point in the frequency spectrum where 1/f noise and white noise are equal is referred to as the noise corner frequency, f_{nc}. Using the same notation as in the equations above, this means that $K^2/fnc = C$. It is useful to find f_{nc} because the total average mean-square noise can be calculated by adding equations (7) and (8) and substituting Cf_{nc} for K^2:

$$\overline{E^2} = C\left(f_{nc}\ ln\ \frac{f_H}{f_L} + f_H - f_L\right) \tag{9}$$

Where C is the square of the white noise voltage specification for the op amp.

Figure 4 shows the equivalent input noise voltage vs frequency graph for the TLV2772 as normally displayed in the data sheet.

f_{nc} can be determined visually from the graph of equivalent input noise per root hertz vs. frequency graph that is included in most op amp data sheets. Since at f_{nc} the white noise and 1/f noise are equal, f_{nc} is the frequency at which the noise is $\sqrt{2}$ x white noise specification. This would be about $17\ nV/\sqrt{Hz}$ for the TLV2772, which is at 1000 Hz as shown in Figure 4.

Another way to find f_{nc}, is to determine K^2 by finding the equivalent input noise voltage per root hertz at the lowest possible frequency in the 1/f noise region, square this value, subtract the white noise voltage squared, and multiply by the frequency. Then divide K^2 by the white noise specification squared. The answer is f_{nc}.

For example, the TLV2772 has a typical noise voltage of $130\ nV/\sqrt{Hz}$ at 10 Hz.

The typical white noise specification for the TLV2772 is 12 $nV/\sqrt{Hz}$

$$K^2 = \left[\left(130\ nV/\sqrt{Hz}\right)^2 - \left(12\ nV/\sqrt{Hz}\right)^2\right] \times (10\ Hz) = 167560\ (nV)^2$$

Therefore, f_{nc} = (167560(nV)^2)/(144(nV)^2/Hz) = 1163 Hz

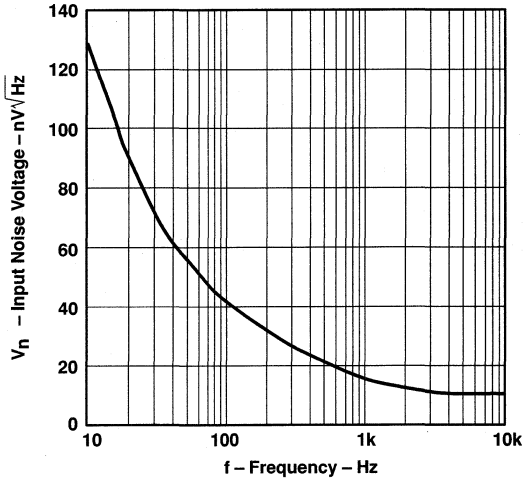


Figure 4. Equivalent Input Noise Voltage vs Frequency for TLV2772 as Normally Presented

Figure 5 was constructed by interpreting the equivalent input noise voltage versus frequency graph for the TLV2772 and plotting the values on log-log scales. The –0.5 dec/dec straight line nature of 1/f noise when plotted on log-log scales can be seen.

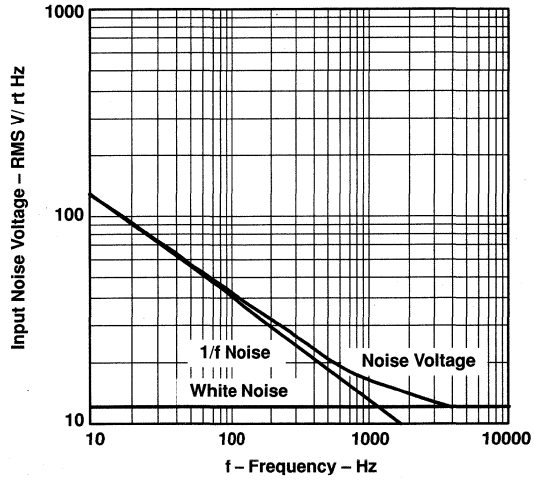


Figure 5. Equivalent Input Noise Voltage vs Frequency for TLV2772 on Log-Log Scale

Equivalent Noise Bandwidth

Equations (7), (8), and (9) are only true if the bandwidth If the op amp circuit is brick-wall. In reality there is always a certain amount of out-of-band energy transferred. The equivalent noise bandwidth (ENB) is used to account for the extra noise so that brick-wall frequency limits can be used in equations (7), (8), and (9). Figure 6 shows the idea for a first order low-pass filter.

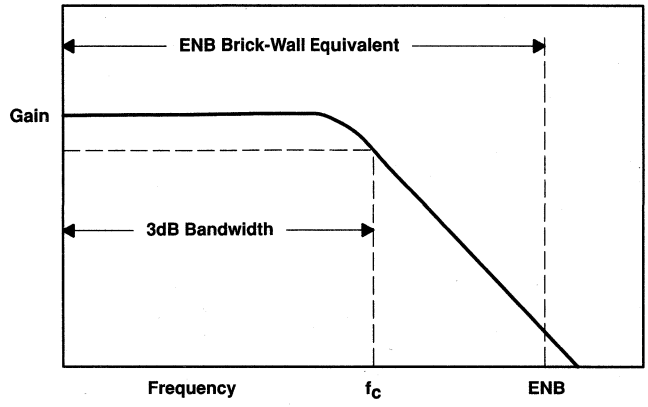


Figure 6. ENB Brick-Wall Equivalent

Figure 7 shows an example of a simple RC filter used to filter a voltage noise source, e_{in}.

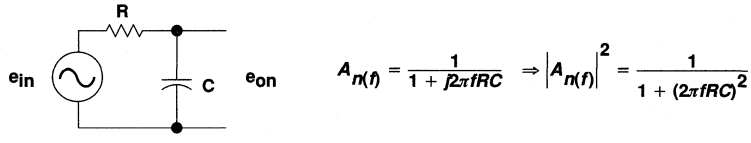


Figure 7. RC Filter

$A_{n(f)}$ is the frequency-dependant gain of the circuit, and e_{on} is calculated:

$$e_{on} = \sqrt{\int_0^\infty |A_{n(f)}|^2 \, e_{in}^2 \, df} \tag{10}$$

Assuming e_{in} is a white noise source (specified as a spectral density in $V/\sqrt{Hz}$), using radian measure for frequency, and substituting for $A_{n(f)}$, the equation can be solved as follows:

(11)

$$e_{on} = e_{in} \sqrt{\int_0^\infty \frac{1}{1 + (2\pi fRC)^2} df} = e_{in} \sqrt{\frac{1}{2\pi RC} \Big|_0^\infty \tan^{-1} 2\pi fRC} = e_{in} \sqrt{\frac{1}{2\pi RC} \frac{\Pi}{2}}$$

So that the ENB = 1.57 x 3dB bandwidth in this first-order system. This result holds for any first-order low-pass function. For higher order filters the ENB approaches the normal cutoff frequency, f_c, of the filter. Table 1 shows the ENB for different order low-pass filters.

Table 1. ENB vs Filter Order for Low-Pass Filters

FILTER ORDER	ENB
1	1.57 x f_c
2	1.11 x f_c
3	1.05 x f_c
4	1.025 x f_c

Resistor Noise Model

To reiterate, noise in a resistor can be modeled as a voltage source in series, or as a current source in parallel, with an otherwise noiseless resistor as shown in Figure 8. These models are equivalent and can be interchanged as required to ease analysis. This is explored in Appendix A.

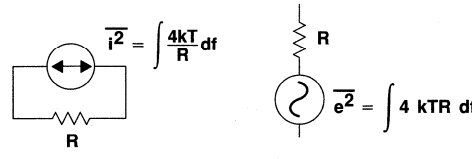


Figure 8. Resistor Noise Models

Op Amp Circuit Noise Model

Op amp manufacturers measure the noise characteristics for a large sampling of a device. This information is compiled and used to determine the typical noise performance of the device. The noise specifications published by Texas Instruments in their data sheets refer the measured noise to the input of the op amp. The part of the internally generated noise that can properly be represented by a voltage source is placed in series with the positive input to an otherwise noiseless op amp. The part of the internally generated noise that can properly be represented by current sources is placed between each input and ground in an otherwise noiseless op amp. Figure 9 shows the resulting noise model for a typical op amp.

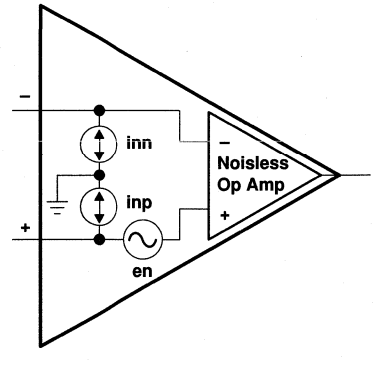


Figure 9. Op Amp Noise Model

Inverting and Noninverting Op Amp Circuit Noise Calculations

To perform a noise analysis, the foregoing noise models are added to the circuit schematic and the input signal sources are shorted to ground. When this is done to either an inverting or a noninverting op amp circuit, the same circuit results, as shown in Figure 10. This circuit is used for the following noise analysis.

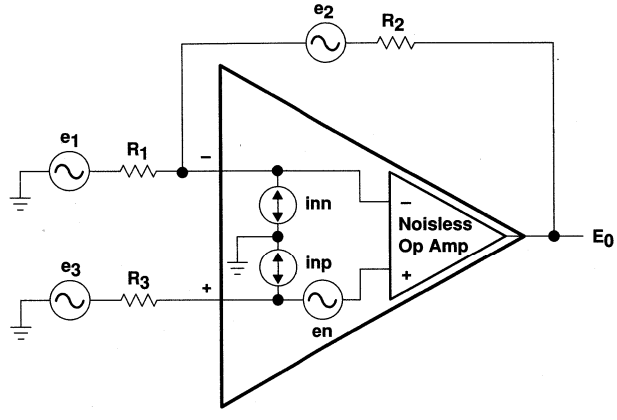
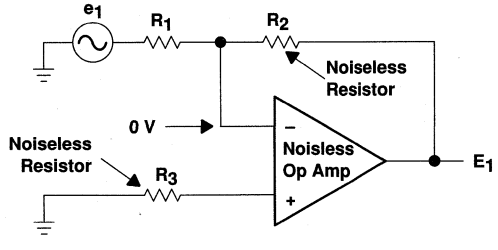


Figure 10. Inverting and Noninverting Noise Analysis Circuit

At first, this analysis may appear somewhat daunting, but it can be deciphered piece by piece. Using the principles of superposition, each of the noise sources is isolated, and everything else is assumed to be noiseless. Then the results can be added according to the rules for adding independent noise sources. An ideal op amp is assumed for the noiseless op amp. In the end it will all seem simple, if a little tedious the first time through.

Figures 11 through 13 show the analysis.

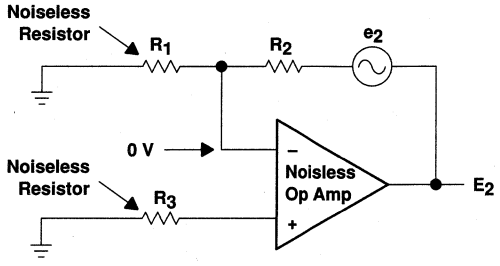


$$\overline{E_1} = \overline{e_1}\,\frac{R_2}{R_1}$$

$$\overline{E_1}^2 = \overline{e_1}^2\left(\frac{R_2}{R_1}\right)^2$$

$$\overline{e_1}^2 = \int 4kTR_1\,df$$

Figure 11. E1

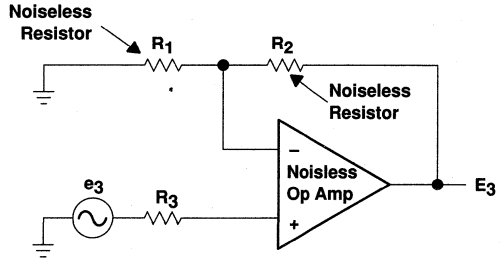


$$\overline{E_2} = \overline{e_2}$$

$$\overline{E_2}^2 = \overline{e_2}^2$$

$$\overline{e_2}^2 = \int 4kTR_2 \, df$$

Figure 12. E2



$$\overline{E_3} = \overline{e_3}\left(\frac{R_1 + R_2}{R_1}\right)$$

$$\overline{E_2}^2 = \overline{e_2}^2\left(\frac{R_1 + R_2}{R_1}\right)^2$$

$$\overline{e_3}^2 = \int 4kTR_3 \, df$$

Figure 13. E3

Combining to arrive at the solution for the circuit's output rms noise voltage, E_{Rrms}, due to the thermal noise of the resistors in the circuit:

(12)

$$E_{Rrms} = \sqrt{\overline{E_1}^2 + \overline{E_2}^2 + \overline{E_3}^2}$$

$$E_{Rrms} = \sqrt{\int \left[4kTR_1\left(\frac{R_2}{R_1}\right)^2 + 4kTR_2 + 4kTR_3\left(\frac{R_1 + R_2}{R_1}\right)^2\right] df}$$

$$E_{Rrms} = \sqrt{\int \left[4kTR_2\left(\frac{R_1 + R_2}{R_1}\right) + 4kTR_3\left(\frac{R_1 + R_2}{R_1}\right)^2\right] df}$$

If it is desired to know the resistor noise referenced to the input, E_{iRrms}, the output noise is divided by the noise gain, A_n, of the circuit:

$$A_n = \left(\frac{R_1 + R_2}{R_1}\right) \tag{13}$$

(14)

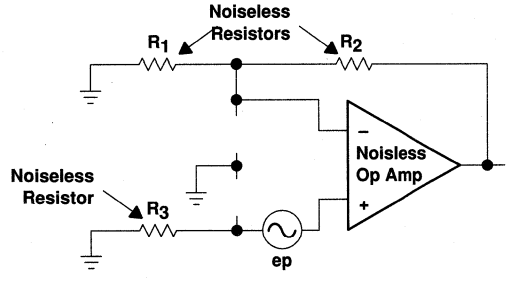
$$E_{iRrms}^2 = \left(\frac{E_{Rrms}}{A_n}\right)^2 = \int \frac{\left[4kTR_2\left(\frac{R_1+R_2}{R_1}\right) + 4kTR_3\left(\frac{R_1+R_2}{R_1}\right)^2\right]df}{\left(\frac{R_1+R_2}{R1}\right)^2} = \int 4kT\left[\left(\frac{R_1R_2}{R_1+R_2}\right) + R_3\right]df$$

Normally R_3 is chosen to be equal to the parallel combination of R_1 and R_2 to minimize offset voltages due to input bias current. If this is done, the equation simplifies to:

(15)

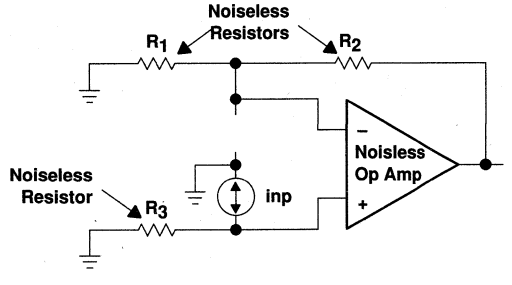
$$E_{iRrms} = \sqrt{\int 8kTR_3\ df} \qquad When\ R3 = \left(\frac{R_1R_2}{R_1+R_2}\right)$$

Now consider the noise sources associated with the op amp itself. The analysis proceeds as before as shown in Figures 14 through 16.



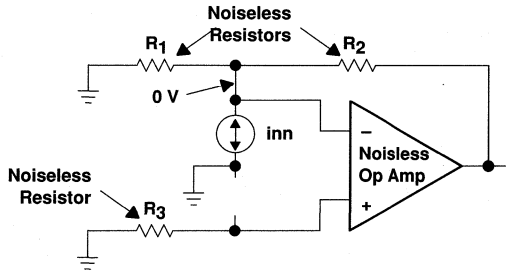
$$\overline{E_p^2} = \int\left[(e_p)\left(\frac{R_1+R_2}{R_1}\right)\right]^2 df$$

Figure 14. E_p



$$\overline{E_{np}^2} = \int\left[(i_{np})(R_3)\left(\frac{R_1+R_2}{R_1}\right)\right]^2 df$$

Figure 15. E_{np}



$$\overline{E_{nn}^2} = \int \left[(i_{nn})(R_2) \right]^2 df$$

Figure 16. E_{nn}

Combining to arrive at the solution for the circuit's output rms noise voltage, E_{oarms}, due to the input referred op amp noise in the circuit:

(16)

$$E_{oarms} = \sqrt{\overline{E_p}^2 + \overline{E_{np}}^2 + \overline{E_{nn}}^2}$$

$$E_{oarms} = \sqrt{\int \left[\left(i_{nn}(R_2)\right)^2 + \left((i_{np}) R_3 \left(\frac{R_1 + R_2}{R_1} \right) \right)^2 + \left(e_p \left(\frac{R_1 + R_2}{R_1} \right) \right)^2 \right] df}$$

Now combining the resistor noise and the op amp noise to get the total output rms noise voltage, E_{Trms}.

(17)

$$E_{Trms} = \sqrt{\int \left[4kTR_2 \left(\frac{R_1 + R_2}{R_1} \right) + 4kTR_3 \left(\frac{R_1 + R_2}{R_1} \right)^2 + \left((i_{np}) R_2 \right)^2 + \left((i_{np}) R_3 \left(\frac{R_1 + R_2}{R_1} \right) \right)^2 + \left(e_n \left(\frac{R_1 + R_2}{R_1} \right) \right)^2 \right] df}$$

The only work left is to evaluate the integral. Most of the terms are constants that can be brought straight out of the integral. The resistors and their associated noise are constant over frequency so that the first two terms are constants. The last three terms contain the input referred noise of the op amp. The voltage and current input referred noise of op amps contains flicker noise, shot noise, and thermal noise. This means that they must be evaluated as a combination of white and 1/f noise. Using equation (9) and Table 1, the output noise is:

$$E_{Trms} = \sqrt{ENB\left(4kTR_2A + 4kTR_3A^2\right) + i_w^2\left(R_2^2 + R_3^2A^2\right)\left(f_{inc}\, ln \frac{f_H}{f_L} + ENB \right) + e_w^2\, A^2 \left(f_{enc} ln \frac{f_H}{f_L} + ENB \right)}$$

Where $A = (R_1 + R_2)/R_1$, i_W is the white current noise specification (spectral density in $A/\sqrt{Hz}$), f_{inc} is the current noise corner frequency, e_W is the white voltage noise specification (spectral density in $V/\sqrt{Hz}$, and f_{enc} is the voltage noise corner frequency. ENB is determined by the frequency characteristics of the circuit. f_H/f_L is set equal to ENB.

In CMOS input op amps, noise currents are normally so low that the input noise voltage dominates and the i_W terms are not factored into the noise computation. Also, since bias current is very low, there is no need to use R_3 for bias current compensation, and it, too, is removed from the circuit and the calculations. With these simplifications the formula above reduces to:

$$E_{Trms} = \sqrt{ENB\ 4kTR_2\ A + e_w^2\ A^2\left(f_{enc}\ ln\ \frac{f_H}{f_L} + ENB\right)} \qquad \text{CMOS input op amps}$$

Differential Op Amp Circuit Noise Calculations

A noise analysis for a differential amplifier can be done in the same manner as the previous example. Figure 17 shows the circuit used for the analysis.

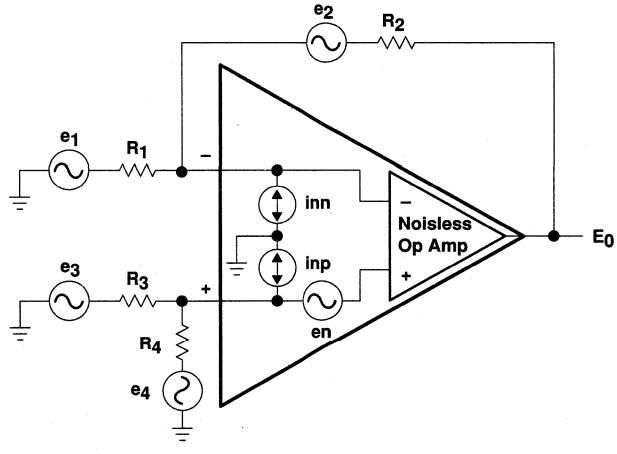
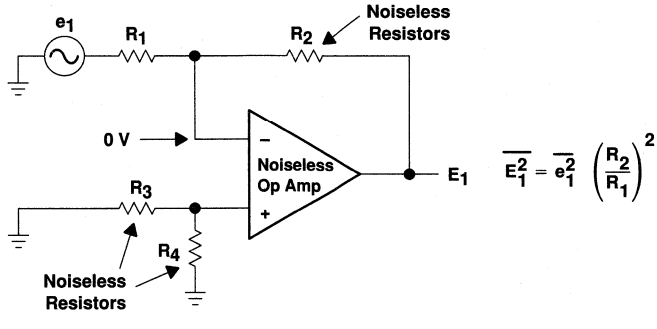


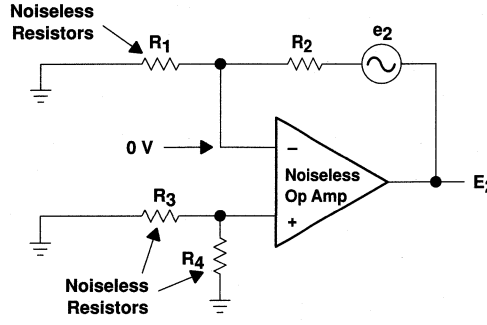
Figure 17. Differenital Op Amp Circuit Noise Model

Figures 18 through 21 show the analysis.



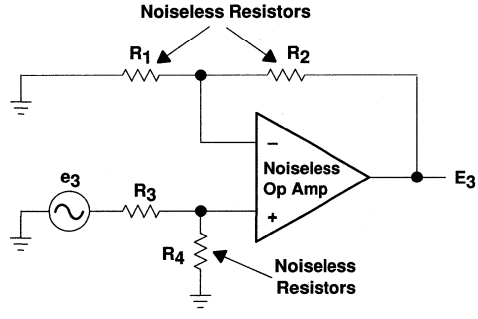
$$\overline{E_1^2} = \overline{e_1^2}\left(\frac{R_2}{R_1}\right)^2$$

Figure 18. e1



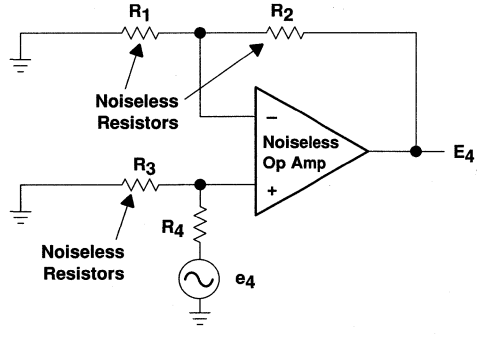
$$\overline{E_2^2} = \overline{e_2^2}$$

Figure 19. e2



$$\overline{E_3^2} = \overline{e_3^2}\left[\left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_1}\right)\right]^2$$

Figure 20. e3



$$\overline{E_4^2} = \overline{e_4^2}\left[\left(\frac{R_3}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_1}\right)\right]^2$$

Figure 21. e4

Combining to arrive at the solution for the circuit's output rms noise voltage, E_{Rrms}, due to the thermal noise in the resistors in the circuit:

(18)

$$E_{Rrms} = \sqrt{E1^2 + E2^2 + E3^2 + E4^2}$$

$$E_{Rrms} = \sqrt{\int \left[\left(4kTR1\left(\frac{R2}{R1}\right)^2 \right) + (4kTR2) + \left(4kTR3\left(\frac{R4}{R3 + R4}\right)^2 \left(\frac{R1 + R2}{R1}\right)^2 \right) + \left(4kTR4\left(\frac{R3}{R3 + R4}\right)^2 \left(\frac{R1 + R2}{R1}\right)^2 \right) \right] df}$$

$$E_{Rrms} = \sqrt{\int 4kT \left[\frac{R2^2}{R1} + R2 + \left(R3\left(\frac{R4}{R3 + R4}\right)^2 \left(\frac{R1 + R2}{R1}\right)^2 \right) + \left(R4\left(\frac{R4}{R3 + R4}\right)^2 \left(\frac{R1 + R2}{R1}\right)^2 \right) \right] df}$$

Normally $R_1 = R_3$ and $R_2 = R_4$. Making this substitution reduces the above equation to:

$$E_{Rrms} = \sqrt{\int 8kTR2\left(1 + \frac{R2}{R1}\right) df} \qquad \textit{If } R1 = R3 \textit{ and } R2 = R4 \tag{19}$$

Now consider the noise sources associated with the op amp itself. The analysis proceeds as before as shown in Figures 22 through 24.

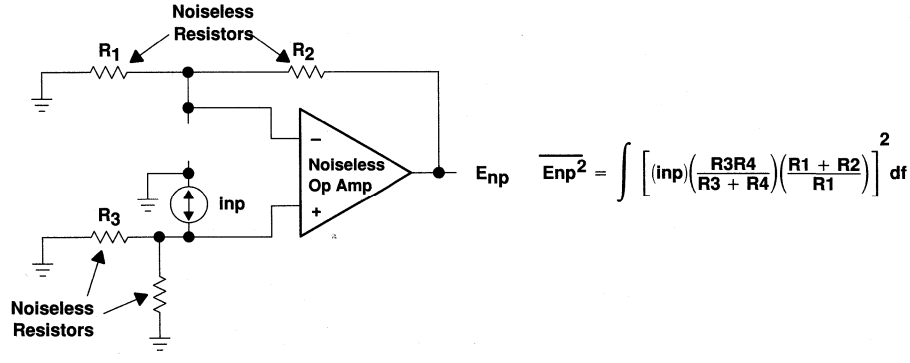


Figure 22. inp

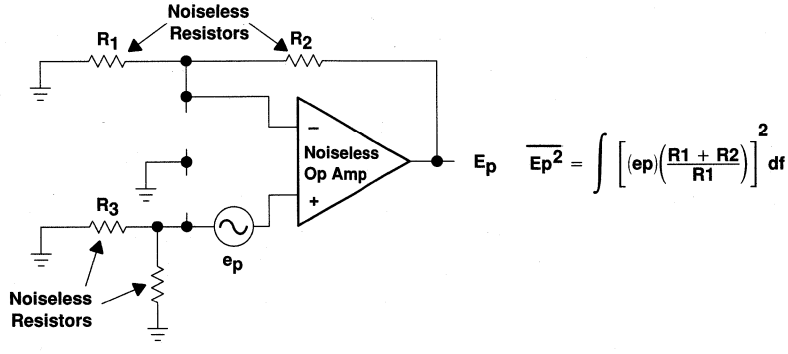


Figure 23. ep

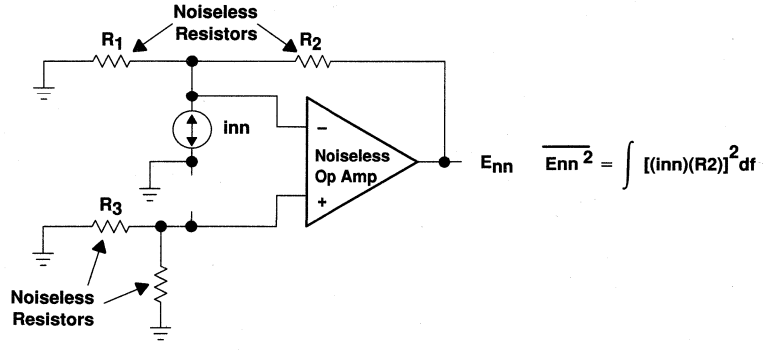


Figure 24. inn

Combining to arrive at the solution for the circuit's output rms noise voltage, E_{oarms}, due to the input referred op amp noise in the circuit:

(20)

$$E_{oarms} = \sqrt{\overline{Ep}^2 + \overline{Enp}^2 + \overline{Enn}^2}$$

$$E_{oarms} = \sqrt{\int \left[((inn)\ R2)^2 + \left((inp) \left(\frac{R3R4}{R3 + R4} \right) \left(\frac{R1 + R2}{R1} \right) \right)^2 + \left(ep \left(\frac{R1 + R2}{R1} \right) \right)^2 \right] df}$$

Normally $R_1 = R_3$, $R_2 = R_4$, and $inn = inp = in$. Making this substitution reduces the above equation to:

(21)

$$E_{oarms} = \sqrt{\int \left[(2inR2)^2 + \left(en \left(\frac{R1 + R2}{R1} \right) \right)^2 \right] df}$$

$$R1 = R3,\ R2 = R4 \text{ and } inn = inp = in$$

Now combine the resistor noise and the op amp noise to get the total output rms noise voltage, E_{Trms}.

(22)

$$E_{Trms} = \sqrt{\int \left[((inn)\ R2)^2 + \left((inp)\left(\frac{R3R4}{R3+R4}\right)\left(\frac{R1+R2}{R1}\right)\right)^2 + \left(en\left(\frac{R1+R2}{R1}\right)\right)^2 + \left(4kTR1\left(\frac{R2}{R1}\right)^2\right) + (4kTR2) + \left(4kTR3\left(\frac{R4}{R3+R4}\right)^2\left(\frac{R1+R2}{R1}\right)^2\right) + \left(4kTR4\left(\frac{R3}{R3+R4}\right)^2\left(\frac{R1+R2}{R1}\right)^2\right)\right] df}$$

$$E_{Trms} = \sqrt{\int \left[((inn)\ R2)^2 + \left((inp)\left(\frac{R3R4}{R3+R4}\right)\left(\frac{R1+R2}{R1}\right)\right)^2 + \left(en\left(\frac{R1+R2}{R1}\right)\right)^2 + 4kT\left[\frac{R2^2}{R1} + R2 + \left(R3\left(\frac{R4}{R3+R4}\right)^2\left(\frac{R1+R2}{R1}\right)^2\right) + \left(R4\left(\frac{R4}{R3+R4}\right)^2\left(\frac{R1+R2}{R1}\right)^2\right)\right]\right] df}$$

Substituting $R_1 = R_3$, $R_2 = R_4$, and $inn = inp = in$:

(23)

$$E_{Trms} = \sqrt{\int \left[2\ (inR2)^2 + \left(en\left(\frac{R1+R2}{R1}\right)\right)^2 + 8kTR2\left(\frac{R1+R2}{R1}\right)\right] df}$$

$$R1 = R3,\ R2 = R4 \text{ and } inn = inp = in$$

Evaluating the integral using these simplifications results in:

(24)

$$E_{Trms} = \sqrt{ENB\ 8kTR_2A + 2\left(i_w^2\ R_2^2\right)\left(f_{inc}\ ln\ \frac{f_H}{f_L} + ENB\right) + e_w^2\ A^2\left(f_{enc}\ ln\ \frac{f_H}{f_L} + ENB\right)}$$

$$R1 = R3,\ R2 = R4 \text{ and } inn = inp = in$$

Where $A = (R_1 + R_2)/R_1$, i_w is the white current noise specification (spectral density in A/$\sqrt{Hz}$), f_{inc} is the current noise corner frequency, e_w is the white voltage noise specification (spectral density in V/$\sqrt{Hz}$), and f_{enc} is the voltage noise corner frequency. ENB is determined by the frequency characteristics of the circuit. f_H/f_L is set equal to ENB.

Summary

The techniques presented here can be used to perform a noise analysis on any circuit. Superposition was chosen for illustrative purposes, but the same solutions can be derived by using other circuit analysis techniques.

Noise is a purely random signal; the instantaneous value and/or phase of the waveform cannot be predicted at any time. The only information available for circuit calculations is the average mean-square value of the signal. With multiple noise sources in a circuit, the total root-mean-square (rms) noise signal that results is the square root of the sum of the average mean-square values of the individual sources.

$$E_{Totalrms} = \sqrt{e_{1rms}^2 + e_{2rms}^2 + \ldots e_{nrms}^2}$$

Because noise adds by the square, when there is an order of magnitude or more difference in value, the lower value can be ignored with very little error. For example:

$$\sqrt{1^2 + 10^2} = 10.05$$

If the 1 is ignored, the error is 0.5%. With modern computational resources, evaluation of all the terms is trivial, but it is important to understand the principles so that time will be spent reducing the 10 before working on the 1.

Noise is normally specified as a spectral density in rms volts or amps per root Hertz, $V/\sqrt{Hz}$ or $A/\sqrt{Hz}$. To calculate the amplitude of the expected noise signal, the spectral density is integrated over the equivalent noise bandwidth (ENB) of the circuit.

Very often the peak-to-peak value of the noise is of interest. Once the total rms noise signal is calculated, the expected peak-to-peak value can be calculated. The instantaneous value will be equal to or less than 6 times the rms value 99.7% of the time.

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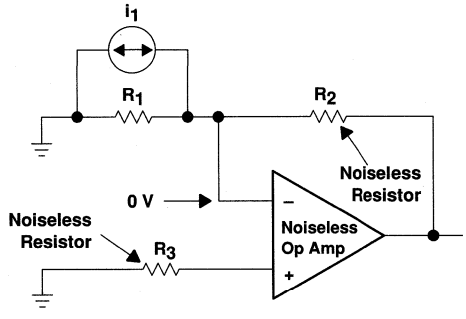
Appendix A Using Current Sources for Resistor Noise Analysis

Figures A1 through A3 show analysis of the resistor noise in the inverting/noninverting op amp noise analysis circuit using current sources in parallel with the noiseless resistors.

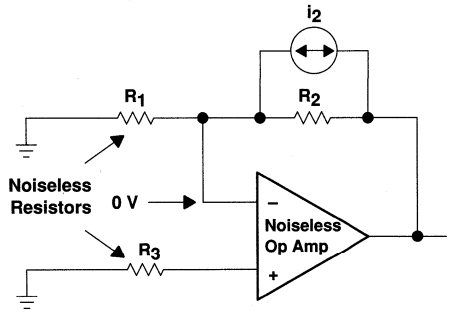


$$\overline{E_1} = \overline{I_1}\, R_1 \frac{R_2}{R_1} = \overline{i_1} R_2$$

$$\overline{E_1}^2 = \left(\overline{i_1} R_2\right)^2$$

$$\overline{i_1}^2 = \int \frac{4kT}{R_1}\, df$$

Figure A–1. E1

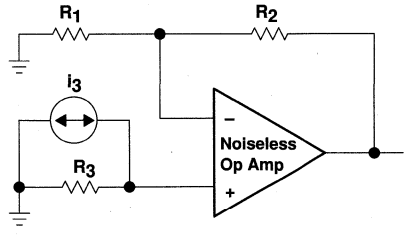


$$\overline{E_2} = \overline{i_2}\, R_2$$

$$\overline{E_2}^2 = \left(\overline{i_2} R_2\right)^2$$

$$\overline{i_2}^2 = \int \frac{4kT}{R_2}\, df$$

Figure A–2. E2



$$\overline{E_3} = \overline{i_3}\, R_3 \left(\frac{R_1 + R_2}{R_1}\right)$$

$$\overline{E_3}^2 = \left[\overline{i_3}\, R_3 \left(\frac{R_1 + R_2}{R_1}\right)\right]^2$$

$$\overline{I_3}^2 = \int \frac{4kT}{R_3}\, df$$

Figure A–3. E3

Combining the independent noise signals:

(A–1)

$$E_{Rrms} = \sqrt{\overline{E_1}^2 + \overline{E_2}^2 + \overline{E_3}^2}$$

$$E_{Rrms} = \sqrt{\int \left[\frac{4kT}{R_1} R_2^2 + \frac{4kT}{R_2} R_2^2 + \frac{4kT}{R_3} R_3^2 \left(\frac{R_1 + R_2}{R_1} \right)^2 \right] df}$$

$$E_{Rrms} = \sqrt{\int \left[4kTR_2 \left(\frac{R_1 + R_2}{R_1} \right) + 4kTR_3 \left(\frac{R_1 + R_2}{R_1} \right)^2 \right] df}$$

The resulting equation is the same as equation (12) presented earlier.

PowerPAD Thermally Enhanced Package

TECHNICAL BRIEF: SLMA002

Mixed Signal Products

Semiconductor Group
21 November 1997

TEXAS INSTRUMENTS

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Contents

Figures

Tables

PowerPAD Thermally Enhanced Package

Abstract

The PowerPAD thermally enhanced package provides greater design flexibility and increased thermal efficiency in a standard size IC package. PowerPAD's improved performance permits higher clock speeds, more compact systems and more aggressive design criteria.

PowerPAD packages are available in several standard surface mount configurations. They can be mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.

To make optimum use of the thermal efficiencies designed into the PowerPAD package, the PCB must be designed with this technology in mind. This document will focus on the specifics of integrating a PowerPAD package into the PCB design.

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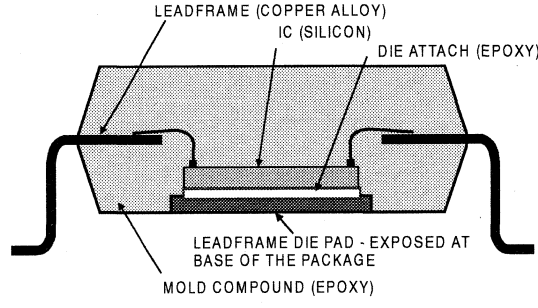
1. Introduction

The PowerPAD concept is implemented in a standard epoxy-resin package material. The integrated circuit die is attached to the leadframe die pad using a thermally conductive epoxy. The package is molded so that the leadframe die pad is exposed at a surface of the package. This provides an extremely low thermal resistance (Θ_{jc}) path between the IC junction and the exterior of the case. Because the external surface of the leadframe die pad is on the PCB side of the package, it can be attached to the board using standard flow soldering techniques. This allows efficient attachment to the board, and permits board structures to be used as heat sinks for the IC. Using vias, the leadframe die pad can be attached to a ground plane or special heat sink structure designed into the PCB. For the first time, the PCB designer can implement power packaging without the constraints of extra hardware, special assembly instructions, thermal grease or additional heat sinks.

Figure 1. Schematic Representation of the PowerPAD Package Components



Section View of a PowerPAD(tm) PACKAGE

Because the exact thermal performance of any PCB is dependent on the details of the circuit design and component installation, exact performance figures cannot be given here. However, representative performance is very important in making design decisions. The data shown in Table 1 is typical of the performance that can be expected from the PowerPAD package.

Table 1. Typical Power Handling Capabilities of PowerPAD Packages

Package Type	Pin Count	Standard Package	PowerPAD Package
SSOP	20	0.75 W	3.25 W
TSSOP	24	0.55 W	2.32 W

Notes: 1) Assumes 150° C junction temperature and 80° C ambient temperature.
2) Values are calculated from Θ_{ja} figures shown in Appendix A.

For example, the user can expect 3.25 watts of power handling capability for the PowerPAD version of the 20-pin SSOP package. The standard version of this package can only handle 0.75 watts. Details for all package styles and sizes are given in Appendix A.

2. Installation and Use

2.1 PCB Attachment

Proper thermal management of the PowerPAD package requires PCB preparation. This preparation is not difficult, nor does it use any extraordinary PCB design techniques, however it is necessary for proper heat removal.

Figure 2. Bottom and Top View of the 20 pin TSSOP PowerPAD Package

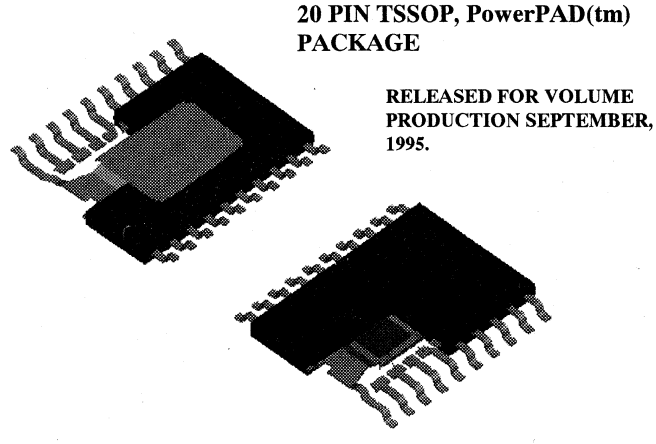
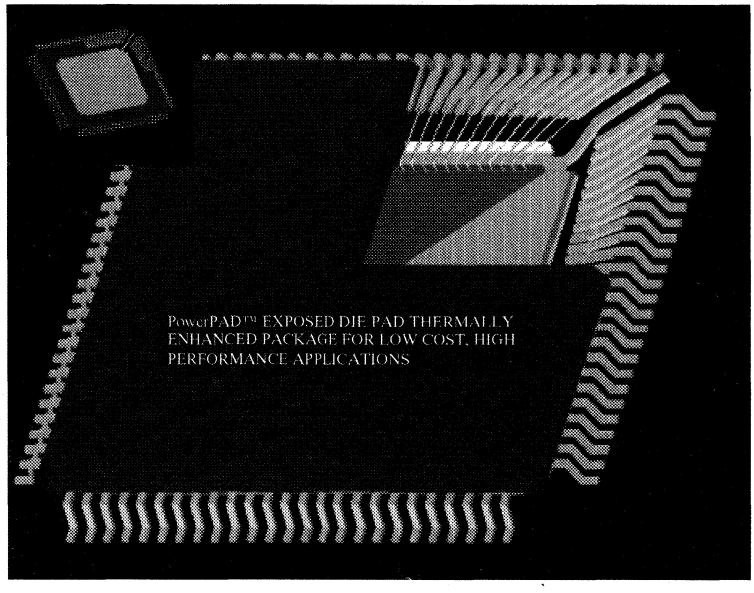


Figure 3. 64 Pin, 14 x 14 x 1.0mm Body TQFP PowerPAD Package



All of the thermally enhanced packages incorporate features that provide a very low thermal resistance path for heat removal from the integrated circuit - either to and through a printed circuit board (in the case of zero airflow environments), or to an external heatsink. The TI PowerPAD implementation does this by creating a leadframe where the bottom of the die pad is even with a surface of the package (as opposed to the case where a heat slug is embedded in the package body to create the thermal path). (See Figure 2 and Figure 3.)

2.2 PCB Design Considerations

The printed circuit board that will be used with PowerPAD packages must have features included in the design to remove the heat from the package efficiently.

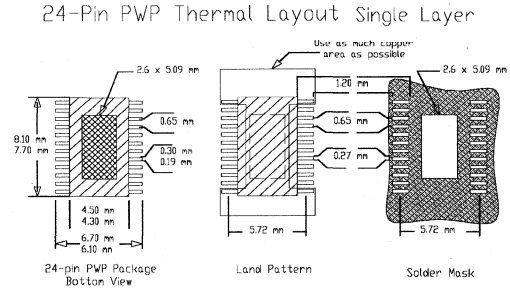
As a minimum, there must be an area of solder-tinned-copper underneath the PowerPAD package. This area is called the thermal land. As detailed below, the thermal land will vary in size depending on the PowerPAD package being used, the PCB construction and the amount of heat that needs to be removed. In addition, this thermal land may or may not contain thermal vias depending on PCB construction. The requirements for thermal lands and thermal vias are detailed below.

2.3 Thermal Lands

A thermal land is required on the surface of the PCB directly underneath the body of the PowerPAD package. During normal surface mount flow solder operations the leadframe on the underside of the package will be soldered to this thermal land creating a very efficient thermal path. Normally, the PCB thermal land will have a number of thermal vias within it that provide a thermal path to internal copper areas (or to the opposite side of the PCB) that provide for more efficient heat removal. The size of the thermal land should be as large as needed to dissipate the required heat.

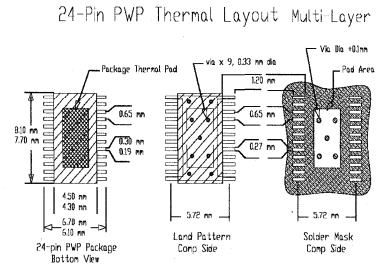
For simple, double-sided PCBs, where there are no internal layers, the surface layers must be used to remove heat. Shown in Figure 4 is an example of a thermal land for a 24-pin package. Details of the package, the thermal land and the required solder mask are shown. If the PCB copper area is not sufficient to remove the heat, the designer can also consider external means of heat conduction, such as attaching the copper planes to a convenient chassis member or other hardware connection.

Figure 4. Package and PCB Land Configuration for a Single Layer PCB



For multilayer PCBs, the designer can take advantage of internal copper layers (such as the ground plane) for heat removal. The external thermal land on the surface layer is still required, however the thermal vias can conduct heat out through the internal power or ground plane. Shown in Figure 5 is an example of a thermal land used for multilayer PCB construction. In this case, the primary method of heat removal is down through the thermal vias to an internal copper plane.

Figure 5. Package and PCB Land Configuration for a Multi-Layer PCB



Shown in Figure 6 are the details of a 64 pin TQFP PowerPAD package. The recommended PCB thermal land for this package is shown in Figure 7.

The maximum land size for TQFP packages is the package body size minus 2.0 mm. This land is normally attached to the PCB for heat removal, but can be configured to take the heat to an external heat sink. This is preferred when airflow is available.

Figure 6. 64 pin TQFP Package with PowerPAD Implemented, Bottom View

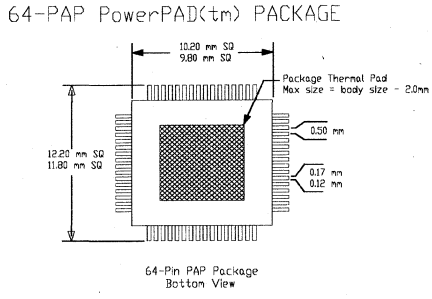
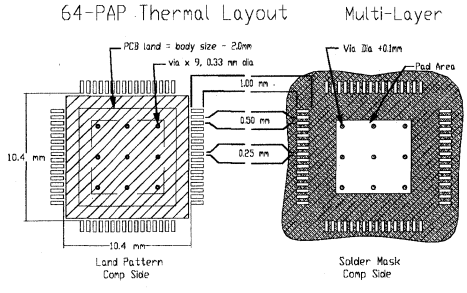


Figure 7. PCB Thermal Land Design Considerations for Thermally Enhanced TQFP Packages



2.4 Thermal Vias

Thermal vias are the primary method of heat transfer from the PCB thermal land to the internal copper planes or to other heat removal sources. The number of vias used, the size of the vias and the construction of the vias are all important factors in both the PowerPAD package thermal performance and the package-to-PCB assembly. Recommendations and guidelines for thermal vias follow.

Shown in Figure 8 and Figure 9 are the effects on PCB thermal resistance of varying the number of thermal vias for various sizes of die for 2- and 4-layer PCBs. As can be seen from the curves, there is a point of diminishing returns where additional vias will not significantly improve the thermal transfer through the board. For a small die, having from five to nine vias should prove adequate for most applications. For larger die, a higher number may be used simply because there is more space available under the larger package. Shown in Figure 10 are examples of ideal thermal land size and thermal via patterns for PowerPAD™ packages using 0.33mm (13 mil) diameter vias plated with 1 oz. copper. This thermal via pattern set represents a copper cross section in the barrel of the thermal via of approximately 1% of the total thermal land area. Fewer vias may be utilized and still attain a reasonable thermal transfer into and through the PCB as shown in Figures 8 and 9.

The number of thermal vias will vary with each product being assembled to the PCB, depending on the amount of heat that must be moved away from the package, and the efficiency of the system heat removal method. Characterization of the heat removal efficiency versus the thermal via copper surface area should be performed to arrive at an optimum value for a given board construction. Then the number of vias required can be determined for any new design to achieve the desired thermal removal value.

Figure 8. Impact of the Number of Thermal Vias versus Chip Area (Die Area)

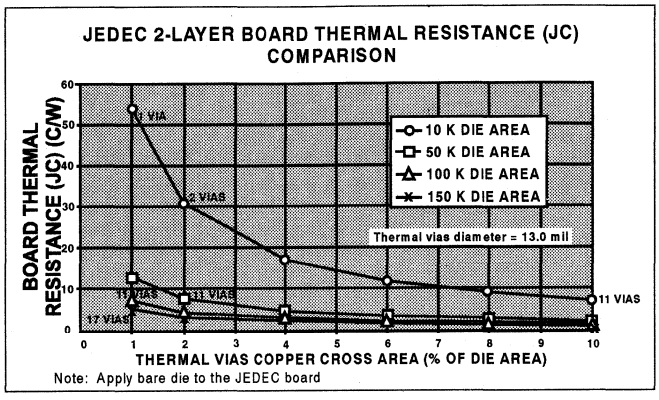


Figure 9. Impact of the Number of 0.33mm (0.013 inch) Diameter Thermal Vias versus Chip Area (Die Area)

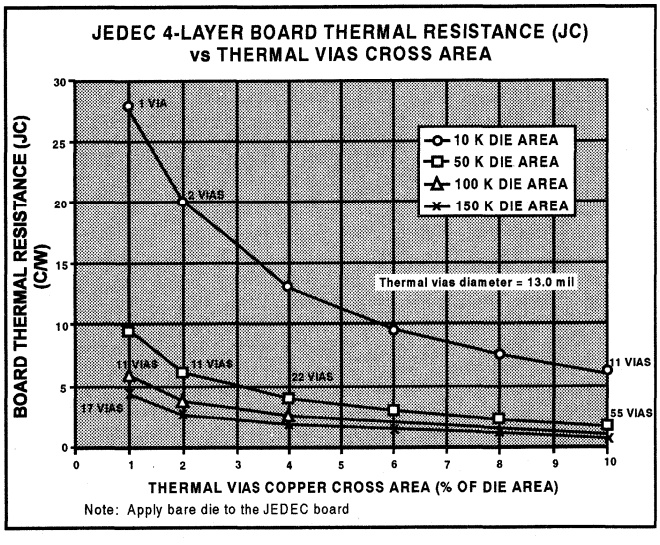
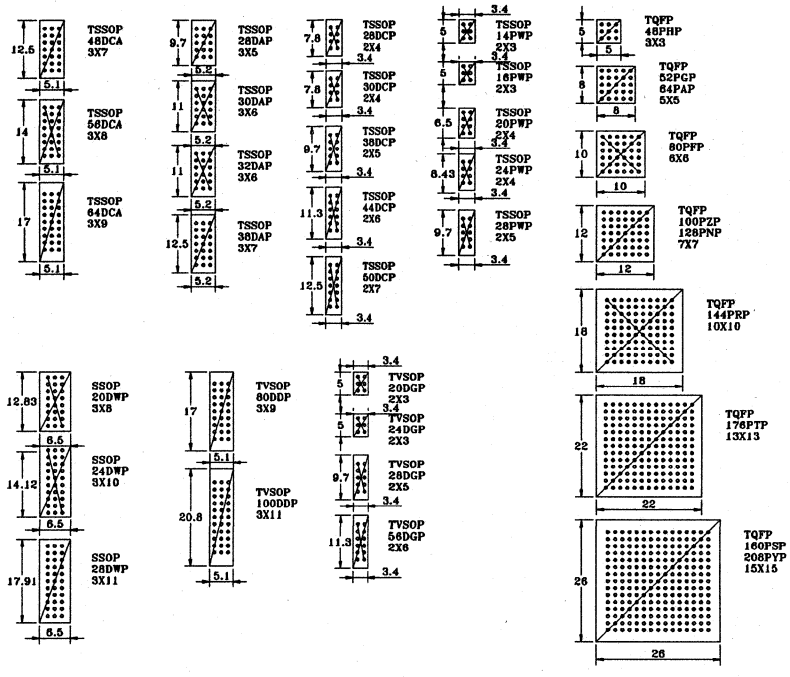


Figure 10. Ideal Thermal Land Size and Thermal Via Patterns for PowerPAD



Thermal vias connect the thermal land to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the thermal land on the surface of the board during solder reflow. The experiments conducted jointly with Solectron Texas indicate that a via drill diameter of 0.33mm (13 mils) or smaller works well when 1 ounce copper is plated at the surface of the board and simultaneously plating the barrel of the via. If the thermal vias will not be plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a dimension equal to the via diameter + 0.1mm minimum. This will prevent the solder from being wicked through the thermal via and potentially creating a solder void in the region between the package bottom and the thermal land on the surface of the PCB.

To assure the optimum thermal transfer through the thermal vias to internal planes or the reverse side of the PCB, the thermal vias used in the thermal land should *not* use web construction techniques. Web construction on PCB vias is a standard technique used in most PCBs today to facilitate soldering, by constructing the via so that it has a high thermal resistance. This is *not* desirable for heat removal from the PowerPAD package. Therefore it is recommended that all vias used under the package make internal connections to the planes using a continuous connection completely around the hole diameter. Web construction for thermal vias is not recommended.

2.5 Solder Stencil Determination

A series of experiments were conducted at Solectron-Texas to determine the effects of solder stencil thickness on the quality of the solder joint between the thermal pad of a PowerPAD package and the thermal land on the surface of the PCB. Stencil thickness of 5, 6, and 7 mils were used in conjunction with a metal squeegee to deposit solder in the desired locations on the board. Note: 6 and 7 mil thick solder stencil is normally used with package lead pitch of 0.5 and 0.65mm respectively. A 5 mil thick stencil is normally used for packages with 0.4mm lead pitch to avoid solder bridging during reflow.

It was found that the standoff height for the package being attached to the PCB was critical in making good solder joints between the thermal pad of the package and the thermal land on the PCB. Note: during this series of experiments, a good solder joint was defined as a connection that joined at least 90% of the area of the smallest pattern to its intended connection point - such as the thermal pad of the package to the thermal land on the PCB. When the standoff height of the package (i.e., the distance between the bottom of the package leads and the bottom of the package body) was in the range of 0 to 2 mils, the package tended to float on the solder. This led to the possibility that all leads of the package would not be soldered to the lead traces on the board. This happened even when the 5 mil thick stencil was utilized. There were also cases when the solder was squeezed out from the desired land area, and then formed solder balls during the reflow process - an undesirable result that could cause shorting between package leads on the board surface, or short the thermal land on the PCB to the lead traces. A standoff height of 2.0 to 4.2 mils provided good solder joints for both the leads and the thermal pad for stencil thickness of 5, 6, and 7 mils. When the standoff height of the package was between 4.2 and 6.0 mils, only the 6 and 7 mil thick stencil provided consistently good solder joints for both the package leads and the thermal-pad to thermal-land bond. A general guideline would be to use the thickest solder stencil that works well for the products being assembled for the most process margin in assembling thermally enhanced parts to a PCB.

The Joint Electron Devices Engineering Council (JEDEC) specification for the standoff height of TSSOP and TQFP packages is the range of 0.05 to 0.15mm (1.97 to 5.91 mils), and is an acceptable range when the solder stencil thickness of 6 and 7 mils are used. Texas Instruments has elected to center the stand-off height of the PowerPAD packages at 3.5 mils (within the JEDEC specification range) to provide good package to PCB solder joint characteristics for standard solder stencil thickness of 5, 6, and 7 mils - the most common range within industry practice today.

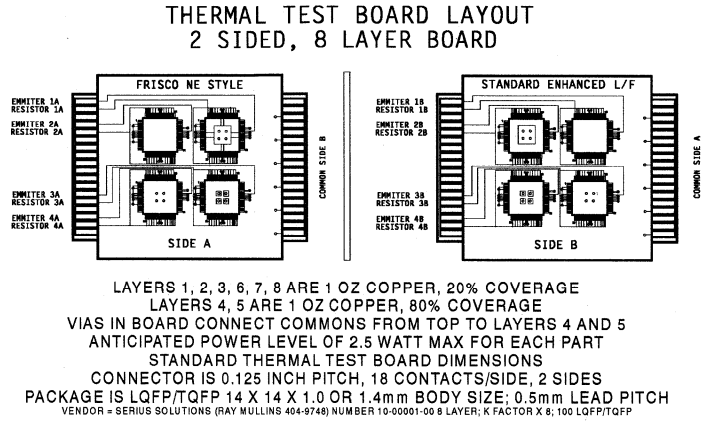
3. Assembly

Solder joint inspection in the attachment area of the thermal pad of the thermally enhanced packages to the thermal land on the PCB is difficult to perform with the best option to date being x-ray inspection. Tests performed within Texas Instruments and during the joint PCB experiments with Solectron-Texas indicate that x-ray inspection will allow detection of voiding within the solder joint and could be used either in a monitor mode, or for 100% inspection if required by the application. However, this is a slow and costly process so an effort was made to determine the minimum amount of solder required in this joint before degradation of the thermal performance became significant.

The experimental vehicle used in determining the amount of solder required was a 6S2P double sided test board with copper thermal lands on the surface of the board representing 0%, 7.5%, 22%, and 83% of the package body area. The package used was a 100 pin PowerPAD package (side B - standard enhanced I/f side of the PCB) as shown in Figure 11. There was additional copper area on the surface of the A side of the board due to connections between selected pins and the thermal land area. Four thermal vias were created in each thermal land area with connections to the internal power or ground plane, and continuing to make connection to the thermal land on the opposite side of the board.

A thermal test chip (Texas Instruments x-1158240) with dimensions of 6.1mm (0.240-inch) square was assembled in the test packages using die pad sizes of 6.0mm square, and 9.0mm square. The assembled units were then mounted to the PCB using either eutectic Sn63:Pb37 solder or thermally conductive epoxy adhesive. Measurement of the thermal resistance junction-to-case and thermal resistance junction-to-ambient with the individual packed parts powered at 2.5 watts was made using standard techniques for these measurements. Results are shown in Table 1 for tests with and without attachment between the package thermal pad and the board thermal land, as well as a comparison between solder and thermally conductive epoxy attachment. Table 2 provides the effective connection area obtained for each of the measurement points.

Figure 11. Test Board for Measurement of Θ_{jc} and Θ_{ja} Using 100 pin PowerPAD TQFP Packages



The relative thermal land size and location is shown along with the location of the thermal vias that connect the surface thermal land to the internal power or ground plane, and continuing to connect to the thermal land on the opposite side of the board. The board is approximately 82.5mm (3.25 inch) square.

Table 2 and Table 3 show the thermal resistance data for Θ_{jc} and Θ_{ja} (junction to case, and junction to ambient) for the 8 layer thermal test board, with the copper thermal land on the PCB shown as a percentage of the area of the package body.

Table 2. Measured Θ_{jc} from Test Board

		MEASURED DATA				
		Θ_{jc}	Θ_{jc}	Θ_{jc}	Θ_{jc}	Θ_{jc}
Part position on PCB	PCB Copper land as % of package body area	6mm Die Pad Soldered one side only	9mm Die Pad Not Soldered to PCB	9mm Die Pad Soldered one side only	9mm Die Pad Soldered both sides of PCB	9mm Die Pad Epoxy used to attach to PCB
1B	0	**9.3**		**9.9**	**11.4**	
4B	7.5			**7.2**	**5.8**	**7.2**
2B	22	**6.8**		**6.3**	**7.2**	**7.5**
3B	83	**6.2**		**6.2**	**6.2**	**6.2**
2A	0	8.7	7.4	**9.1**	**7.8**	**7.8**
3A	7.5	7.6	8.3	**6.3**	**6.8**	**6.8**
1A	30		8		**6.6**	**6.5**
4A	85	7.5	7.3	**6.4**	**6.4**	**6.9**

Notes: 1) Numbers in **bold** have die pad attached to the board.
2) Power level for all measurements is 2.5 watt.
3) Θ_{jc} is measured in 1 cubic foot of liquid freon.

Table 3. Measured Θ_{ja} from Test Board

		MEASURED DATA				
		Θ_{ja}	Θ_{ja}	Θ_{ja}	Θ_{ja}	Θ_{ja}
Part position on PCB	PCB Copper land as % of package body area	6mm Die Pad Soldered one side only	9mm Die Pad Not Soldered to PCB	9mm Die Pad Soldered one side only	9mm Die Pad Soldered both sides of PCB	9mm Die Pad Epoxy used to attach to PCB
1B	0	**33.8**		**40.6**	**44.3**	
4B	7.5			**27**	**23.1**	**25.5**
2B	22	**28.4**		**25.8**	**25**	**24.3**
3B	83	**24.2**		**26.9**	**24.6**	**24**
2A	0	34.4	34	**33.3**	**32.3**	**25.8**
3A	7.5	33.5	33	**24.4**	**24.9**	**25.2**
1A	30		31		**24.4**	**23.2**
4A	85	33.3	30	**25.5**	**24.6**	**24**

Notes: 1) Numbers in **bold** have die pad attached to the board.
2) Power level for all measurements is 2.5 watt.
3) Θ_{ja} is measured in 1 cubic foot of still air.

Small changes in the percentage of copper land area (between the "A" side of the PCB and the "B" side of the PCB) do not significantly affect the thermal resistance.

Table 4 and Table 5 show the relationship of the solder joint area between the thermal pad in the PowerPAD package and the thermal land of the PCB for the thermal resistance values obtained in Table 2 and Table 3.

Table 4. Relationship of the Solder Joint Area on Θ_{jc}, from Test Board Data

THERMAL PAD TO THERMAL LAND CONNECTION AREA ANALYSIS - %						
		Θ_{jc}	Θ_{jc}	Θ_{jc}	Θ_{jc}	Θ_{jc}
Position on PCB	PCB Copper land size on PCB	6mm Die Pad Soldered one side only	9mm Die Pad Not Soldered to PCB	9mm Die Pad Soldered one side only	9mm Die Pad Soldered both sides of PCB	9mm Die Pad Epoxy used to attach to PCB
1B	0	**0**	0	**0**	**0**	**0**
4B	4*(2x2)	**36**	16	**16**	**16**	**100**
2B	1*(6x6)	**80**	32	**32**	**32**	**100**
3B	1*(12x12)	**100**	100	**100**	**100**	**100**
2A	0	0	0	**0**	**0**	**0**
3A	4*(2x2)	80	16	**16**	**16**	**100**
1A	1*(6x6)+4*(5.7)	85	58	**58**	**58**	**100**
4A	1*(12x12)+4*(5.6)	100	100	**100**	**100**	**100**

Notes: 1) Numbers in **bold** have die pad attached to the board.
2) Power level for all measurements is 2.5 watt.
3) Θ_{jc} is measured in 1 cubic foot of liquid freon.

Table 5. Relationship of the Solder Joint Area on Θ_{ja}, from Test Board Data

THERMAL PAD TO THERMAL LAND CONNECTION AREA ANALYSIS - %						
		Θ_{ja}	Θ_{ja}	Θ_{ja}	Θ_{ja}	Θ_{ja}
Position on PCB	PCB Copper land as % of package body area	6mm Die Pad Soldered one side only	9mm Die Pad Not Soldered to PCB	9mm Die Pad Soldered one side only	9mm Die Pad Soldered both sides of PCB	9mm Die Pad Epoxy used to attach to PCB
1B	0	**0**	0	**0**	**0**	**0**
4B	4*(2x2)	**36**	16	**16**	**16**	**100**
2B	1*(6x6)	**80**	32	**32**	**32**	**100**
3B	1*(12x12)	**100**	100	**100**	**100**	**100**
2A	0	0	0	**0**	**0**	**0**
3A	4*(2x2)	80	16	**16**	**16**	**100**
1A	1*(6x6)+4*(5.7)	85	58	**58**	**58**	**100**
4A	1*(12x12)+4*(5.6)	100	100	**100**	**100**	**100**

Notes: 1) Numbers in **bold** have die pad attached to the board.
2) Power level for all measurements is 2.5 watt.
3) Θ_{ja} is measured in 1 cubic foot of still air.

In this example, there is significant improvement in thermal heat removal with solder joint areas as small as 16%, and the thermal removal efficiency as measured by Θ_{jc} and Θ_{ja} are within measurement error tolerance for all solder joint areas greater than 32%.

Based on the measured data for this test board configuration, Texas Instruments recommends a minimum solder joint area of 50% of the package thermal pad area when the part is assembled on a PCB. The results of the PCB assembly study conducted with Solectron-Texas indicate that standard board assembly processes and materials will normally achieve >80% solder joint area without any attempt to optimize the process for thermally enhanced packages. A characterization of the solder joint achieved with a given process should be conducted to assure that the results obtained during testing apply directly to the customer application, and that the thermal efficiency in the customer application is similar to the thermal test board results for the power level of the packaged component. If the heat removal is not at the efficiency desired, then either additional thermal via structures will have to be added to the PCB construction, or additional thermal removal paths will need to be defined (such as direct contact with the system chassis).

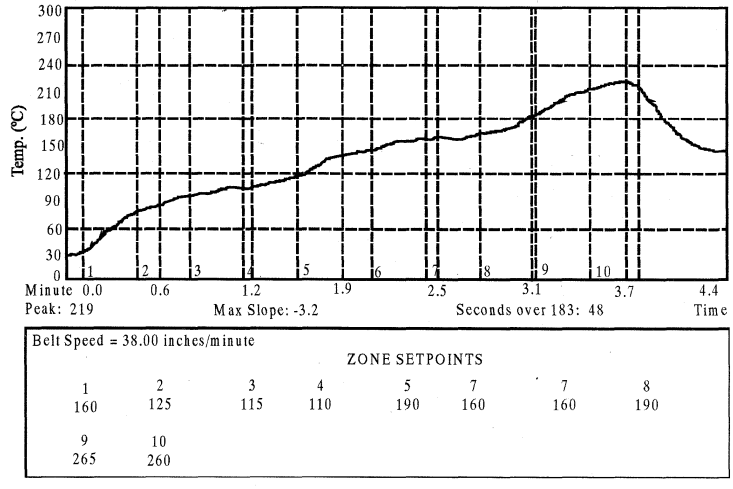
An alternative to attaching the thermal pad of the package to the thermal land of the PCB with solder is to use thermally conductive epoxy for the attachment. This epoxy can either be dispensed from the liquid form with a material that will cure during the reflow cycle, or a "B" staged preform that will receive the final cure during the reflow cycle. These materials can be the same as normally used with externally applied heat sinks. When epoxy is used as the attachment mechanism, then the effective attachment area is 100% of the die pad area, and there is some added benefit as thermal transfer to the PCB can occur, even with no copper thermal land at the surface of the PCB.

3.1 Solder Reflow Profile Suggestion

The reflow profile for IR board assembly using the Texas Instruments PowerPAD packages does not have to change from that used with conventional plastic packaged parts. The construction of the package does not add thermal mass, and the only new thermal load is due to the increased solder area between the package thermal pad and the thermal land on the PCB. A typical IR oven profile for fine pitch surface mount packages is shown in Figure 11. for eutectic Sn63:Pb37 solder. Nitrogen purged, convection IR reflow will be advantageous for this part to PCB assembly to minimize the possibility of solder ball formation under the package body.

Figure 12 shows a typical infrared (IR) oven profile for a fine pitch plastic package assembly mounted to an FR-4 PCB using eutectic Sn63:Pb37 solder.

Figure 12. Typical Infrared Oven Profile



Peak temperature should be approximately 220 degrees centigrade, and the exposure time should normally be less than 1 minute at temperatures above 183 degrees centigrade.

3.2 Installation and Assembly Summary

The PowerPAD package families can be attached to printed circuit boards using conventional Infrared solder reflow techniques that are standard in the industry today without changing the reflow process used for normal fine pitch surface mount package assembly. A minimum solder attachment area of 50% of the package thermal pad area is recommended to provide efficient heat removal from the semiconductor package, with the heat being carried into or through the PCB to the final thermal management system. This attachment can be achieved either by the use of solder for the joining material, or through the use of thermally conductive epoxy materials. Typical PCB thermal land pattern definitions have been provided that have been shown to work with 4 and 8 layer PCB test boards, and can be extended for use by other board structures.

4. Repair

Reworking thermally enhanced packaged semiconductors that have been attached to PCB assemblies through the use of solder or epoxy attachment can present significant challenges, depending on the point at which the re-work is to be accomplished. Tests of re-work procedures to date indicate that part removal from the PCB is successful with all of the conventional techniques used in the industry today. The challenge is part replacement on the board due to the combined thermal enhancement of the PCB itself, and the addition of thermal removal enhancement features to the semiconductor package. The traditional steps in the rework or repair process can be simply identified by the following steps for solder attached components:

1) Unsolder old component from the board
2) Remove any remaining solder from the part location
3) Clean the PCB assembly
4) Tin the lands on the PCB and leads, or apply solder paste to the lands on the PCB
5) Target, align, and place new component on the PCB
6) Reflow the new component on the PCB
7) Clean the PCB assembly

When thermally conductive epoxy has been used to attach the thermal pad of the package to the thermal land on the PCB, the same basic steps in the rework or repair procedure can be followed with only minor modifications:

1) Unsolder old component and torque package to remove from the board
2) Remove any remaining solder from the part location
3) Remove any remaining epoxy from the thermal land on the PCB
4) Clean the PCB assembly
5) Tin the lands on the PCB and leads, or apply solder paste to the lands on the PCB
6) Place new thermally conductive "B" staged epoxy preform or dispense epoxy on thermal land
7) Target, align, and place new component on the PCB
8) Reflow the new component on the PCB

9) Complete epoxy cure (if required as a separate step)

10) Clean the PCB assembly

4.1 Part Removal From PCBs

Almost any removal process will work to remove the device from the PCB, even with the thermal pad of the package soldered to the PCB. Heat is easily transferred to the area of the solder attachment either from the exposed surface thermal land of the PCB (single layer example), or through the thermal vias in the PCB (multi-layer example) from the backside of the PCB.

Re-work has been performed for both the TSSOP and TQFP PowerPAD style packages using METCAL removal irons and hot air. The specific example of a 20 pin TSSOP PowerPAD part removal is discussed in detail.

A 750-Watt METCAL removal iron was used in conjunction with hot air to verify the removal method efficiency to take 20 pin PowerPAD TSSOP packages off of assembly test boards. The hot air method is recommended as it subjects the PCB and surrounding components to less thermal and mechanical stress than other methods available, and has been proven to be much easier to control than some of the hot bar techniques. Use of the hot air method may require assemblers to acquire tools specifically for the smaller packages since most assemblers use a hot bar method for packages of this size. (Note: This same tool will also be needed for part re-attachment to the PCB when the hot air method is employed). A tool with an integrated vacuum pick up tip will be an advantage in the part removal process so the part can be physically removed from the board as soon as the solder reaches liquidus. Preheating of the local area of the PCB to a temperature of approximately 160 degrees centigrade can make the part removal easier. This is especially helpful in the case of larger packages such as 56 pin TSSOP or 100-pin TQFP style packages. This preheat will be required in the thermal removal method if the semiconductor package is a heat slug package rather than the TI PowerPAD package version. Some experimentation will be required to find the optimum procedure to use for any specific PCB construction and thermally enhanced package version.

After the part has been removed from the PCB, conventional techniques to clean the area of the part attachment - such as solder wicking - will be needed to prepare the location for subsequent attachment of a new component.

When thermally conductive epoxy has been used for attachment of the package thermal pad to the thermal land on the PCB, a slightly different approach to part removal must be used. This will require a tool that has dimensions that will allow contact with the sides of the package body directly above the leads, and will allow the package to be twisted or rotated horizontally when the solder joints of the package leads have reached liquidus. The temperature at the epoxy interface to the package thermal pad or the PCB thermal land must be above the glass transition temperature of the epoxy (typically less than 180 degrees centigrade) to break the adhesion between the epoxy and the attach location with the twisting or rotational method discussed above. In most cases, any remaining epoxy on the PCB after part removal can be removed by peeling it from the surface - occasionally, it will be necessary to apply heat to the epoxy location so it will peel away from the PCB cleanly.

4.2 Attachment of a Replacement Component to the PCB

Preparation of the PCB for attachment of a new component follows normal industry practice with respect to the lands on the board and the leads of the package. Both may be tinned, and/or solder paste applied to the lands for new component attachment. In addition, when solder will be used to re-attach the thermal pad of the package to the thermal land on the PCB, solder paste will need to be applied to the surface of the thermal land on the board. This may be in the form of stripes of solder paste with sufficient volume to achieve the desired solder coverage, or a solder preform may be applied to the location for attachment. In a factory environment, the component is then placed in the desired location and alignment, and processed through a reflow oven to re-establish the desired solder joints. This is the most desirable process and is normally the easiest to accomplish.

When a manual or off-line attachment and reflow procedure is to be used, the challenge of supplying sufficient heat to the components and solder becomes a greater concern. In most cases, the corner leads of the package being attached will be tack soldered to hold the component in alignment so the balance of the leads and the thermal pad to thermal land solder reflow can be accomplished without causing part movement from its desired location. As in the part removal case, it is advisable to pre-heat the board or the specific device location to a temperature below the melting point of the solder to minimize the amount of heat that must be provided by the reflow device as the part is being attached. A good starting point is to pre-heat to approximately 160 degrees centigrade. A hot gas reflow tool can then be used to complete the solder joint formation both at the leads and for the connection of the thermal pad to the thermal land of the PCB. Care must be taken at this operation to avoid blowing solder out from the thermal pad to thermal land interface and causing solder balling under the package or creating

lead to lead or thermal land to lead shorts. The thermal enhancement of the package and the PCB will require a higher temperature gas or higher gas flow to reach solder liquidus than would be needed with an assembly lacking these enhancements. The tool should be specifically sized to the part being reworked to minimize possible damage to surrounding components or the PCB itself.

If the re-attachment of the interface between the thermal pad of the package and the thermal land of the PCB using solder attachment is too difficult to control using hot gas methods, then the best approach is to use either a thermally conductive "B" staged epoxy preform cut to the shape of the thermal land on the PCB, or dispensing liquid thermally conductive epoxy in a pattern on the thermal land that will result in at least a 50% void free connection between the pad and the land. Virtually any epoxy material that is used for the attachment of external heat sinks to packaged components is suitable for this application, and cure time/temperature requirements can be matched to the product need (anywhere from 24 hours at room temperature to less than 1 hour at temperatures below 100 degrees centigrade). Care must be taken to choose a material with limited run-out to avoid the possibility of shorting adjacent package leads together or shorting the thermal land of the PCB to the package leads.

It should be noted that the Texas Instruments PowerPAD packages are easier to rework at the board level than other semiconductor packages utilizing metal slugs for the thermal path between the chip and the PCB. This is due to the additional requirement for heating the total mass of the slug to reflow temperatures versus heating the thermal pad of the PowerPAD package. The hot gas temperature and/or flow becomes critical for effective joining of the components without causing damage to the adjacent components or the PCB. In either case, the use of thermally conductive epoxy materials will make the rework task easier and more reliable to perform in a manual repair environment.

5. Summary

An overview of the design, use and performance of the Texas Instruments PowerPAD package has been presented. The package is simple to use and can be assembled and repaired using existing assembly and manufacturing tools and techniques. Package performance is outstanding. By exposing the leadframe on the package bottom, extremely efficient thermal transfer between the die and the PCB can be achieved.

The simplicity of the PowerPAD package not only makes for a low cost package, but there is no additional cost in labor or material for the customer using standard surface mount assembly techniques. The only preparation needed to implement a PowerPAD design is at the PCB design stage. Simply by including a thermal land and thermal vias on the PCB the design can use the PowerPAD package effectively.

Appendix A. Thermal Modeling of PowerPAD Packages

Table 6. Thermal Characteristics for Different Package and PCB Configurations

Package Description			2 oz. Trace and Copper Pad with Solder			2 oz. Trace and Copper Pad without Solder			Standard Package JEDEC Low Effect with 1 oz. trace		
Pkg Type	Pin Count	Package Designator	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Ψ_{JT} (°C/W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Ψ_{JT} (°C/W)	θ_{JA} (°C/W)	θ_{JC} (°C/W)	Ψ_{JT} (°C/W)
SSOP	20	DWP	21.46	0.37	1.617	43.91	0.37	6.031	92.95	16.58	2.212
	24	DWP	20.77	0.27	1.507	38.43	0.27	4.88	80.49	13.49	1.959
	28	DWP	19.52	0.22	1.337	33.92	0.22	4.109	69.73	11.24	1.641
TVSOP	80	DDP	19.88	0.21	0.196	32.64	0.21	0.359	65.53	4.69	0.353
	100	DDP	18.35	0.17	0.182	28.45	0.17	0.313	54.55	3.73	0.297
	20	DGP	37.92	2.46	1.074	95.88	2.46	3.318	192.65	28.85	1.054
	24	DGP	36.87	2.46	1.056	89.50	2.46	3.176	179.91	28.41	0.999
	48	DGP	27.35	0.72	0.45	52.82	0.72	1.138	107.49	12.32	0.58
	56	DGP	25.42	0.58	0.406	46.69	0.58	0.98	95.48	10.40	0.526
TSSOP	48	DCA	22.30	0.32	0.22	40.27	0.32	0.443	84.04	6.63	0.434
	56	DCA	21.17	0.27	0.212	36.42	0.27	0.401	75.50	5.81	0.395
	64	DCA	19.89	0.21	0.196	32.52	0.21	0.357	65.70	4.69	0.35
	28	DAP	25.10	0.45	0.244	51.28	0.45	0.556	110.60	8.96	0.548
	30	DAP	24.20	0.45	0.233	48.34	0.45	0.551	103.45	8.73	0.486
	32	DAP	23.51	0.32	0.233	44.32	0.32	0.468	95.63	7.32	0.478
	38	DAP	22.41	0.31	0.219	41.18	0.31	0.444	87.32	6.57	0.454
	28	DCP	30.62	0.94	0.534	63.99	0.94	1.424	133.67	16.13	0.707
	30	DCP	30.55	0.94	0.532	63.32	0.94	1.408	131.23	16.05	0.695
	38	DCP	27.41	0.72	0.447	52.93	0.72	1.13	109.55	12.42	0.598
	44	DCP	25.57	0.58	0.406	47.18	0.58	0.982	97.13	10.47	0.538
	50	DCP	24.10	0.51	0.369	43.76	0.51	0.892	89.53	9.34	0.5
	14	PWP	37.47	2.07	0.851	97.65	2.07	2.711	195.35	26.86	1.047
	16	PWP	36.51	2.07	0.848	90.26	2.07	2.6	182.31	26.56	0.964
	20	PWP	32.63	1.40	0.607	74.41	1.40	1.777	151.89	19.90	0.77
	24	PWP	30.13	0.92	0.489	62.05	0.92	1.263	128.44	14.83	0.665
	28	PWP	27.87	0.72	0.446	56.21	0.72	1.169	115.82	12.41	0.623
TQFP	48	PHP	29.11	1.14	0.429	64.42	1.14	1.262	108.71	18.18	0.511
	52	PGP	21.61	0.38	0.192	42.58	0.38	0.391	77.15	7.83	0.353
	64	PBP	17.46	0.12	0.155	28.04	0.12	0.252	52.21	3.12	0.267
	64	PAP	21.47	0.38	0.19	42.20	0.38	0.386	75.83	7.80	0.347
	80	PFP	19.04	0.17	0.174	31.52	0.17	0.29	57.75	4.20	0.297
	100	PZP	17.28	0.12	0.154	27.32	0.12	0.247	49.17	3.11	0.252
	128	PNP	17.17	0.12	0.152	27.07	0.12	0.244	48.39	3.11	0.248
LQFP	144	PRP	15.68	0.13	0.199	27.52	0.13	0.346	47.34	4.62	0.288
	176	PTP	14.52	0.10	0.17	24.46	0.10	0.28	42.95	3.67	0.257
	160	PSP	11.14	0.10	0.14	22.40	0.10	0.266	43.93	3.70	0.262
	208	PYP	10.96	0.10	0.139	21.48	0.10	0.258	39.18	3.66	0.235

General

Thermal modeling is used to estimate the performance and capability of IC packages. From a thermal model, design changes can be made and thermally tested before any time is spent on manufacturing. It can also be determined what components have the most influence on the heat dissipation of a package. Models can give an approximation of the performance of a package under many different conditions. In this case, a thermal analysis was performed in order to approximate the improved performance of a PowerPAD thermally enhanced package to that of a standard package.

Modeling Considerations

There are only a few differences between the thermal models of the standard packages and models for PowerPAD. The geometry of both packages was essentially the same, except for the location of the lead frame bond pad. The pad for the thermally enhanced PowerPAD package is deep downset, so its location is further away from the lead fingers than a standard package lead frame pad. Both models used the maximum pad and die size possible for the package, as well as using a lead frame that had a gap of one lead frame thickness between the pad and the lead fingers. The lead frame thickness was:

TQFP/LQFP: 0.127 mm, or 5 mils
TSSOP/TVSOP/SSOP: 0.147 mm, or 5.8 mils

In addition, the board design for the standard package is different than the PowerPAD. One of the most influential components on the performance of a package is board design. In order to take advantage of PowerPAD's heat dissipating abilities, a board must be used that acts similarly to a heat sink and allows for the use of the exposed (and solderable) deep downset pad. This is Texas Instruments' recommended board for PowerPAD (see

Figure 13). A summary of the board geometry is included below.

Texas Instruments Recommended Board for PowerPAD

0.062" thick

3" x 3" (for packages <27 mm long)

4" x 4" (for packages >27 mm long)

2 oz. copper traces located on the top of the board (0.071 mm thick)

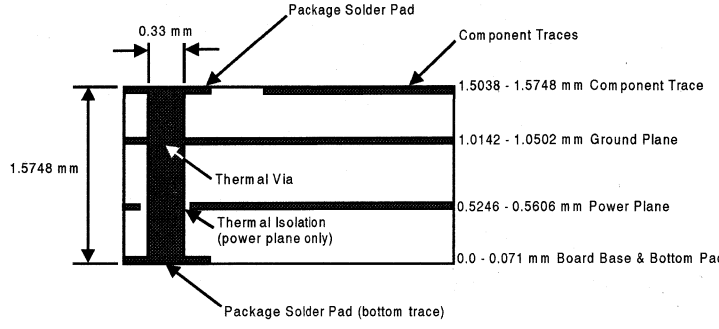
Copper areas located on the top and bottom of the PCB for soldering

Power and ground planes, 1 oz. copper (0.036 mm thick)

Thermal vias, 0.33 mm diameter, 1.5 mm pitch

Thermal isolation of power plane

Figure 13. Texas Instruments Recommended Board (Side View)



The standard packages were placed on a board that is commonly used in the industry today, following the JEDEC standard. It does not contain any of the thermal features that are found on the Texas Instruments recommended board. It only has component traces on the top of the board. A summary of the standard is located below:

JEDEC Low Effective Thermal Conductivity Board (Low-K)

0.062" thick

3" x 3" (for packages <27 mm long)

4" x 4" (for packages >27 mm long)

1 oz. copper traces located on the top of the board (0.036 mm thick)

These boards were used to estimate the thermal resistance for both PowerPAD and the standard packages under many different conditions. While the PowerPAD can be used on a JEDEC low-k board, in order to achieve the maximum thermal capability of the package, it is recommended that it be used on the Texas Instruments heat dissipating board design. It allows for the exposed pad to be directly soldered to the board, which creates an extremely low thermal resistance path for the heat to escape.

A general modeling template was used for each PowerPAD package, with variables dependent on the package size and type. The package dimensions and an example of the template used to model the packages are shown in Figure 14 and Table 7. While only 1/4 of the package was modeled (in order to simplify the model and to lessen the calculation time), the dimensions shown are those for a full model.

Figure 14. Thermal Pad and Lead Attachment to a PCB Using the PowerPAD Package

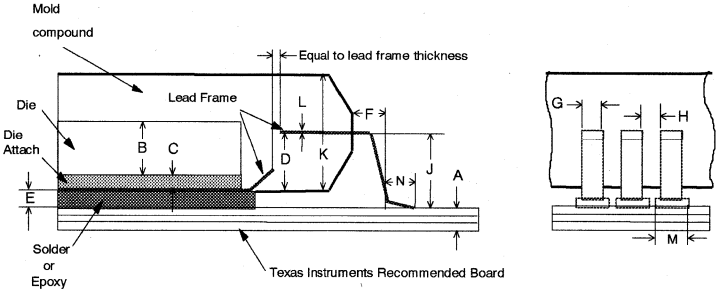


Table 7. PowerPAD Package Template Description

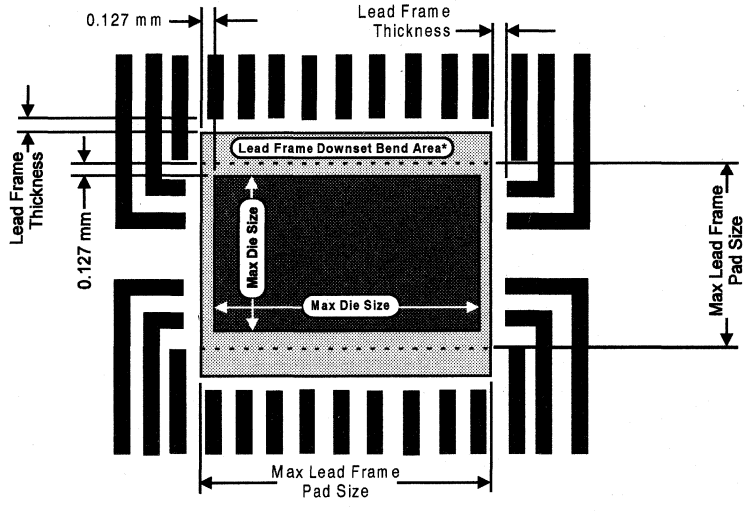
(A)	PCB Thickness:	1.5748 mm	(K)	Package Thickness:	(3)
	PCB Length:	76.2 mm (1)		Package Length:	(3)
	PCB Width:	76.2 mm (1)		Package Width:	(3)
(B)	Chip Thickness:	0.267 mm	(L)	Pad Thickness:	0.147 mm (8)
	Chip Length:	(2)		Pad Length:	(3)
	Chip Width:	(2)		Pad Width:	(3)
(C)	Die Attach Thickness:	0.0127 mm		PCB Trace Length:	25.4 mm
(D)	Lead Frame Downset:	(3)		PCB Trace Thkn:	0.071 mm
	Tie Strap Width:	(3)		PCB Backplane Th:	0.0 mm (4)
(E)	PCB to Package Bottom:	0.09 mm		PCB Trace Width:	0.254 mm
(G)	Shoulder Lead Width:	(3),(5),(6)	(M)	Foot Width:	(5)
(H)	Shoulder Lead Space:	(3),(6)	(N)	Foot Length on PCB:	(3)
(J)	Shoulder to PCB Dist.:	(7)			

Notes: 1) 99.6mm for packages > 27mm max length
2) Chip size is 10 mils smaller than the largest pad size (5 mils from each side)
3) Dependent on package size and type
4) The recommended board requires the addition of two internal copper planes, solder pads, and thermal vias
5) Foot width was set equal to shoulder lead width for model efficiency
6) Lead pitch is equal to the shoulder lead width plus the shoulder lead space (pitch = G + H)

7) The shoulder to board distance is equal to the downset plus the board to package bottom distance (J = D + E)
8) The pad thickness for TQFP/LQFP is equal to 0.127 mm
9) All dimensions are in millimeters.

In addition to following a template for the dimensions of the package, a simplified lead frame was used. A description of the lead frame geometry is seen in Figure 15.

Figure 15. General Leadframe Drawing Configuration



NOTE:
The lead frame downset bend area = 20 mils (lead frame thickness). For SSOP, TSSOP, and TVSOP packages, add the bend area to the width of the pad. For TQFP and LQFP, add the bend area to both the width and length of the pad.

Results

The purpose of the thermal modeling analysis was to estimate the increase in performance that could be achieved by using the PowerPAD package over a standard package. For this package comparison, several conditions were examined:

Case 1. PowerPAD soldered to the TI recommended board

Case 2. PowerPAD not soldered to the TI recommended board

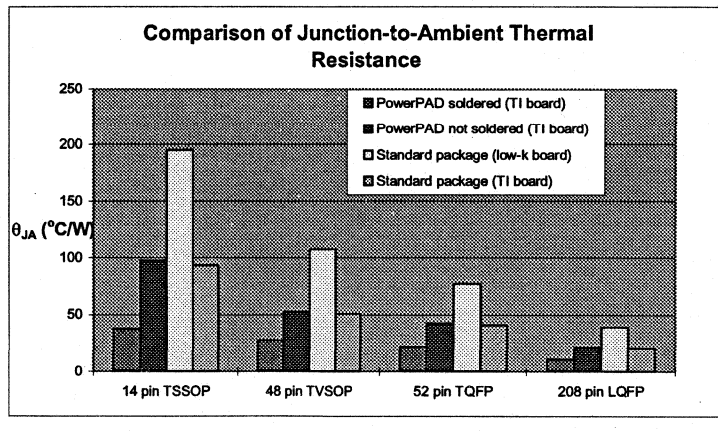
Case 3. A standard package configuration on a low-k board

Case 4. A standard package on the TI recommended board

The first three cases show a comparison of PowerPAD packages on the recommended board to standard packages on a board commonly used in the industry. The results are shown in Table 6. From these results, it was shown that the PowerPAD, when soldered to the TI recommended board, performed an average of 47% cooler than when not soldered, and 73% cooler than a standard package on a low-k board.

For the final case, a separate analysis was performed in order to show the difference in thermal resistance when the standard and the thermally enhanced packages are used on the same board. The results showed that the PowerPAD, when soldered, performed an average of 44% cooler than the standard package (See Figure 18).

Figure 18. Comparison of θ_{JA} for Various Packages

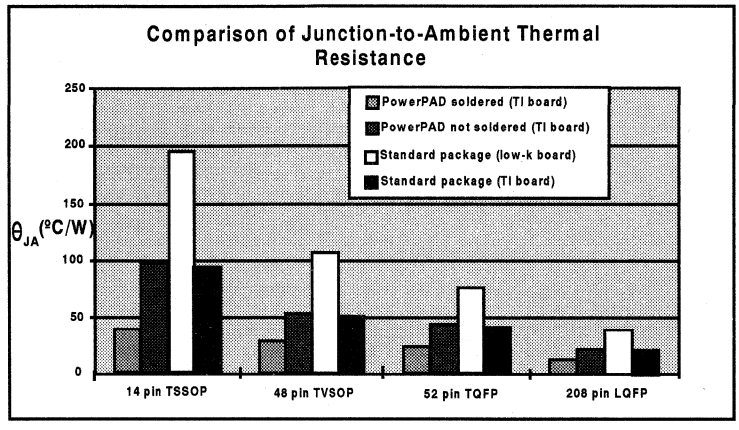


However, when the PowerPAD is not soldered to the board, similar to a standard package, the θ_{JA} is approximately 3% hotter than a standard package. This is due to the location of the lead frame pad relative to the lead fingers, which is the strongest conduction path in a standard package. Since the pad on a standard package lead frame is closer to the lead fingers, more heat is dissipated through the leads than in the PowerPAD package with its deep downset pad.

Conclusions

The deep downset pad of a PowerPAD package allows for an extensive increase in package performance. Standard packages are limited by using only the leads to transport a majority of the heat away. The addition of a heat sink will improve standard package performance, but greatly increases the cost of a package. The PowerPAD package improves performance, but maintains a low cost. The results of the thermal analysis showed that by soldering the PowerPAD package directly to a board designed to dissipate heat, thermal performance increased approximately 44% over the standard packages used on the same board.

Figure 18. Comparison of θ_{JA} for Various Packages



However, when the PowerPAD is not soldered to the board, similar to a standard package, the θ_{JA} is approximately 3% hotter than a standard package. This is due to the location of the lead frame pad relative to the lead fingers, which is the strongest conduction path in a standard package. Since the pad on a standard package lead frame is closer to the lead fingers, more heat is dissipated through the leads than in the PowerPAD package with its deep downset pad.

Conclusions

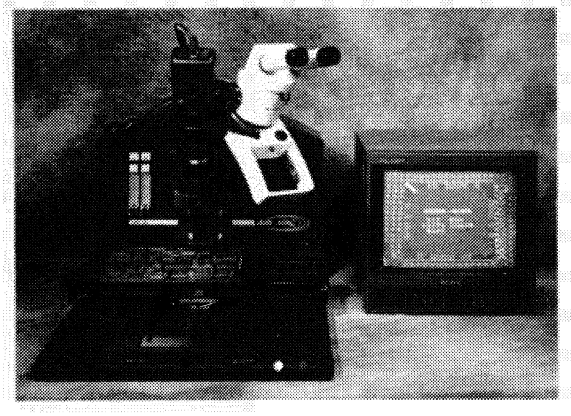
The deep downset pad of a PowerPAD package allows for an extensive increase in package performance. Standard packages are limited by using only the leads to transport a majority of the heat away. The addition of a heat sink will improve standard package performance, but greatly increases the cost of a package. The PowerPAD package improves performance, but maintains a low cost. The results of the thermal analysis showed that by soldering the PowerPAD package directly to a board designed to dissipate heat, thermal performance increased approximately 44% over the standard packages used on the same board.

Appendix B. Rework Process for Heat Sink TQFP and TSSOP PowerPAD Packages - from Air-Vac Engineering

Introduction

The addition of bottom side heat sink attachment has enhanced the thermal performance of standard surface mounted devices. This has presented new process requirements to effectively remove, redress, and replace (rework) these devices due to the hidden and massive heat sink, coplanarity issues, and balance of heat to the leads and heat sink. The following is based on rework of the TQFP100 and TSSOP20/24 pin devices.

Figure 19. DRS22C Reworking Station

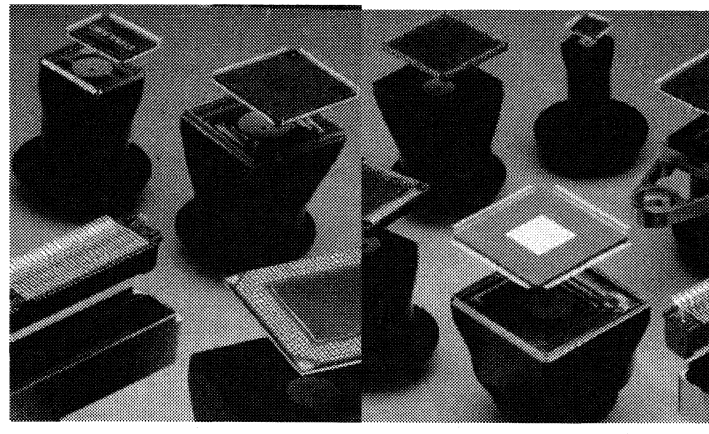


Equipment

The equipment used was the Air-Vac Engineering DRS22C hot gas reflow module. The key requirements for the heat sink applications include: stable PCB platform with sufficient bottom side preheat, alignment capabilities, very accurate heat control, and proper nozzle design.

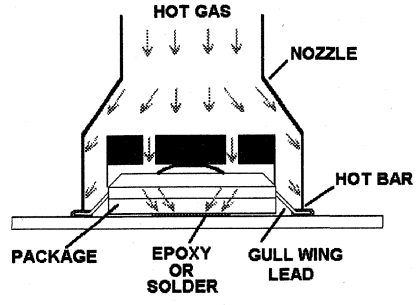
PCB support is critical to reduce assembly sagging and to provide a stable, flat condition throughout the process. The robust convection-based area heater provides sufficient and accurate bottom side heat to reduce thermal gradient, minimize local PCB warpage, and compensate for the heat sink thermal characteristics. The unique pop-up feature allows visible access to the PCB with multiple easy position board supports.

Figure 20. Reworking Nozzles of Various Sizes



During removal, alignment, and replacement, the device is held and positioned by a combination hot gas/hot bar nozzle. Built-in nozzle tooling positions the device correctly to the heat flow. A vacuum cup holds the component in place. Hot gas is applied to the top of the device while hot gas/hot bar heating is applied to the component leads. The hot bar feature also insures bonding of the fine pitch leads.

Figure 21. Nozzle Configuration



Profile

The gas temperature, flow, and operator step-by-step instructions are controlled by an established profile. This allows complete process repeatability and control with minimal operator involvement. Very accurate, low gas flow is required to insure proper temperature control of the package and to achieve good solder joint quality.

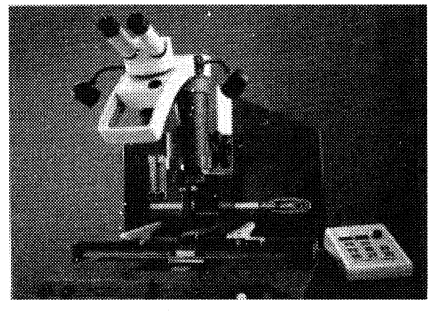
Removal

The assembly is preheated to 75 °C. While the assembly continued to preheat to 100 °C, the nozzle is preheated. After the preheat cycle, the nozzle is lowered and the device is heated until reflow occurs. Machine settings: TSSOP 20/24 - 220 °C at 0.39 scfm gas flow for 50 seconds (preheat) above board level, 220 °C at 0.39 scfm for 10 seconds. TQFP 100 - 240 °C at 0.10 scfm for 60 seconds (preheat) above board level, 250 °C at 0.65 scfm for 15 seconds. The built in vacuum automatically comes on at the end of the cycle and the nozzle is raised. The time to reach reflow was approximately 15 seconds. The component is released automatically allowing the part to fall into an appropriate holder.

Site Redress

After component removal the site must be cleaned of residual solder. This may be done by vacuum desoldering or wick. The site is cleaned with alcohol and lint-free swab. It is critical that the heat sink area be flat to allow proper placement on the leads on new device. Stenciling solder paste is the preferred method to apply new solder. Solder dispensing or reflowing the solder bumps on the pads for the leads may also be an alternative, but reflow (solid mass) of solder to the heat sink is not.

Figure 22. Air-Vac Vision System



Alignment

A replacement device is inserted into the gas nozzle and held by vacuum. The device is raised to allow the optical system to be utilized. The optical system used for alignment consists of a beam-splitting prism combined with an inspection quality stereo microscope or camera/video system. the leads of the device are superimposed over the corresponding land pattern on the board. This four sided viewing allows quick and accurate operator alignment.

Replacement

Once aligned, the x/y table is locked and the optical system retracts away from the work area. The preheat cycle is activated. The device is then lowered to the board. An automatic multi-step process provides a controlled reflow cycle with repeatable results. Machine settings for TSSOP 20/24: 160 °C at 0.39 scfm gas flow for 40 seconds (preheat), 220 °C at 0.39 scfm for 60 seconds above board level, 220 °C at 0.39 scfm for 10 seconds. For TQFP 100: 100 °C at 0.78 scfm for 40 seconds (preheat), 240 °C at 0.10 scfm for 90 seconds above board level, 250 °C at 0.65 scfm for 15 seconds (2 stages).

Conclusion

Rework of heat sink devices, TQFP and TSSOP, can be successful with attention to the additional issues they present. With respect to proper thermal profiling of the heat sink, die, and lead temperatures, the correct gas nozzle and profile can be developed to meet the requirements of the device and assembly. Existing equipment and nozzle design by Air-Vac can provide the tools and process knowledge to meet the heat sink TQFP and TSSOP rework application.

Appendix C. PowerPAD Process Rework Application Note from Metcal

The following report references six of Texas Instruments' fine pitch, surface mount prototype packages (TSOP20, TSOP56, TSOP24, TQFP100, and TQFP64). The shapes and sizes are not new to the circuit board industry. Normally, I would use Metcal conduction tools to simply remove and replace these components. However, these packages are unique because all packages include a 'dye lead' on the underside of the package. This dye lead cannot be accessed by contact soldering. Therefore, convection rework methods are necessary for component placement.

NOTE:
Conduction tools can be used for removal. But, convection rework techniques are required for placement, and recommended for removal.)

Removal

Conduction (optional): All packages can be removed with Metcal conduction tips. Use the following tips:

Component	Metcal Tip Cartridge	OK Nozzle
TSOP20	SMTC-006	N-S16
TSOP56	SMTC-166	N-TSW32
TSOP24	SMTC-006	N-S16
TQFP100	SMTC-0118	N-P68
TQFP64	SMTC-112	N-P20

The dye lead, which is not in contact with the Metcal tip, will easily reflow as heat passes through the package.

Conduction Procedure

1) Tin the tip, contact all perimeter leads simultaneously, and wait 3-5 seconds for the leads to reflow.

2) Lift the package off the board (surface tension will hold it in the tip cartridge). Dislodge the component from the tip by wiping the tip cartridge on a damp sponge.

Convection Procedure

1) Flux the leads. Preferably, use a liquid RMA/rosin flux. Pre-heat the board at 100C. Use a convection or IR preheater, like the SMW-2201 from OK Industries. The settings 2-4 will generally heat a heavy board to 100° in 60 seconds.

2) Remove the component with the OK Industries FCR hot air system. Use a nozzle that matches the size and shape of the component (see above). With the preheat still on, heat the top of the board for 30-45 seconds on a setting of 3-4 (depending on board thickness and amount of copper in board*).

Since convection is NECESSARY for placement, convection is recommended for removal.

Placement Procedure

1) Pads can be tinned by putting solder paste on the pads and reflowing with hot air. Simply apply a fine bead of solder paste (pink nozzle, 24AWG) to the rows of pads. Be sure to apply very little paste. Excessive paste will cause bridging, especially with fine pitch components.

2) Once the pads are tinned, apply gel flux (or liquid flux) to the pads. RMA flux is preferable. Be sure to apply gel flux to the dye pad as well. It is important that your pads not be OVER tinned. If too much solder has formed on the dye pad, the component will sit above the perimeter leads, causing co-planarity problems. The gel flux is tacky and helps with manual placement. The joints require very little solder, so stenciling is not necessary. The pads are so thin that a minimal amount of solder is needed to form a good joint. Use a hot air nozzle for the FCR system. Pre-heat the board and (setting 3-5). Use low air flow (5-10 liters/minute) and topside heat (setting 3-4) for about 30-45 seconds*.

NOTES:

The quality of the dye lead's solder joint cannot be visually inspected. An X-ray machine, cross sectioning, or electrical testing will be required.

The vias on the test board are not solder masked very well which causes some bridging and solder wicking.

*Specific board and component temperatures will vary from board to board and from nozzle to nozzle. Larger nozzles require a higher setting because the heat must travel farther away from the heat source. There will be a slight convection cooling effect from pushing hot air through long flutes, and depending on how wide the nozzle is. However, as a rule, keep the board temperature at 100 °C (as thermocoupled from the TOP). You can regulate the board temperature by setting the temperature knob on the bottom side pre-heater. Apply a HIGHER topside heat from the FCR heating head. As a rule, use a maximum of 200-210°C for a short peak period (10 seconds). Look for the flux to burn off. For board profiling purposes, you can visually inspect the condition of the solder joints during the removal process. Note the time allotted for reflow and set the system to Auto Remove or Auto Place at the same time designation for good repeatability. Be sure not to overheat the joints. Excessive heat can cause board delamination and discoloration. Alignment will 'self-correct' once all the solder has reflowed. Tap board lightly. Remove any solder bridges with solder braid. Also, limit the board's heating cycles to a minimum. Excessive heat shock may warp the board or cause cracking in the solder joints.

Understanding Basic Analog – Active Devices Application Report

By Ron Mancini

Literature Number: SLOA026
July 1999

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Contents

List of Figures

Understanding Basic Analog – Active Devices

By Ron Mancini

ABSTRACT

This application report describes active devices and their use as the basic building blocks of all electronic equipment. Active devices, coupled with passive devices, create the combination needed to fulfill all circuit requirements. A select few active devices are discussed in this report.

Introduction

Active devices have gain, thus they have transfer functions which are not available to passive devices. Active devices are considerably more complicated than passive devices; hence, their models and transfer equations are more complicated than those of passive devices. Active devices are the foundation on which all electronics equipment is built. Integrated circuits and higher forms of electronic components are built from the active devices discussed here.

Bipolar Junction Transistor

The bipolar junction transistor (BJT) was the first active semiconductor device manufactured; therefore, it became the workhorse of the semiconductor industry. When the field effect transistor (FET) manufacturing process was perfected, it began competing with the BJT. Since then, the FET has been taking sockets from the BJT, but there are many applications, such as high frequency amplifiers, where the BJT still excels. Also, the BJT manufacturing process can be simple and inexpensive, and this, coupled with the BJT's long list of captured sockets, insures that the BJT will be around for a long time.

BJT transistors are made from a silicon bar that has three areas that are doped differently to produce the transistor. Doping means that the base semiconductor material has charged atoms added to change its polarity. These three areas are called the base, emitter, and collector. The emitter and collector are doped to have the same polarity which can be positive or negative, and the base is doped to have the opposite polarity. The BJT, like most transistors, come in two types called NPN or PNP. P stands for positive, N stands for negative, and the positive or negative regions gain their name from the doping of the semiconductor material making up the base, collector, and emitter areas of the BJT. An NPN transistor has a positively doped base and a negatively doped collector and emitter.

An NPN transistor looks like two diodes with the anodes connected together (see Figure 1). The point where the anodes connect is called the base, one cathode is called the collector, and the other cathode is called the emitter. Although this illustration does not work with discrete diodes, it is fact in a BJT because when the width of the base junction is decreased enough, the back-to-back diodes function as a transistor. Using the back-to-back diode model, transistors are commonly checked for short circuits and open circuits with an ohmmeter. The base-emitter and base-collector junctions of a BJT act like forward biased diodes when the positive ohmmeter lead is connected to the base while the negative ohmmeter is connected to the emitter or collector. It looks like a reverse biased diode when the lead connections are reversed.

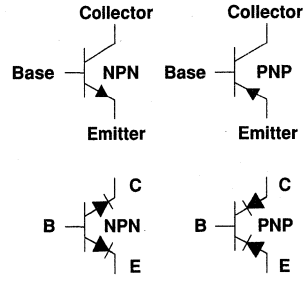

Figure 1. BJT Description

The model of a BJT is shown in Figure 2. The input circuit looks like a forward biased diode; the input impedance equation is $Z_{IN} = r_e = I_C/26$. The base-emitter junction must be forward biased, thus there is a forward voltage drop of V_{BE}. V_{BE} is approximately 0.6 volts in a silicon transistor, and 0.2 volts in a germanium transistor. The input current is called I_{base} or I_B.

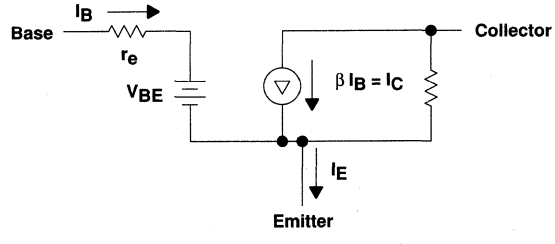

Figure 2. BJT Model

Since the collector-base junction is reverse biased, the collector current flows from the collector to the emitter. The collector current equation is $I_C = \beta(I_B)$ where β is the current gain of the transistor, and the emitter current equation is $I_E = I_C + I_B$. The impedance of the collector-emitter junction is called r_c, and r_c is very a high value (in the MΩ range). Current gain and the forward voltage drop are a function of the manufacturing process, temperature, and device physics, hence they are not stable parameters. Therefore, BJT circuits that depend on β and V_{BE} are not stable; thus, in well designed BJT circuits, the external components stabilize these parameters with feedback. This is not a drawback with just BJTs; this same condition exists for all transistors.

Junction Field Effect Transistor

The junction field effect transistor is called the JFET, and it comes in two flavors, p-channel and n-channel. It has high input impedance, so it is often used in the input circuit of amplifiers. The JFET has a high bandwidth, but circuit topologies and parasitic capacitors prevent it from achieving the same high bandwidth circuits where the BJT excels. Very often, the JFET is used as the input stage to achieve high input impedance. The JFET can achieve high bandwidth when its output is limited to small signal swings which are characteristic of input circuits. JFETs and BJTs can be made simultaneously on a semiconductor process called BIFET, thus they are often combined to make a high input impedance, high bandwidth amplifier. The JFET output impedance is high in the off state and low in the on state.

The JFET can be visualized as a bar of doped silicon that has a diode junction made in the middle of the bar. If the silicon bar is doped N, the JFET is called an N-channel device. Figure 3 shows the symbols for n-channel and p-channel JFETs. When the n-channel gate is negative with respect to the source the diode is biased off, the bar is depleted of carriers, and the source to drain resistance is quite high (several MΩ). When the n-channel gate is biased positive with respect to the source, the diode is biased on, and the bar is flooded with carriers thus causing a low source to drain resistance (as low as mΩ). The converse is true for a p-channel JFET.

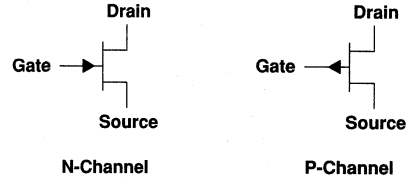

Figure 3. JFET Description

The linear JFET model is shown in Figure 4. When the JFET is biased in its linear region, the gate is represented as an open circuit because the input diode is reverse biased. The drain to source current is a voltage controlled current source, $g_m(e_g)$. The output resistance is modeled by R_O. As long as the signal swings stay in the linear region, the gate-source voltage signal swing induces a drain-source current flow. Again, as is the case with the BJT, the key parameters of the JFET such as gain are temperature and drift sensitive, so feedback is used to make JFET circuits dependent on stable passive components.

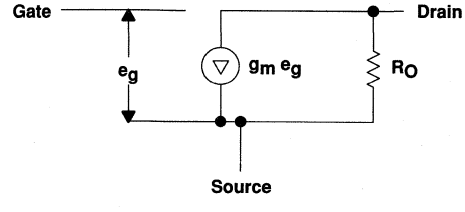

Figure 4. JFET Model

Metal Oxide Semiconductor Field Effect Transistors

The BJT and JFET have a diode in their input circuit which controls their mode of operation. The metal oxide semiconductor field effect transistor (MOSFET) works on a similar principle, but the diode is buried within the MOSFET. The MOSFET input diode is controlled by an electric field in the gate region, thus the input impedance is always extremely high because there is no forward biased diode to lower the input impedance. The input impedance of MOSFETs is so high that there is no mechanism that readily bleeds off the accumulated charge except for humidity, thus they are often packaged with lead shorting wires to drain the charge. The lead shorting devices protect the MOSFETs from charge buildup and the subsequent catastrophic discharge current. All semiconductor devices should be protected from static discharge, but MOSFETs are the most liable to build up a killing charge. Do not be lax with static protection because some sensitive BJTs are affected by only a few hundred volts static discharge.

The MOSFET is a majority carrier device, and because majority carriers have no recombination delays, the MOSFET achieves extremely high bandwidths and switching times. The gate is electrically isolated from the source, and while this provides the MOSFET with its high input impedance, it also forms a good capacitor. Driving the gate with a dc or a low frequency signal is a snap because Z_{IN} is so high, but driving the gate with a step signal is much harder because the gate capacitance must be charged at the signal rate. This situation leads to a paradox; the high input impedance MOSFET must be driven with a low impedance driver to obtain high switching speeds and low bandwidth.

MOSFETs do not have a secondary breakdown area, and their drain-source resistance has a positive temperature coefficient, so they tend to be self protective. These features, coupled with the very low on resistance and no junction voltage drop when forward biased, make the MOSFET an extremely attractive power supply-switching transistor.

The MOSFET (see Figure 5 for a description) can be visualized as a bar of doped silicon that contains a capacitively coupled diode junction in the middle of the bar. If the silicon bar is doped N, then the MOSFET is called an N-channel device. When the n-channel gate is charged negative with respect to the source the internal gate diode is biased off, the bar is depleted of carriers, and the source to drain resistance is quite high (several hundred MΩ). When the n-channel gate is charged positive with respect to the source, the internal gate diode is biased on, and the bar is flooded with carriers thus causing a low source to drain resistance (in the low mΩ range). The converse is true for a P-channel MOSFET.

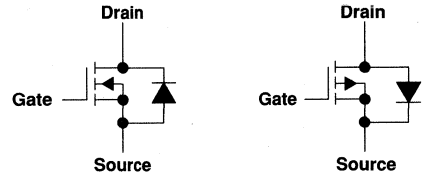

Figure 5. MOSFET Description

The linear MOSFET model is shown in Figure 6. When the MOSFET is biased in its linear region, the gate appears as an open circuit to dc. The drain to source current is derived from a voltage controlled current source, $g_m(e_g)$. The output resistance is modeled by R_O. As long as the signal swings stay in the linear region, gate-source voltage signals induce a drain-source current.

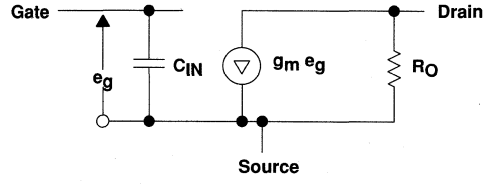

Figure 6. MOSFET Model

The MOSFET contains a diode connected across from the drain (cathode) to the source (anode). This diode is not forward biased during normal operation, consequently it does not conduct current during normal operation. When the MOSFET is connected to an inductive load, the inductive kick causes the diode to turn on and conduct current. In some modes of operation, this is a desired effect because it limits the inductive voltage rise. The diode is not a fast turn-off diode, so it consumes quite a bit of power during turn-off. The turn-off power consumption is detrimental in some circuits, thus those circuits must put a diode with a smaller forward voltage drop (Schottky diode) in parallel with the body diode.

C_{IN} can be as large as several hundred pF, and it must be charged by the gate signal. When the MOSFET is used in a power switching application, the gate is normally driven by a low impedance driver so that C_{IN} can be charged quickly. If C_{IN} is charged slowly, the switching time of the MOSFET is long causing the MOSFET to stay in the linear region for a long time. When the MOSFET operates in the linear region, its voltage drop and current flow are high, resulting in high power dissipation.

Again, as is the case with the BJT, the key parameters of the MOSFET such as gain are temperature and drift sensitive, so feedback is used to make MOSFET circuits dependent on stable passive components.

Voltage Feedback Operational Amplifier

The voltage feedback operational amplifier (VF op amp), or op amp as it is affectionately known, is a versatile amplifier which requires feedback to function. The op amp gain is so high that the output saturates on any differential input signal, so feedback is employed to lower the closed loop gain. The feedback makes the op amp circuit a precision circuit because the closed loop gain is dependent on the passive components which can be very accurate. Some op amp parameters, such as input offset voltage can still degrade precision, but there are specially designed precision op amps that have very low input offset voltages (micro volts), and selected salient parameters chosen to yield a precision circuit. The differential input structure of op amp enhances precision because the transistors in both inputs can be matched.

Op amp bandwidth depends on the process used to make the op amp, and BJT op amps have the highest bandwidth and current drain, with JFET op amps are next highest, and MOSFET op amps have the lowest bandwidth and current drain. Voltage feedback op amps are discussed in this section, and their bandwidth starts rolling off at low frequencies (about five decades before the advertised gain–bandwidth point.

The input impedance of the op amps is very high, and their output impedance is relatively low, thus they are ideal for configuring many different circuits. Some of the possible circuits op amps make are inverting amplifiers, noninverting amplifiers, differential amplifiers, summing amplifiers, and integrating amplifiers. The op amp model is shown in Figure 7. The input impedance of op amps is very high, and it is often modeled as an open circuit. The output circuit consists of a voltage controlled voltage source, and the control voltage is the differential voltage applied across the inputs.

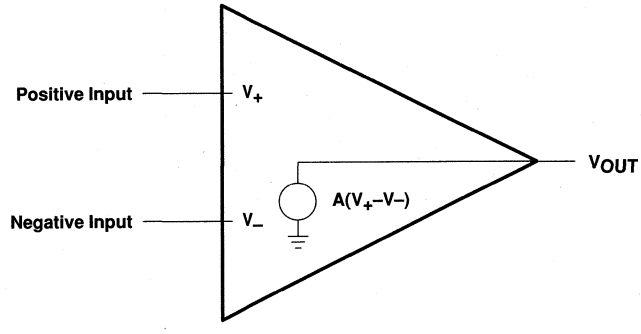

Figure 7. Voltage Feedback Op Amp Model

Op amps are always surrounded with passive components, which are required to program the gain and add stability.

Current Feedback Operational Amplifiers

Current feedback op amps, called CFA for current feedback amplifier, are also called op amps, hence there can be confusion about which type of op amp (voltage or current feedback) is under discussion. It is assumed that voltage feedback op amps are being discussed unless a reference is made to the current feedback op amp (CFA).

The CFA configuration makes it hard to achieve precision because there is a buffer tied across the inputs. The input structure of a CFA is not matched, hence it is hard to obtain dc precision, which requires a matched input structure (usually a differential amplifier is used when matching is required). The applications for CFAs generally do not require high precision because CFAs are used in high frequency circuits. In many high frequency circuits, the dc portion of the signal contains little or no information, thus precision is not paramount in these applications.

CFAs are usually made with BJTs because they yield very high bandwidths. The high bandwidth of a CFA does not start rolling off till much higher frequencies (several decades higher) than a VFA does, but it rolls off at a much faster rate. CFA have bandwidths in the GHz range while VFA bandwidths are down in the several hundred MHz range. The input impedance of CFAs is high for the positive input and low for the negative input because of the input voltage buffer.

The CFA model is shown in Figure 8. The positive input is a voltage buffer input, so the positive input has very high input impedance. The negative input is connected to the output of the same voltage buffer, hence the negative input impedance is close to zero. It is very hard to match parameters between the inputs because they are connected to different ends of a buffer, and this situation makes it hard to build precision CFAs.

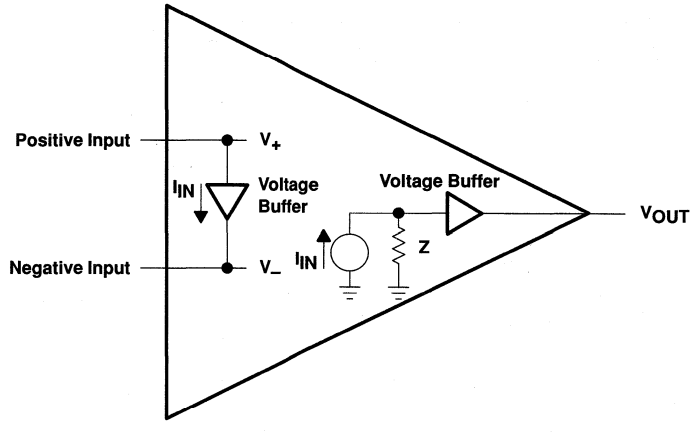

Figure 8. Current Feedback Op Amp Model

The output circuit contains a transimpedance stage, Z, so the error current which flows through the input stage I_{IN} is multiplied by Z to form a voltage. This voltage is buffered before it becomes the output voltage, thus the CFA has very low output impedance.

Voltage Comparators

The voltage comparator is used to convert an analog signal to a digital signal. This is usually accomplished by connecting a reference to the negative comparator input and a signal to the positive comparator input. When the signal exceeds the reference the output goes from a low voltage (a logic zero) to a high voltage (a logic one). Inverted operation can be obtained with a comparator by reversing the inputs.

The input stage of a comparator is similar to an op amp input stage. The differential input voltage is multiplied by the gain to obtain an output signal. The comparator gain is very large, and it is not limited by feedback, so the output would saturate if it was an op amp. The difference is that the comparator has an output stage that reaches a limit but does not saturate. The comparator's ability to run open loop without saturating separates it from the op amp which always saturates when it runs open loop. Never use op amps for a comparator function when propagation delay is important, because when an op amp saturates, the time needed for it to come out of saturation is unpredictable.

The voltage comparator is shown in Figure 9. The voltage comparator input stage is identical to a VF op amp input stage, consequently the comparator input impedance is very high. The inputs can be matched very well, thus comparators are capable of doing precision work. The voltage comparator output stage looks like a very high open loop gain stage that has its output clamped to the power supply rails. There are other forms of the output stage which have two leads, and they enable the circuit designer to connect the output to two different voltage levels. This type of comparator is useful when the input must sense signals over a wide voltage range including negative voltages, and the output voltage swing must be compatible with a specific logic family.

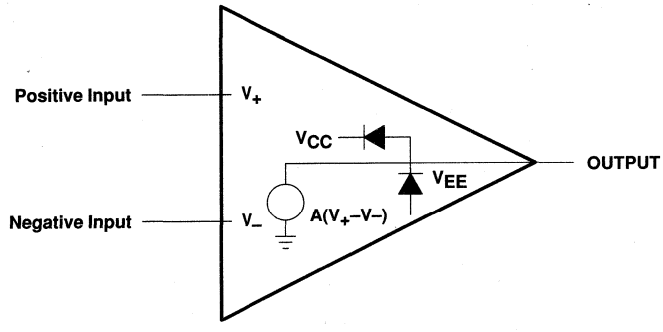

Figure 9. Voltage Comparator Model

Other Active Devices

There are many more active devices than are covered in this application report. The exposure here is limited to the most popular devices, and these devices are adequate to cover the large majority of electronic equipment applications.

Specialty fields like power supplies, motor controls, data transmission, etc. have active devices not shown here. Rather than turn this application report into a two hundred-page collection of active devices, 99 percent of which are of little or no interest to the average reader, the author chose to ignore 99 percent. If you have a need for further information on an active device, mentioned or not mentioned here, contact the manufacturer. For example, if you contact the local TI sales office or the factory in Dallas, and ask for information on current feedback op amps, TI will send you information gratis. If you contact the local analog field specialist, they will see that you are sent data sheets and applications literature.

This application note is purposely kept brief, but the manufacturer's support system is more than happy to flood you with information. If you can't get information from a manufacturer, maybe you are talking to the wrong manufacturer.

Summary

Active devices have gain, so they perform functions that passive devices can't fill. Active devices have voltage, current, and power gain; hence, when active devices are coupled with passive devices the combination fulfills all circuit requirements.

Active devices employ feedback to control the gain, and the feedback makes active devices dependent on passive device parameters. Accept this for now, because later applications will illustrate the concept. Feedback brings its own problems as well as its advantages. Oscillation resulting from misapplied feedback is the major disadvantage of active circuits.

Understanding Basic Analog – Circuit Equations Application Report

By Ron Mancini

Literature Number: SLOA025
July 1999

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Contents

List of Figures

Understanding Basic Analog—Circuit Equations

By Ron Mancini

ABSTRACT

This application report provides a basic understanding of analog circuit equations. Only sufficient math and physics are presented in this application report to enable understanding the concepts.

Introduction

Although this application note tries to minimize math, some algebra is germane to the understanding of analog electronics. Math and physics are presented in this application note in the manner in which they are used later, so no practice exercises are given. For example, after the voltage divider rule is explained, it is used several times in the development of other concepts, and this usage constitutes the practice. This application note builds on each concept after it has been explained, thus, if you want to get familiar with the concepts, read it from beginning to end.

Circuits are a mix of passive and active components. The components are arranged in a manner that enables them to perform some desired function. The resulting arrangement of components is called a circuit or sometime a circuit configuration. The art portion of analog design is designing the circuit configuration. There are many published circuit configurations for almost any circuit task, thus all circuit designers need not be artists.

When the design has progressed to the point that a circuit exists, equations must be written to predict and analyze circuit performance. Textbooks are filled with rigorous methods for equation writing, and this application note does not supplant those textbooks. But, a few equations are used so often that they should be memorized, and these equations are considered here.

There are almost as many ways to analyze a circuit as there are electronic engineers, and if the equations are written correctly, all methods yield the same answer. There are some simple ways to analyze the circuit without completing unnecessary calculations, and these methods are illustrated here.

Laws of Physics

Ohm's law is stated as V=IR, and it is fundamental to all electronics. Ohm's law can be applied to a single component, to any group of components, or to a complete circuit. When the current flowing through any portion of a circuit is known, the voltage dropped across that portion of the circuit is obtained by multiplying the current times the resistance.

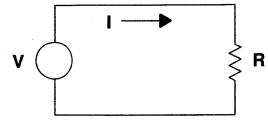


Figure 1. Ohm's Law Applied to the Total Circuit

$$V = IR \tag{1}$$

In Figure 1, Ohm's law is applied to the total circuit. The current, (I) flows through the total resistance (R), and the voltage (V) is dropped across R. In Figure 2, Ohm's law is applied to a single component. The current (I_R) flows through the resistor (R) and the voltage (V_R) is dropped across R. Notice, the same formula is used to calculate the voltage drop regardless of what portion of the circuit the calculation is made on.

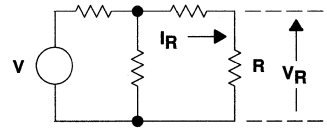


Figure 2. Ohm's Law Applied to a Component

Kirchoff's voltage law states that the sum of the voltage drops in a series circuit equals the sum of the voltage sources. Otherwise, the source (or sources) voltage must be dropped across the passive components. When taking sums keep in mind that the sum is an algebraic quantity.

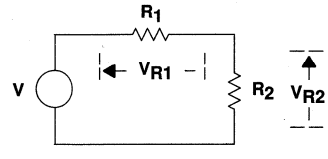


Figure 3. Kirchoff's Voltage Law

$$\sum V_{SOURCES} = \sum V_{DROPS} \tag{2}$$

$$V = V_{R1} + V_{R2} \tag{3}$$

Kirchoff's current law states; the sum of the currents entering a junction equals the sum of the currents leaving a junction. It makes no difference if a current flows from a current source, through a component, or through a wire, because all currents are equal. Kirchoff's law is illustrated in Figure 4.

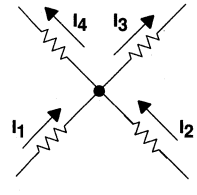


Figure 4. Kirchoff's Current Law

$$\sum I_{IN} = \sum I_{OUT} \quad (4)$$

$$I_1 + I_2 = I_3 + I_4 \quad (5)$$

Voltage Divider Rule

When the output of a circuit is not loaded, the voltage divider rule can be used to calculate the circuit's output voltage. Assume that the same current flows through all circuit elements. Equation 6 is written using Ohm's law as $V = I (R_1 + R_2)$. Equation 7 is written as Ohm's law across the output resistor.

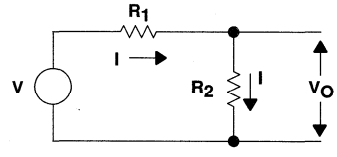


Figure 5. Voltage Divider Rule

$$I = \frac{V}{R_1 + R_2} \quad (6)$$

$$V_D = IR_2 \quad (7)$$

Substituting equation 6 into equation 7, and using algebraic manipulation yields equation 8.

$$V_D = V \frac{R_2}{R_1 + R_2} \quad (8)$$

A simple way to remember the voltage divider rule is that the output resistor is divided by the total circuit resistance. This fraction is then multiplied by the input voltage to obtain the output voltage. Remember that the voltage divider rule always assumes that the output resistor is not loaded; the equation is not valid when the output resistor is loaded by parallel component. Fortunately, most circuits following a voltage divider are input circuits, and input circuits are usually high resistance. When a fixed load is in parallel with the output resistor, the equivalent parallel value comprised of the output resistor and loading resistor can be used in the voltage divider calculations with no error. Many people ignore the load resistor if it is ten times greater than the output resistor value, but this calculation can lead to a 10% error.

Current Divider Rule

When the output of a circuit is not loaded, the current divider rule can be used to calculate the current flow in the output branch circuit (R_2). The currents I_1 and I_2 in Figure 6 are assumed to be flowing in the branch circuits. Equation 9 is written with the aid of Kirchoff's current law. The circuit voltage is written in equation 10 with the aid of Ohm's law. Combining equations 9 and 10 yields equation 11.

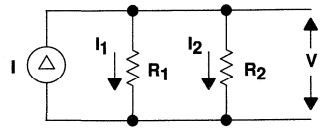


Figure 6. Current Divider Rule

$$I = I_1 + I_2 \tag{9}$$

$$V = I_1R_1 = I_2R_2 \tag{10}$$

$$I = I_1 + I_2 = I_2\frac{R_2}{R_1} + I_2 = I_2\left(\frac{R_1 + R_2}{R_1}\right) \tag{11}$$

Rearranging the terms in equation 11 yields equation 12.

$$I_2 = I\left(\frac{R_1}{R_1 + R_2}\right) \tag{12}$$

The total circuit current divides into two parts, and the resistance (R_1) divided by the total resistance determines how much current flows through R_2. An easy method of remembering the current divider rule is to remember the voltage divider rule. Then modify the voltage divider rule such that the opposite resistor is divided by the total resistance, and the fraction is multiplied by the input current to get the branch current.

Thevenin's Theorem

There are times when it is advantageous to isolate a part of the circuit, and analyze just the isolated part of the circuit. Rather than write loop or node equations for the complete circuit, and solving them simultaneously, Thevenin's theorem enables us to isolate the part of the circuit we are interested in. We then replace the remaining circuit with a simple series equivalent circuit, thus Thevenin's theorem simplifies the analysis.

There are two theorems that do the similar functions, and the second theorem is called Norton's theorem. Thevenin's theorem is used when the input driver is a voltage source, and Norton's theorem is used when the input drive is a current source. Norton's theorem is rarely used, so its explanation is left for the reader to dig out of a textbook if it is ever required.

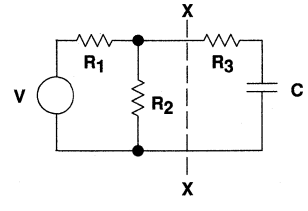


Figure 7. Original Circuit

The rules for Thevenin's theorem start with the component or part of the circuit being replaced. Referring to Figure 7, look into the terminals (point XX in the figure) of the circuit being replaced. Calculate the no load voltage (V_{TH}) as seen from these terminals (use the voltage divider rule). Look into the terminals of the circuit being replaced, short independent voltage sources, and calculate the impedance between these terminals. The final step is to substitute the Thevenin equivalent circuit for the part you wanted to replace.

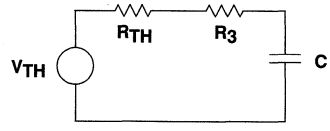
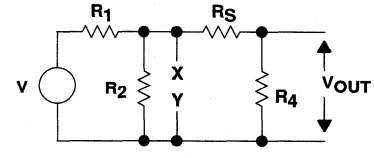


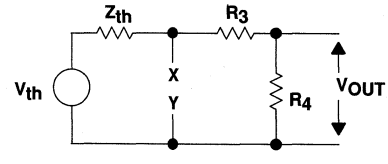
Figure 8. Thevenin's Equivalent Circuit for Figure 7

The Thevenin equivalent circuit is a simple series circuit, thus further calculations are simplified. The simplification of circuit calculations is often sufficient reason to use Thevenin's theorem because it eliminates the need for solving several simultaneous equations. The detailed information about what happens in the circuit that was replaced is not available when using Thevenin's theorem, but that is no consequence because you had no interest in it.

As an example of Thevenin's theorem, let's calculate the output voltage (V_O) shown in Figure 9A. The first step is to stand on the terminals X–Y with your back to the output circuit, and calculate the open circuit voltage seen. This is a perfect opportunity to use the voltage divider rule to obtain equation 13.



(a) The Original Circuit



(b) The Thevenin Equivalent Circuit

Figure 9. Example of Thevenin's Equivalent Circuit

$$V_{TH} = V \frac{R_2}{R_1 + R} \tag{13}$$

Still standing on the terminals X-Y, step two is to calculate the impedance seen looking into these terminals (short the voltage sources). The Thevenin impedance is the parallel impedance of R_1 and R_2 as calculated in equation 14. Now get off the terminals X-Y before you damage them with your big feet. Step three replaces the circuit to the left of X-Y with the Thevenin equivalent circuit V_{TH} and R_{TH}.

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} \tag{14}$$

The final step is to calculate the output voltage. Notice the voltage divider rule is used again. Equation 15 describes the output voltage, and it comes out naturally in the form of a series of voltage dividers, which makes sense. That's another advantage of the voltage divider rule; the answers normally come out in a recognizable form rather than a jumble of coefficients and parameters.

$$V_{OUT} = V_{TH} \frac{R_4}{R_{TH} + R_3 + R_4} = V\left(\frac{R_2}{R_1 + R_2}\right) \frac{R_4}{\frac{R_1 R_2}{R_1 + R_2} + R_3 + R_4} \tag{15}$$

The circuit analysis is done the hard way in Figure 10, so you can see the advantage of using Thevenin's Theorem. Two loop currents, I_1 and I_2, are assigned to the circuit. Then the loop equations 16 and 17 are written.

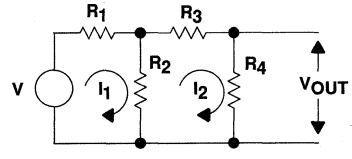


Figure 10. Analysis Done the Hard Way

$$V = I_1(R_1 + R_2) - I_2 R_2 \tag{16}$$

$$I_2(R_2 + R_3 + R_4) = I_1 R_2 \tag{17}$$

Equation 17 is rewritten as equation 18 and substituted into equation 16 to obtain equation 19.

$$I_1 = I_2 \frac{R_2 + R_3 + R_4}{R_2} \tag{18}$$

$$V = I_2 \left(\frac{R_2 + R_3 + R_4}{R_2}\right)(R_1 + R_2) - I_2 R_2 \tag{19}$$

The terms are rearranged in equation 20. Ohm's law is used to write equation 21, and the final substitutions are made in equation 22.

$$I_2 = \frac{V}{\frac{R_2 + R_3 + R_4}{R_2}(R_1 + R_2) - R_2} \tag{20}$$

$$V_{OUT} = I_2 R_4 \tag{21}$$

$$V_{OUT} = V \frac{R_4}{\frac{(R_2 + R_3 + R_4)(R_1 + R_2)}{R_2} - R_2} \tag{22}$$

This is a lot of extra work for no gain. Also, the answer is not in a usable form because the voltage dividers are not recognizable, thus more algebra is required to get the answer into usable form.

Superposition

Superposition is a theorem that can be applied to any linear circuit. Essentially, when there are independent sources, the voltages and currents resulting from each source can be calculated separately, and the results are added algebraically. This simplifies the calculations because it prevents writing a series of loop or node equations.

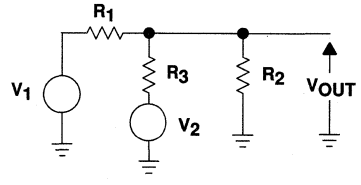


Figure 11. Superposition Example

When V_1 is grounded, V_2 forms a voltage divider with R_3 and the parallel combination of R_2 and R_1. The output voltage for this circuit (V_{OUT1}) is calculated with the aid of the voltage divider equation. The circuit is shown in Figure 12. The voltage divider theorem yields the answer quickly.

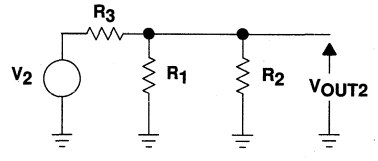


Figure 12. When V_1 is Grounded

$$V_{OUT2} = V_2 \frac{R_1 \parallel R_2}{R_3 + R_1 \parallel R_2} \tag{23}$$

Likewise, when V_2 is grounded, V_1 forms a voltage divider with R_1 and the parallel combination of R_3 and R_2, and the voltage divider theorem is applied again to calculate V_{OUT1}.

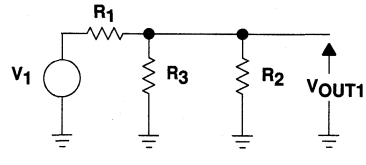


Figure 13. When V_2 is Grounded

$$V_{OUT1} = V_1 \frac{R_2 \parallel R_3}{R_1 + R_2 \parallel R_3} \tag{24}$$

After the calculations for each source are made the components are added to obtain the final solution.

$$V_O = V_1 \frac{R_2 \parallel R_3}{R_1 + R_2 \parallel R_3} + V_2 \frac{R_1 \parallel R_2}{R_3 + R_1 \parallel R_2} \tag{25}$$

The reader should analyze this circuit with loop or node equations to gain an appreciation for superposition. Again, the superposition results come out as a simple arrangement that is easy to understand. One looks at the final equation and it is obvious that if the sources are equal and opposite polarity, and $R_1 = R_3$, then the output voltage is zero. Conclusions such as this are hard to make after the results of a loop or node analysis unless considerable effort is made to manipulate the final equation into symmetrical form.

Calculation of a Saturated Transistor Circuit

The circuit specifications are: when $V_{IN} = 12$ V, $V_{OUT} < 0.4$ V at $I_{SINK} < 10$ mA, and $V_{IN} < 0.05$ V, $V_{OUT} > 10$ V at $I_{OUT} = 1$ mA. The circuit diagram is shown in Figure 14.

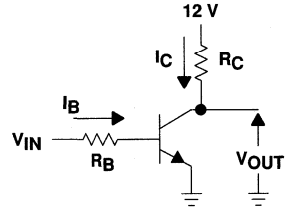


Figure 14. Saturated Transistor Circuit

The collector resistor must be sized when the transistor is off, because it has to be small enough to allow the output current to flow through it without dropping more than two volts.

$$R_C \leq \frac{V_{+12} - V_{OUT}}{I_{OUT}} = \frac{12 - 10}{1} = 2 \text{ K} \tag{26}$$

When the transistor is off, 1 mA can be drawn out of the collector resistor without pulling the collector or output voltage to less than ten volts. When the transistor is on, the base resistor must be sized to enable the input signal to drive enough base current into the transistor to saturate it. The transistor beta is 50.

$$I_C = \beta I_B = \frac{V_{+12} - V_{CE}}{R_C} + I_L \approx \frac{V_{+12}}{R_C} + I_L \tag{27}$$

$$R_B \leq \frac{V_{+12} - V_{BE}}{I_B} \tag{28}$$

Substituting equation 27 into equation 28 yields equation 29.

$$R_B \leq \frac{(V_{+12} - V_{BE})\beta}{I_C} = \frac{(12 - 0.6)50}{\frac{12}{2} + (10)} = 35.6 \text{ K} \tag{29}$$

When the transistor goes on it sinks the load current, and it still goes into saturation. These calculations neglect some minor details, but they are in the 98% accuracy range.

Transistor Amplifier

The amplifier is an analog circuit, and the calculations, plus the points that must be considered during the design, are more complicated than for a saturated circuit. This extra complication leads people to say that analog design is harder than digital design (the saturated transistor is digital i.e.; on or off). Analog design is harder than digital design because the designer must account for all states in analog, whereas in digital only two states must be accounted for. The specifications for the amplifier are an ac gain of four and a peak-to-peak signal swing of 4 volts.

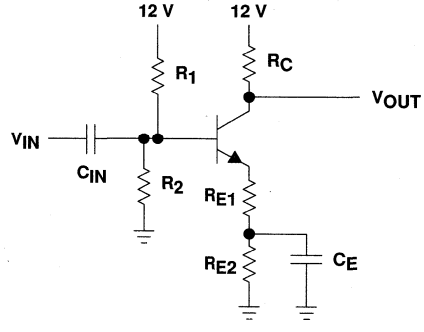


Figure 15. Transistor Amplifier

I_C is selected as 10 mA because the transistor has a current gain (β) of 100 at that point. The collector voltage is arbitrarily set at 8 V; when the collector voltage swings positive 2 V (from 8 V to 10 V) there is still enough voltage dropped across R_C to keep the transistor on. Set the collector-emitter voltage at 4 V; when the collector voltage swings negative 2 V (from 8 V to 6 V) the transistor still has 2 V across it, so it stays linear. This sets the emitter voltage (V_E) at 4 V.

$$R_C \leq \frac{V_{+12} - V_C}{I_C} = \frac{12 - 8}{10} = 400\ \Omega \tag{30}$$

$$R_E = R_{E1} + R_{E2} = \frac{V_E}{I_E} = \frac{V_E}{I_B + I_C} \cong \frac{V_E}{I_C} = \frac{4}{10} = 400\ \Omega \tag{31}$$

Use Thevenin's equivalent circuit to calculate R_1 and R_2 as shown in Figure 16.

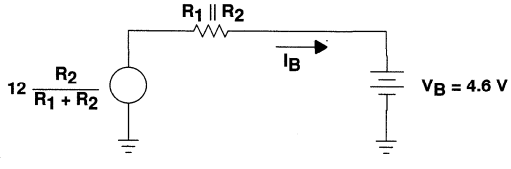


Figure 16. Thevenin Equivalent of the Base Circuit

$$I_B = \frac{I_C}{\beta} = \frac{10\ mA}{100} = 0.1\ mA \tag{32}$$

$$V_{TH} = \frac{12R_2}{R_1 + R_2} \tag{33}$$

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} \tag{34}$$

We want the base voltage to be 4.6 V because the emitter voltage is then 4 V. Assume a voltage drop of 0.4 V across R_{TH}, so equation 35 can be written. The drop across R_{TH} may not be exactly 0.4 V because of beta variations, but a few hundred mV does not matter is this design. Now, calculate the ratio of R_1 and R_2 using the voltage divider rule (the load current has been accounted for).

$$R_{TH} = \frac{0.4}{0.1} K = 4\ K \tag{35}$$

$$V_{Th} - I_B R_{Th} + V_B = 0.4 + 4.6 = 5 = 12 \frac{R_1}{R_1 + R_2} \tag{36}$$

$$R_1 = \frac{7}{5} R_2 \tag{37}$$

R_1 is almost equal to R_2, thus selecting R_2 as twice the Thevenin resistance yields approximately 4 K as shown in equation 35. Hence, R_2 = 11.2 K and R_1 = 8 K. The ac gain is approximately R_C/R_{E1} so we can write equation 38.

$$R_{E1} = \frac{R_C}{G} = \frac{400}{4} = 100\ \Omega \tag{38}$$

$$R_{E2} = R_E - R_{E1} = 400 - 100 = 300\ \Omega \tag{39}$$

The capacitor selection depends on the frequency response required for the amplifier, but 10 μF for C_{IN} and 1000 μF for C_E suffice for a starting point.

Conclusions

The application note presents the minimum number of physics laws and equations required for beginning analog analysis. The laws and equations are simple, but when applied correctly, they are powerful. As you proceed further into the realm of analog analysis or into analog design, the physics laws and equations get more complicated, but they are understandable.

Understanding Basic Analog—Passive Devices Application Report

By Ron Mancini

Literature Number: SLOA027
July 1999

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Contents

List of Figures

Understanding Basic Analog – Passive Devices

By Ron Mancini

ABSTRACT

This application report describes passive devices such as resistors, capacitors, and inductors that are required to build an electronic circuit along with active devices. A well-designed circuit consists of passive devices selected to obtain specified performance.

Introduction

Passive devices are the resistors, capacitors, and inductors required to build electronic hardware. They always have a gain less than one, thus they can not oscillate or amplify a signal. A combination of passive components can multiply a signal by values less than one, they can shift the phase of a signal, they can reject a signal because it is not made up of the correct frequencies, they can control complex circuits, but they can not multiply by more than one because they lack gain.

All the glory goes to the sophisticated high gain amplifiers, but they are useless without the resistors and capacitors which control their gain. Good circuit design practice demands accurate and stable amplifiers, but active devices are by nature unstable, so they are tamed with passive components. Feedback is employed in almost all circuit designs to insure that the circuit performance is a function of the passive rather than the active components.

Passive devices are neglected in the rush to complete the design of an electronic system. Many engineers select passive devices as an afterthought; they just pick them from a list of standard components. Although this practice is adequate for some circuits, it does not suffice in the demanding world of high-frequency amplifiers, precision sample-holds, data converters, or other demanding circuits. The hardware designer must select adequate passive components to obtain specified performance in demanding applications.

The selection criteria for passive devices is as demanding as the applications for which they are used. The first selection criterion for passive components dictates that they be accurate and stable to insure proper circuit performance. After this criterion is satisfied, there are further requirements for low cost, small size, and surface-mounting, which must be met to satisfy the design specifications. Accuracy normally dictates larger size, so the accuracy requirement and the small size requirements often conflict. New surface-mount components are being introduced each day; thus, the design engineer is in a constant search to find accurate and stable passive components which meet all the criteria.

Detailed specifications including definitions of parasitic components are available from the various component manufacturers. Usually a call, letter, or email to one of these manufacturers requesting application information results in a flood of responses. The applications information should contain detail about the components, equations, dimensions, and graphs of salient parameters, photographs, tolerances, mechanical dimensions, and reliability data. If a component manufacturer cannot or will not send you this information, switch to a different manufacturer.

Resistors

There are many different resistors available for use, but only a few of them are satisfactory for accurate, stable, or high-frequency circuits. The first group of resistors includes the wirewound and composite power resistors; these resistors have too much stray inductance and capacitance to be usable at high frequencies. Because these resistors are made of wire which changes value when the temperature rises (either from self-generated heat or an external heat source), they have very poor temperature drift coefficients.

Most carbon film resistors have less stray capacitance and inductance, so they are usable at higher frequencies, but they are limited to about one percent accuracy. In addition, carbon film resistors tend to drift with temperature and vibration. Carbon composition resistors have lost their popularity to carbon film resistors because of the cost difference, but they are still used in many applications. It is reasonable to assume that a carbon composition resistor will act much like a carbon film resistor.

Metal film resistors share the stray inductance and capacitance problem with carbon films, but to a lesser extent. Metal film resistors come in smaller initial tolerances approaching 0.5%, and they are more stable under temperature and vibration extremes. Tolerances of 0.1% and lower are hard to achieve, but there are specialty houses which make precision resistors with tolerances below 0.1% on a daily basis.

Film resistors have pretty good noise performance, but some of the old carbon composition types had outstanding noise performance. When noise performance is a critical specification in a design, the resistor selection becomes very complicated. The problems associated with leaded resistors are complicated when working with surface mount resistors because of the their small size. Some very good surface-mount resistors have come on the market lately, but the surface-mount selection still leaves a lot to be desired.

Inexperienced engineers assume that a resistor is just a resistor, but it is a very complicated circuit as Figure 1 illustrates. L_L simulates the inductance of each lead. C_P is the capacitance across the resistor; thus, it appears to be in parallel with the resistor. C_P is about 0.5 pF for a 250 mΩ resistor.

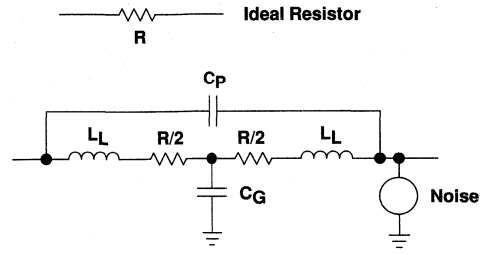


Figure 1. Resistor Equivalent Circuit

C_G is a capacitance formed by the resistor body and the ground plane, and it, like the rest of these stray effects, is a distributed effect. It can be modeled as a capacitor connected to ground from the center of the resistor because its value is small. Depending on the physical size of the resistor, C_P ranges from 0.01 pF on up to 0.5 pF. The stray effects are reduced as the size of the resistor is reduced. Surface-mount resistors have the best high frequency performance primarily because of their small size. The equation for a resistor when it is used in a circuit is given in equation 1, where V is the voltage across the resistor, and I is the current flowing through the resistor.

$$R = \frac{V}{I} \quad (1)$$

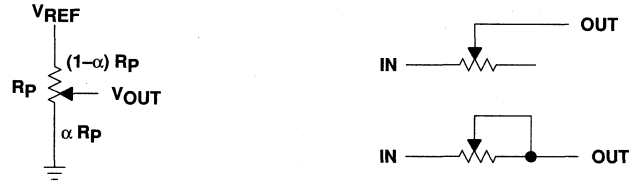
Variable Resistors or Potentiometers

Potentiometers (often called pots) are used to adjust the voltage or current at some point in a circuit. When tolerances stack up or when the specifications for a component can not be predicted accurately, pots are used to adjust out the tolerances. This adjustment enables the designer to obtain the correct circuit parameter regardless of tolerances. The overuse of potentiometers is often a sign of poor design because there are sophisticated methods for compensating for drift and tolerances. Some equipment such as projection displays use many adjustments to correct for mechanical deficiencies in the display system and these adjustments can not be designed out.

Pots have all the problems associated with fixed resistors, and they exacerbate some of them while introducing new ones. Pots are notorious for drifting under temperature, vibration, or other forms of stress. The connection from the resistive element to the lead is critical in fixed resistor design, and resistor manufacturers have become so good at making the connection that it is not considered a problem. The wiper on a pot must slide across the resistive element; thus, a good firm connection is impossible leading to a relatively high resistance connection. The best pots use films for the resistor elements, thus the wiper slides across a film where it is easier to make a low resistance connection. Beware, there is a maximum current allowed through the wiper, and either the circuit design or an external fixed resistor must be used to limit the wiper current to a safe value.

Systems that use large numbers of pots are converting to digital to analog (DAC) converters. DACs come eight and twelve to a package, and their cost is becoming equivalent to that of a pot. The adjustments are made through the keyboard or through a production test fixture. Smart systems self calibrate on start-up thus eliminating the need for pots.

Pots are used in two major applications: as voltage dividers for setting a reference voltage and as variable resistors, and both of these applications are shown in Figure 2. The voltage divider application uses the pot to set a reference voltage. The circuit shown in Figure 2 is a popular voltage divider application, and when the load resistance is much greater than the pot resistance, equation 3 represents the transfer function.



Used to Set a Reference Voltage **Used as a Variable Resistor**

Figure 2. Potentiomenter Applications

$$R_P = \alpha R_P + (1 - \alpha)R_P = R_P \tag{2}$$

The pot is divided into two parts α and $(1-\alpha)$.

$$V_{OUT} = V_{REF} \frac{\alpha R_P}{(1 - \alpha)R_P + \alpha R_P} = \alpha V_{REF} \text{ for } R_L \gg R_P \tag{3}$$

This is a very popular application for pots, and the reference input voltage must be very stable because the circuit is controlled by the reference. The reference voltage source should by well decoupled with a good grade capacitor to localize noise and keep it from spreading to other circuits.

Variable resistor applications can be very subtle, but the first thing to remember is that the pot has a limited current carrying capability. Do not connect the variable resistor configuration between the power supply and ground even if it connects through a semiconductor junction. When the variable resistor configuration is connected across a power supply or battery (even through a semiconductor junction), a series resistor must be inserted in the circuit to limit the current flow to a safe value.

Capacitors

The capacitor impedance is a function of frequency; at low frequencies the capacitor blocks signals, and at high frequencies the capacitor passes signals. Depending on the circuit connection, the capacitor can pass the signal to the next stage, or it can shunt it to ground. The impedance of a capacitor varies with frequency as shown in equation 4.

$$X_C = \frac{1}{2\pi fC} \tag{4}$$

All capacitors have a self–resonant frequency where the parasitic lead and dielectric inductance resonates with the capacitor in a series resonant circuit. Essentially, the capacitor impedance decreases until it reaches self-resonance where it is minimum impedance. The capacitor goes to lunch at frequencies higher than self resonance because the parasitic inductance causes it to becomes inductive, increasing the impendance; hence, capacitors are not dependable near their self-resonant frequency.

Aluminum electrolytic capacitors have a very low self–resonant frequency, so they are not effective in high frequency applications above a few hundred kHz. Tantalum capacitors have a mid range self-resonant frequency, thus they can be used up to several MHz. Beyond several MHz, ceramic and mica capacitors are the best choice because they have self-resonant frequencies ranging into the hundreds of MHz. Beware; there are a lot of inexpensive ceramic capacitors on the market with poor high-frequency performance.

Very low frequency and timing applications require another set of stable capacitors. The dielectric of these types of capacitor are made from paper, polypropylene, polystyrene, and polyester. These capacitors have low leakage current, low dielectric absorption, and they come in large values.

Referring to Figure 3, L models the lead and internal inductance of the capacitor. Except for dielectric materials such as ceramic and mica, the internal inductance is dominant at high frequencies. In high frequency capacitors the lead inductance can be approximated as 1/12 nh per foot. The combination of internal and lead inductance causes the capacitor to become self-resonant, and at frequencies above resonance the capacitor will appear to be an inductor. High-frequency applications demand capacitors with high self-resonant frequencies and short leads which is why surface-mount capacitors are used so often in high frequency circuit design.

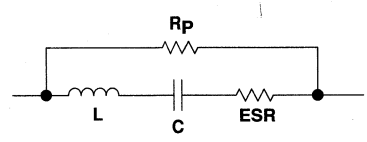


Figure 3. Capacitor Equivalent Circuit

The actual value of the capacitor is C. Equivalent series resistance (ESR) is the effective resistance of the capacitor at the operating frequency. It is an important parameter when high currents are involved. Power supply filter design requires low ESR capacitors because voltage is dropped across the ESR, and the current flowing through the capacitor causes power dissipation resulting in self heating. ESR is not an important parameter in the design of high frequency or signal processing circuits, thus ESR is only specified for aluminum electrolytic and tantalum capacitors.

The parallel resistance of a capacitor is modeled by R_P. This resistance is a function of the operating voltage and capacitor temperature; hence, it drifts quite a bit. Electrolytic capacitors exhibit the lowest parallel resistance, and aluminum electrolytic capacitors are often modeled with a parallel current source in place of R_P. Other types of capacitors have a relatively high R_P ranging in the hundreds of megohms.

Inductors

The primary use for inductors is filtering. There are two very different types of filter inductors: the high current inductor wound around a large core is used in power supply filters, and low current air core inductors are used in signal filters. The impedance of an inductor varies with frequency as shown in equation 5.

$$X_L = 2\pi fL \tag{5}$$

High current inductors require cores to keep the losses within acceptable limits and to achieve high performance. The cores are big and heavy, so they are a large contributor to cost, weight, and size. Switching power supplies require extensive inductors or transformers to control the switching noise and filter the output voltage waveform.

Low current inductors are used for filters in signal processing circuits. Capacitors, used in circuits which simulate inductors, replace inductors where possible because they are less expensive and readily available, but there are a few applications that inductors excel in. An inductive/capacitive filter has sharper slopes than a resistive/capacitive filter, thus it is a more effective filter in some applications. In general, inductors are rarely seen outside power circuits.

The inductor model, see Figure 4, is rather simple consisting of the inductor, L, the series resistance, R_S, and the parallel capacitance, C_P. The series resistor lowers the Q, or quality factor of the inductor. Inductors are wound with wire whose size determines the series resistance. The wire size also determines the weight and number of turns that can be wound on a core, so series resistance versus inductance is always a compromise that the manufacturer must make. The parallel capacitance degrades the inductor performance at high frequencies because it turns the inductor into a parallel resonant circuit. The range of C_P values is very large because of the many sizes and shapes of inductors.

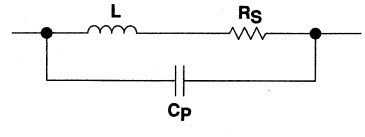


Figure 4. Inductor Equivalent Circuit

Signal or Rectifier Diodes

Diodes must be biased to be used, and often the circuit using the diode provides the bias. Forward biased diodes have the most positive voltage applied to their anode, while reversed biased diodes have the most positive voltage applied to their cathode. Forward biased diodes pass current (current is defined as the movement of positive charges) in the forward direction which is the direction of the arrow, and reverse biased diodes block current flow. Forward biased diodes exhibit a low resistance, and reverse biased diodes exhibit a high resistance.

It takes a small voltage to forward bias the diode, but as the current flow increases, its voltage drop quickly rises to approximately 0.6 volts for a silicon diode and 0.2 volts for a germanium diode. The voltage drop is a function of the bias current, but these approximations suffice for the majority of applications. Equation 6 is not an equation that you will use very much, but it describes the I/V relationship in a diode. Note that the I/V relationship is exponential.

$$I_F = I_{SAT} e^{\frac{qV_F}{KT}} \quad (6)$$

When the diode is forward biased, the voltage drop, V_F, is shown as a battery (see Figure 5).The diode resistance, r_e, is also a function of the forward current, and it is approximated by the equation $r_e = 26/I$, where I is in milliamps. This approximation of r_e holds over a wide current range. When the diode is reverse biased the forward current is zero, and the equation says that r_e equals infinity. This is not exactly true, but the relationship is too complicated for this discussion. A simple way out of the trap is to include the current source, I_L, which models a reverse biased leakage current. The leakage current is voltage and temperature sensitive, so it is best to use diodes which have very low leakage currents.

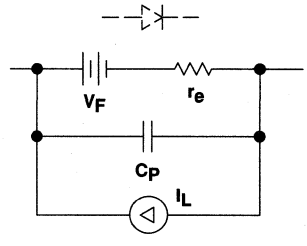


Figure 5. Diode Equivalent Circuit

A diode is used to make a positive peak detector by letting the signal forward bias the diode and storing the resultant voltage on a capacitor. Lesser voltages do not forward bias the diode, so they are ignored. When a diode is forward biased it is low resistance so it can pass a signal, and when it is reverse biased, the diode is high resistance thus it blocks the signal. The forward biased current is limited by connecting a resistor in series with the diode.

Diodes take a finite amount of time to turn on and turn off. Some of this time results from the carrier physics internal to the diode, and some of this time results from the parallel capacitance, C_P. Depending on the diode and the bias conditions, C_P ranges from a fraction of a pF for small switching diodes to a few hundred pF for power diodes. Remember, diodes have switching times that may have to be accounted for.

Component Tolerances

All passive components have initial tolerances, and no prudent engineer would design a circuit without considering tolerances induced by the circuit. The list of tolerances includes initial tolerance, temperature drift, aging, vibration, stress, and several others which are beyond the scope of this application note. The tolerance discussion is simplified by experience which yields rule of thumb tolerances which can be added to the initial tolerances.

Double the initial tolerance for resistors to allow a safety margin. Use 1% initial tolerance resistors as 2%, 2% initial tolerance resistors as 4%, and 5% initial tolerance resistors as 10%. There really is not much reason to use resistors with larger initial tolerances than 5%.

Capacitors, except for electrolytic and tantalum, follow the same rule as resistors. Both electrolytic and tantalum capacitors are polarity sensitive, so they must not be reverse biased even for short periods. Electrolytic capacitors have tolerances in the 20%, –80% percent range. Doubling these large tolerances is prohibitive, thus the application of the electrolytic capacitor determines its tolerance. Tantalum capacitors also need special care, and the application determines their tolerance, but doubling the initial tolerance works in most applications.

Miniature inductors used in high frequency work should have their initial tolerances tripled. Core inductors are extremely application sensitive, so no general rule can be given for their tolerances.

Summary

There are many different components which are not discussed. The components not covered include several types of diodes such as Schottky diodes, Zener diodes, tunnel diodes, selenium diodes, and others. The discussion does not lose much because of the components not covered, rather it enables us to focus on the components used in 99% of the applications.

Resistors control current flow by resisting it. A capacitor's impedance is a function of frequency; it blocks dc and passes ac signals. Inductors are seldom used. Diodes block reverse current and pass forward current. When diodes are forward biased their resistance is low, and when they are reverse biased their resistance is high.

All components have initial and application tolerances which must be accounted for.

Voltage Feedback Vs Current Feedback Op Amps Application Report

James Karki

Literature Number: SLVA051
November 1998

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Contents

List of Figures

Voltage Feedback Vs Current Feedback Op Amps

ABSTRACT

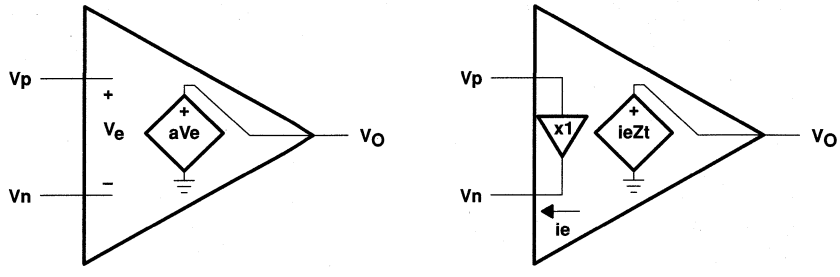
This application report contrasts and compares the characteristics and capabilities of voltage and current feedback operational amplifiers. The report also points out the many similarities between the two versions.

1 Introduction

The voltage feedback (VF) operational amplifier (op amp) is the most common type of op amp. The less well known current feedback (CF) op amp has been commercially available for about 20 years, but many designers are still uncertain about how to use them. Terminology is a confusing factor for many people. The CF op amp is a transimpedance op amp and so has a different vocabulary associated with it. This report attempts to show that there are more similarities than differences between CF and VF op amps when considering basic circuit operation.

2 Ideal Models

The ideal VF op amp model is a powerful tool that aids in understanding basic VF op amp operation. There is also an ideal model for the CF op amp. Figure 1 (a) shows the VF ideal model and Figure 1 (b) shows the CF ideal model.



(a) VF Ideal Op Amp Model (b) CF Ideal Op Amp Model

Figure 1. Ideal Op Amp Model

In a VF op amp,

$$Vo = a \times Ve \tag{1}$$

where $Ve = Vp - Vn$ is called the error voltage and a is the open loop voltage gain of the amplifier.

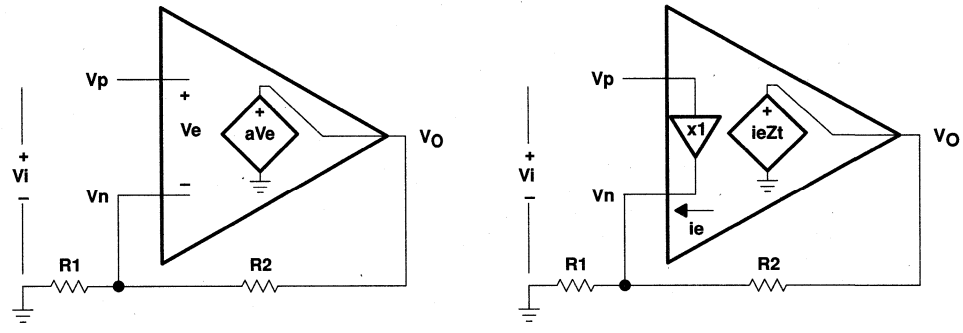
In a CF op amp,

$$Vo = ie \times Zt \tag{2}$$

where *ie* is called the error current and *Zt* is the open loop transimpedance gain of the amplifier. An amplifier where the output is a voltage that depends on the input current is called a transimpedance amplifier because the *trans*fer function equates to an *impedance* i.e., $\frac{Vo}{ie} = Zt$.

3 Ideal Models with Feedback

Applying negative feedback around the ideal models, as shown in Figure 2 (a) and Figure 2 (b), results in noninverting amplifiers. In a VF op amp, when negative feedback is applied, the action of the op amp is to drive the error voltage to zero; thus the name voltage feedback. In a CF op amp, when negative feedback is applied, the action of the op amp is to drive the error current to zero; thus the name current feedback.



(a) VF Ideal Noninverting Amp

(b) CF Ideal Noninverting Amp

Figure 2. Noninverting Amplifier

For each circuit, solving for *Vo* in relation to *Vi* gives the transfer function of the circuit. In the VF circuit, Equation 1 still holds true so that, $Vo = a \times Ve$ where $Ve = Vp - Vn$. Now $Vp = Vi$ and $Vn = Vo\frac{R1}{R1 + R2}$. Substituting and solving for $\frac{Vo}{Vi}$,

$$\frac{Vo}{Vi} = \left[\frac{a}{1 + a\left(\frac{R1}{R1+R2}\right)}\right] = \left(\frac{R1 + R2}{R1}\right)\left[\frac{1}{1 + \left(\frac{1}{a}\right)\left(\frac{R1+R2}{R1}\right)}\right] = \left(\frac{1}{b}\right)\left[\frac{1}{1 + \left(\frac{1}{ab}\right)}\right] \quad (3)$$

$$\text{where } b = \left(\frac{R1}{R1 + R2}\right)$$

In the CF circuit, Equation 2 still holds true so that, $Vo = ie \times Zt \Rightarrow ie = \frac{Vo}{Zt}$. Also, $Vn = Vp = Vi$. Summing currents at node *Vn*, $(-ie) + \left(\frac{Vn}{R1}\right) + \left(\frac{Vn-Vo}{R2}\right) = 0$. Substituting and solving for $\frac{Vo}{Vi}$;

$$\frac{Vo}{Vi} = \left(\frac{R1 + R2}{R1}\right)\left[\frac{1}{1 + \left(\frac{R2}{Zt}\right)}\right] = \left(\frac{1}{b}\right)\left[\frac{1}{1 + \left(\frac{R2}{Zt}\right)}\right] \text{where } b = \left(\frac{R1}{R1 + R2}\right) \quad (4)$$

In either circuit (VF or CF noninverting amplifier), it is desired to set the gain by the ratio of R1 to R2. The second term on the right hand side of Equations 3 and 4 is seen as an error term. In the VF case, if *ab* is large (ideally equal to infinity), then the error is negligible. In the CF case, if *Zt* is large (ideally equal to infinity) in comparison to *R2,* then the error is negligible.

Comparing the ideal behavior of VF and CF amplifiers shows very little difference.

4 Frequency Dependant Gain Model

The open loop gain, *a* for VF or *Zt* for CF, is frequency dependant in real op amps. In Figure 3, components are added to the ideal models (of Figure 1), which model the dominant bandwidth limitations. See Appendix A for the derivation of these models.

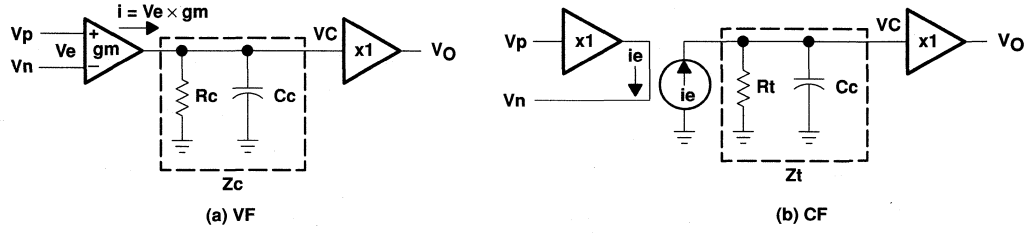


Figure 3. Frequency Model

To solve the input to output transfer function is the same as above.

For the VF op amp:

$$Vo = Vc = i \times Zc = Ve \times gm \times (Rc \parallel Cc) \ . \tag{5}$$

Rearranging and substituting $Rc \parallel Cc = \dfrac{Rc}{1 + j2\pi fRcCc}$

$$\frac{Vo}{Ve} = gm\left(\frac{Rc}{1 + j2\pi fRcCc}\right). \tag{6}$$

This is the same as Equation 1 with $a = gm\left(\dfrac{Rc}{1 + j2\pi fRcCc}\right)$.

The term $gm\left(\dfrac{Rc}{1 + j2\pi fRcCc}\right)$ is the open loop gain of the op amp, usually denoted as *a(f)* in the literature. The VF op amp's open loop gain has a dc response, a break frequency, and a –20dB/dec roll-off. At low frequencies, $2\pi fRcCc \ll 1$, and $\left|\dfrac{Vo}{Ve}\right| \cong gm \times Rc$, which is extremely high at dc. As frequency increases, eventually $2\pi fRcCc = 1$, and $\left|\dfrac{Vo}{Ve}\right| = (gm \times Rc)\left(\dfrac{1}{\sqrt{2}}\right)$. This is the dominant pole frequency, f_D. At frequencies above f_D, *Cc* begins to dominate the response so that $\left|\dfrac{Vo}{Ve}\right| \cong \dfrac{gm}{2\pi fCc}$, and the gain rolls off at –20dB/dec. *Cc* is usually chosen so that the amplification falls to unity [noted as Fu in Figure 5(a)] before upper frequency poles cause excessive phase shift.

For the CF op amp:

$$Vo = Vc = ie \times Zt = ie \times (Rc \parallel Cc) \ . \tag{7}$$

Rearranging and substituting $Rc \parallel Cc = \dfrac{Rc}{1 + j2\pi fRtCc}$

$$\frac{Vo}{ie} = \left(\frac{Rt}{1 + j2\pi fRtCc}\right).$$

This is the same as Equation 2 with $Zt = \left(\dfrac{Rt}{1 + j2\pi fRtCc}\right)$

The term $Zt = \dfrac{Rt}{1 + j2\pi fRtCc}$ is the open loop gain of the op amp, which is frequency dependent, and is more properly denoted *Zt(f)*. The CF op amp's open loop gain has a dc response, a break frequency, and a –20dB/dec roll off. At low frequencies, $2\pi fRtCc \ll 1$, and $\left|\dfrac{Vo}{ie}\right| \cong Rt$, which is extremely high at dc. As frequency increases, eventually $2\pi fRtCc = 1$, and $\left|\dfrac{Vo}{ie}\right| = \dfrac{Rt}{\sqrt{2}}$. This is the dominant pole frequency, f_D. At frequencies above f_D, *Cc* begins to dominate the response so that $\left|\dfrac{Vo}{ie}\right| \cong \dfrac{1}{2\pi fCc}$, and the gain rolls off at –20dB/dec. *Cc* is usually chosen so that *Zt* will roll off to the desired feedback resistor value before upper frequency poles cause excessive phase shift.

5 Feedback with Frequency Dependant Models

Applying a negative feedback network (as in Figure 2) to the op amp frequency models as shown in Figure 4 results in noninverting amplifiers.

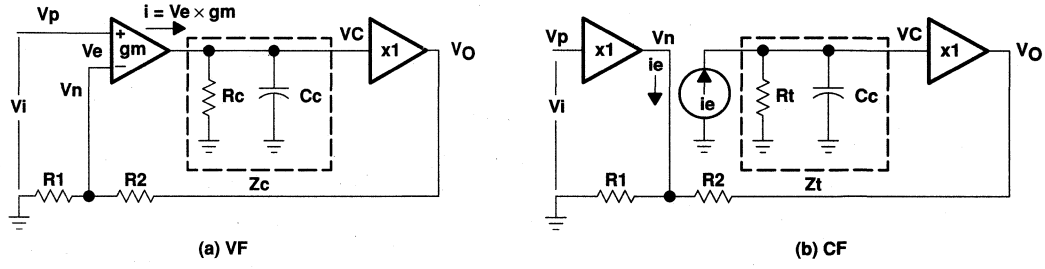


Figure 4. Feedback with Frequency Dependant Models

Solve the transfer function for the VF noninverting amplifier by substituting

$$a = gm\left(\frac{Rc}{1 + j2\pi fRcCc}\right) \text{ in Equation 3. Therefore:} \tag{8}$$

$$\frac{Vo}{Vi} = \left(\frac{R1 + R2}{R1}\right)\left[\frac{1}{1 + \dfrac{1}{gm\left(\dfrac{Rc}{1+j2\pi fRcCc}\right)\left(\dfrac{R1}{R1+R2}\right)}}\right]$$

The gain-bandwidth relationship of the VF noninverting amplifier can be seen clearly by expanding and collecting terms in the second term on the right hand side of Equation 8.

$$\left[\frac{1}{1 + \dfrac{1}{gm\left(\dfrac{Rc}{1+j2\pi fRcCc}\right)\left(\dfrac{R1}{R1+R2}\right)}}\right] = \left[\frac{1}{1 + \dfrac{(R1+R2)(1+j2\pi fRcCc)}{gm \times Rc \times R1}}\right] \tag{9}$$

$$= \left[\frac{1}{1 + \left(\dfrac{1}{gm \times Rc}\right)\left(\dfrac{R1+R2}{R1}\right) + \left(\dfrac{R1+R2}{R1}\right)\left(\dfrac{j2\pi fCc}{gm}\right)}\right]$$

Usually $gm \times Rc$ is very large so that $\left(\dfrac{1}{gm \times Rc}\right)\left(\dfrac{R1 + R2}{R1}\right) \ll 1$. Disregarding this term and substituting Equation 9 into Equation 8 results in

$$\frac{Vo}{Vi} \cong \left(\frac{R1 + R2}{R1}\right)\left[\frac{1}{1 + \left(\frac{R1}{R1 + R2}\right)\left(\frac{j2\pi fCc}{gm}\right)}\right] \tag{10}$$

The term $\left(\frac{R1 + R2}{R1}\right)$ is the desired closed loop gain of the amplifier. (11)

At low frequency where $\left(\frac{R1 + R2}{R1}\right)\left(\frac{j2\pi fCc}{gm}\right) \ll 1j$, $\left|\frac{Vo}{Vi}\right| \cong \left(\frac{R1 + R2}{R1}\right)$.

As frequency increases, eventually $\left(\frac{R1}{R1 + R2}\right)\left(\frac{j2\pi f_c Cc}{gm}\right) = 1j$

and the gain of the circuit is reduced by 3 dB: $\left|\frac{Vo}{Vi}\right| \cong \left(\frac{R1 + R2}{R1}\right)\left(\frac{1}{\sqrt{2}}\right)$. The frequency $f_c = \left(\frac{gm}{2\pi Cc}\right)\left(\frac{R1}{R1 + R2}\right)$ is the –3 dB bandwidth, or cutoff frequency of the circuit. Rearranging, $(f_c)\left(\frac{R1 + R2}{R1}\right) = \left(\frac{gm}{2\pi Cc}\right) = constant$. Therefore, in a voltage feedback op amp, the product of the closed loop gain and the closed loop bandwidth is constant over most of the frequencies of operation. This is the gain bandwidth product, (GBP). The result is that if gain is multiplied by 10, bandwidth is divided by 10.

Solve the transfer function for the CF noninverting amplifier by substituting $Zt = \frac{Rt}{1 + j2\pi fRtCc}$ in Equation 4. Therefore:

$$\frac{Vo}{Vi} = \left(\frac{R1 + R2}{R1}\right)\left[\frac{1}{1 + (R2)\left(\frac{1 + j2\pi fRtCc}{Rt}\right)}\right] \tag{12}$$

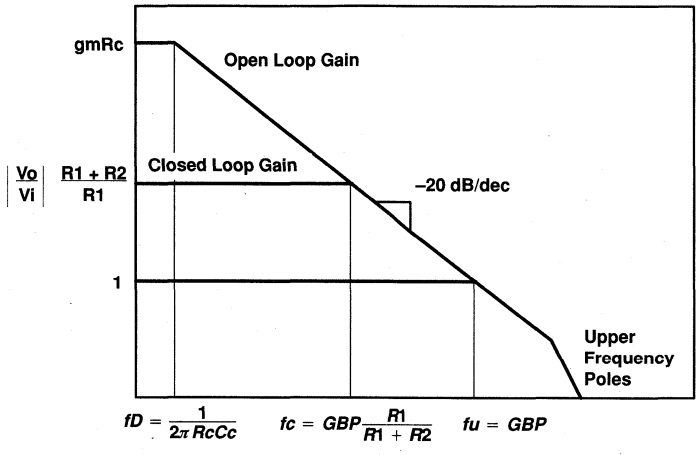
$$= \left(\frac{R1 + R2}{R1}\right)\left[\frac{1}{1 + \left(\frac{R2}{Rt}\right) + (j2\pi fR2Cc)}\right]$$

Normally $\frac{R2}{Rt} \ll 1$ and is disregarded resulting in:

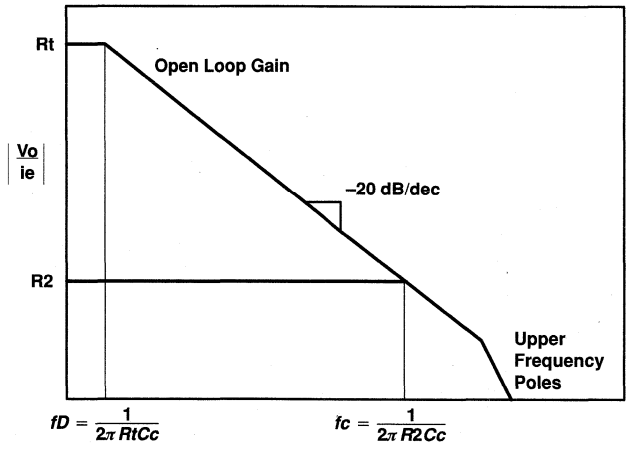
$$\frac{Vo}{Vi} \cong \left(\frac{R1 + R2}{R1}\right)\left[\frac{1}{1 + (j2\pi fR2Cc)}\right] \tag{13}$$

Equation 13 shows that the –3dB bandwidth or cutoff frequency, f_c, can be set by selection of $R2$ so that $f_c = \frac{1}{2\pi R2Cc}$, and gain can be set by selection of $R1$. Thus in a CF op amp gain and bandwidth are independent of each other.

Figure 5 shows Bode plots of the gain vs. frequency characteristics of the VF and CF op amp models.



(a) VF Bode Plot



(b) CF Bode Plot

Figure 5. Bode Plot

6 Summary

A VF op amp is a voltage amplifier $\frac{Vo}{Ve} = a(f)$ and a CF op amp is a transimpedance amplifier $\frac{Vo}{ie} = Zt(f)$. In each the effect of negative feedback is to drive the input to zero: $Ve \rightarrow 0$ and $ie \rightarrow 0$; thus the names VF and CF. When configured as noninverting amplifiers with negative feedback, both op amps provide a voltage gain that is determined by the feedback network. In each the open loop gains, $a(f)$ and $Zt(f)$, are frequency-dependent and limit the bandwidth of operation. In VF op amp circuits the gain bandwidth product is constant over the normal frequencies of operation. In CF op amp circuits the gain and bandwidth can be set independently of one another.

The majority of VF op amps are unity-gain stable, so the designer is relieved of the burden of compensating circuits for stable operation. This also limits bandwidth to the minimum capability of the op amp design.

The impedance of the negative feedback component determines stability in a CF op amp circuit. There is a minimum value of R2 to maintain stability (conversely there is a maximum bandwidth for a given phase margin). For this reason, if a buffer amplifier is configured by shorting the output to the negative input, the circuit will oscillate. Also, care must be taken when using capacitance in the feedback loop as in the case of an integrator or low pass filter.

Table 1. VF vs CF: Comparison of Major Parameters

PARAMETER	VF	CF
Open loop gain	Voltage $\frac{Vo}{Ve} = a(f)$. Frequency dependant, limits bandwidth.	Transimpedance $\frac{Vo}{ie} = Zt(f)$. Frequency dependant, limits bandwidth.
Closed loop gain	$\frac{Vo}{Vi} = \left(\frac{1}{b}\right)\left[\frac{1}{1+\left(\frac{1}{ab}\right)}\right]$	$\frac{Vo}{Vi} = \left(\frac{1}{b}\right)\left[\frac{1}{1+\left(\frac{R2}{Zt}\right)}\right]$
Ideal closed loop gain	Set by feedback factor $\left(\frac{1}{b}\right)$	Set by feedback factor $\left(\frac{1}{b}\right)$
Gain bandwidth product	Gain and bandwidth interdependent. Constant over most frequencies of operation.	Gain and bandwidth independent of each other.
Stability	Normally unity gain stable.	Minimum impedance in feedback component required for stability
Bandwidth	Set by closed loop gain	Set by impedance of feedback component

Appendix A Derivation of Models

Figure A1 and Figure A2 show simplified schematic diagrams of the THS4001 and THS3001, and their models. The following discussion provides an overview of how the frequency dependent models are derived.

A.1 THS4001 – VF Frequency Dependent Model (see Figure A–1)

A.1.1 Differential Pair

Q1 and Q2 comprise the input differential pair. Three current sources, *i*, are used to bias the circuit for normal operation; *i=i1+i2.*

- When *Vp=Vn, i1=i2*, and the collector currents of Q1, Q2, Q3, and Q4 are equal.
- When *VP>Vn*, Q2 turns on harder and *i2* increases. The bottom current source insures that i=i1+i2. Therefore i1 decreases..
- When *Vp<Vn*, Q1 turns on harder and *i1* increases. The bottom current source insures that *i=i1+i2.* Therefore *i2* decreases.

Thus the differential voltage at the input Vn and Vp causes differential currents to be generated in Q3 and Q4. The differential input stage is modeled by the transconductance amplifier, *gm.*

A.1.2 High Impedance

The current, *i2,* develops voltage, *Vc,* at the high impedance node formed by the current mirror structure, D5–Q5 and D6–Q6, and capacitor *Cc.* The high impedance stage is modeled by the parallel impedance, $Zc = Rc \parallel Cc$. *Rc* models the equivalent dc resistance to ground. *Cc* is actually two capacitors; one to the positive supply and one to the negative supply. *Cc* is the parallel combination and the supply pins are assumed to be ac grounds.

A.1.3 Double Output Buffer

Q7 through Q10 form a double buffer that is a class AB amplifier. The voltage *Vc* is buffered to the output so that *Vo=Vc.* The double output buffer is modeled by the X1 buffer amplifier.

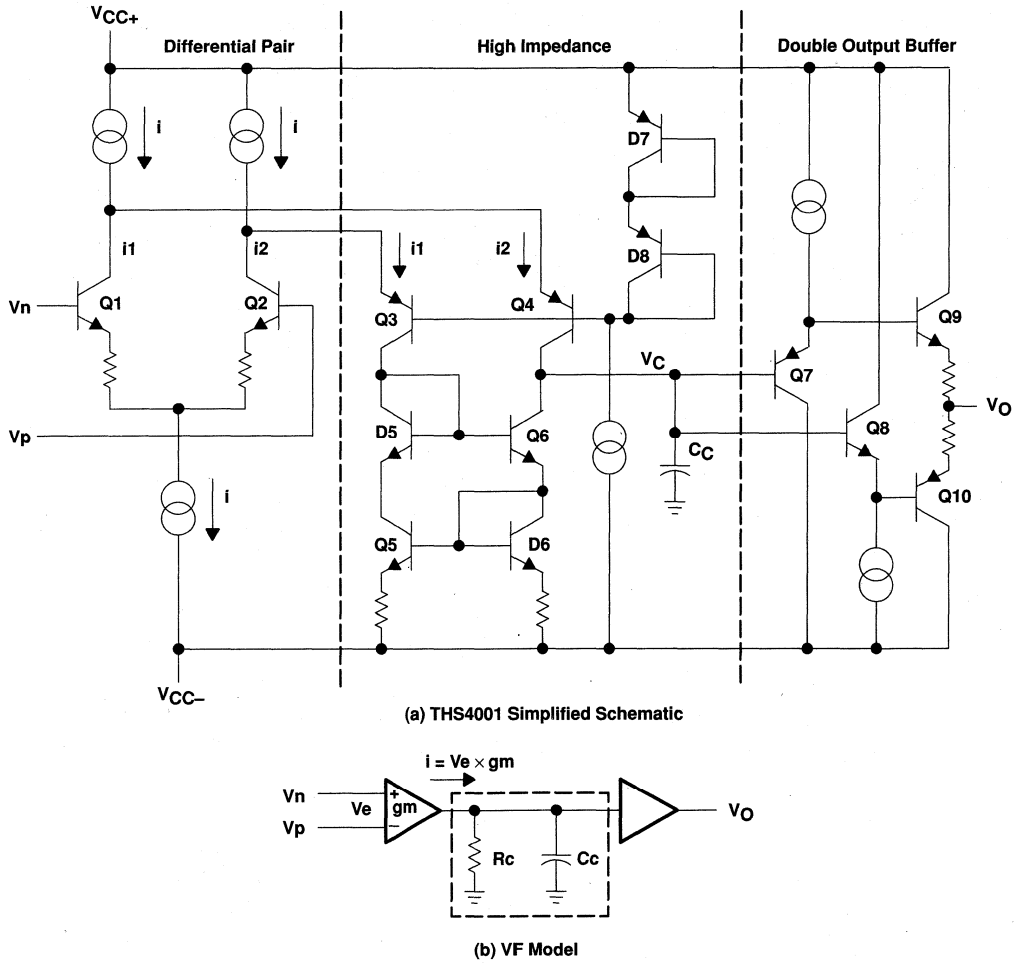


Figure A–1. VF Model Derivation

A.2 THS3001 – CF Frequency Dependent Model (see Figure A–2)

A.2.1 Class AB Amplifier

D1–Q1 and D2–Q2 comprise a class AB amplifier where the signal at *Vp* is buffered with a gain of 1 to *Vn*. The input stage is modeled by the X1 buffer amplifier between *Vp* and *Vn*.

A.2.2 Current Mirror

The collector current of Q1 is drawn through D3. D3–Q3 form a current mirror so that the collector current of Q3 equals the collector current of Q1. The same is true for the bottom side so that Q2's current is mirrored by Q4. This is modeled as a current source equal to the input error current driving the high impedance.

A.2.3 High Impedance

The current, *i1* or *i2,* develops voltage, *Vc*, at the high impedance node, D5–D6, and *Cc*. The high impedance is modeled by parallel impedance, $Zt = Rt \| Cc$. *Rt* models the equivalent dc resistance to ground. *Cc* is actually two capacitors; one to the positive supply and one to the negative supply. *Cc* is the parallel combination and the supply pins are assumed to be ac grounds.

A.2.4 Triple Output Buffer

Q5 through Q10 form a triple buffer that is a class AB amplifier. The voltage *Vc* is buffered to the output so that *Vo=Vc*. The triple output buffer is modeled by the X1 buffer amplifier.

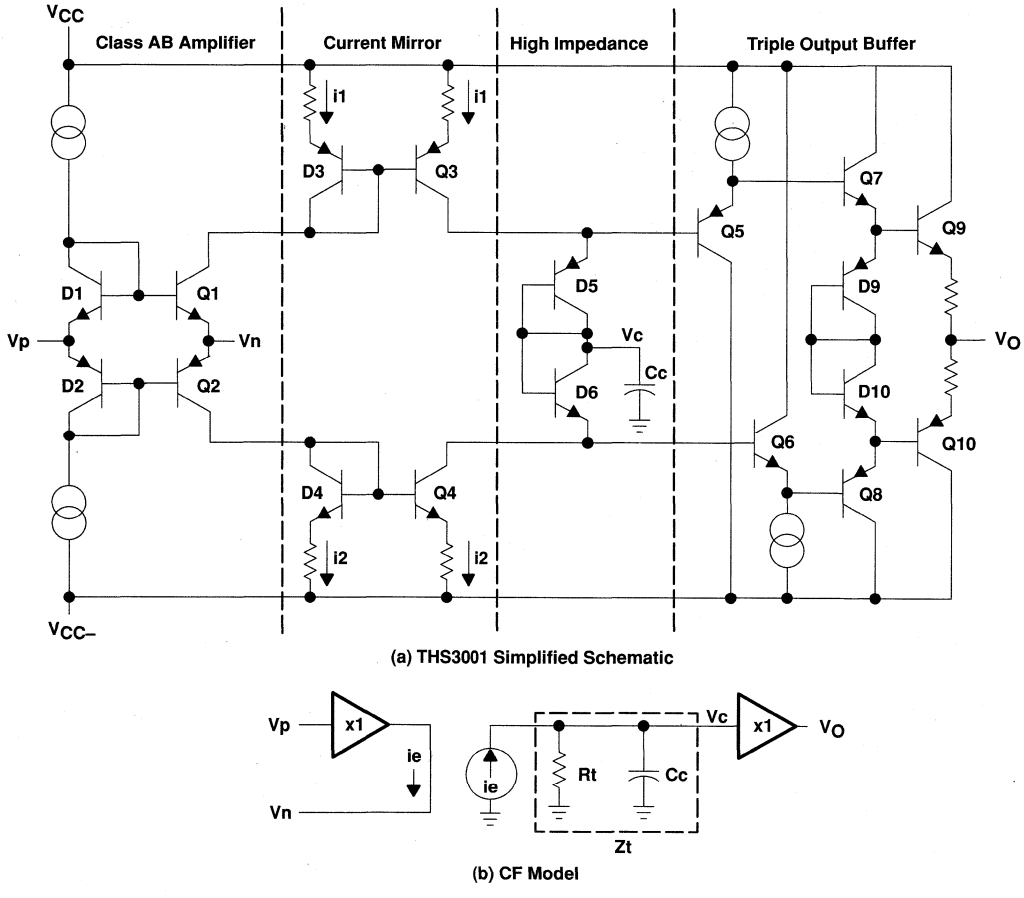


Figure A–2. CF Model Derivation

TEXAS INSTRUMENTS

Application Report
SLOA032 - October 1999

10 MHz Butterworth Filter Using the Operational Amplifier THS4001

Dirk Gehrke and Andreas Hahn

MSLP/AAP

ABSTRACT

This application report describes the design of an active 10MHz second-order Butterworth low-pass filter useful for band-limiting applications. As an active component, TI's operational amplifier type THS4001, which has a bandwidth of 300 MHz, was used.

The design of the filter described in this report is typical of practical applications, and the steps involved in calculating component values can be completed easily. This filter has the following features:

- The component values are easily calculated.
- It is a second-order filter.
- It has an attenuation of 40 dB/decade (12 dB/octave).
- The amplitude frequency response is linear up to the cutoff frequency.

Contents

List of Figures

List of Tables

1 Introduction

Texas Instruments produces a variety of operational amplifier products for high-frequency applications. The operational amplifiers that are now available attain much greater bandwidths than previous models and allow the design of circuits that take full account of more demanding requirements. SMD components and smaller semiconductor packages make it easier to meet requirements for more compact applications with improved performance.

Although digital circuits play a dominant role, analog components remain important in a variety of systems because they are essential for signal conditioning and processing in many circuits. Special low-pass filters are commonly needed in such cases. Analog filter circuits are usually designed with passive components (R,L,C), or they are constructed in combination with active components, such as operational amplifiers and transistors.

2 The Basic Theory of Low-Pass Filters

An electronic filter can be considered as a network. This network changes the signal amplitude and phase as a function of the frequency, and no new frequency components are added to the signal. An ideal low-pass filter must attenuate all signals 100% which are higher than the cutoff frequency (f_g), and the signal response must be linear up to the cutoff frequency. From the stop frequency (f_s), a specified attenuation must not be exceeded. In practice, however, the ideal cannot be attained; compromises must always be reached.

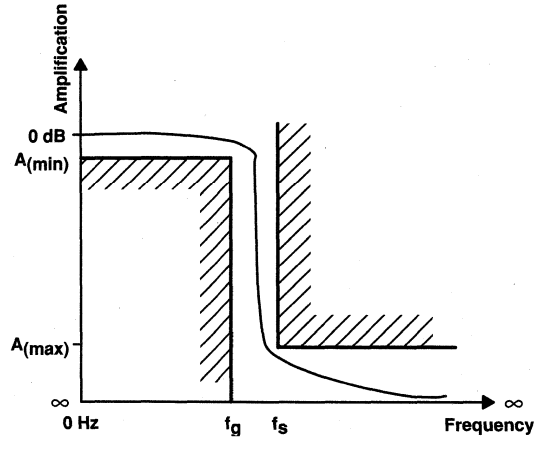


Figure 3. The Amplitude Response With Frequency and Limits of a Low-Pass Filter

A wide variety of filter types is available, each characterized by different properties. For every application requirement, a particular type of filter fulfills the requirements specific to the application. The three most important types of filters are the Butterworth low-pass filter, the Tschebyscheff low-pass filter, and a Bessel low-pass filter.

A Butterworth low-pass filter features a horizontal amplitude frequency response that changes direction abruptly at the cutoff frequency, depending on the order number. However, the square pulse response of this filter shows a considerable overshoot when compared to the Bessel filter. This increases with increasing filter order.

With a Tschebyscheff low-pass filter, the reduction of the amplification is even more pronounced than with the Butterworth low-pass filter. The amplitude frequency response within the pass band is not monotone, but instead contains ripples of constant amplitude. The higher the permissible ripple for the filter order used, the greater is the reduction in the amplification above the cutoff frequency.

In a Bessel low-pass filter, the amplitude frequency response does not change direction as abruptly as with the Butterworth and Tschebyscheff low-pass filters. However, this filter has an optimum square-wave response.

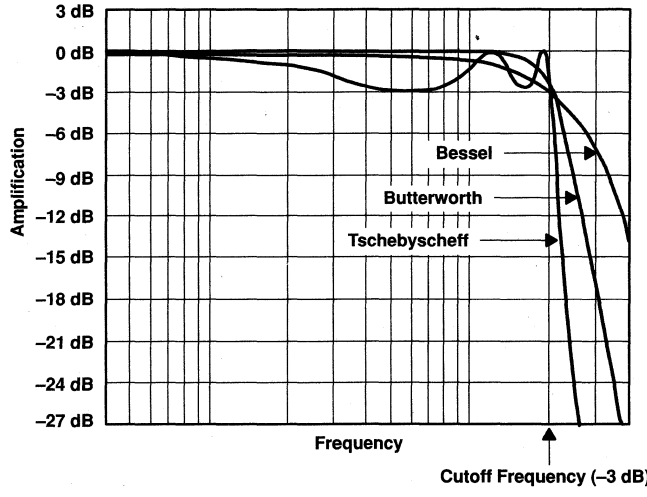


Figure 4. Amplitude Frequency Response for Fifth-Order Filters

3 The Correct Choice of a Filter Type

The most important consideration in choosing a filter type is the intended use of the filter. For example, if the requirement is to attain optimum behavior with square-wave signals, together with good frequency limiting, then the Bessel low-pass filter is the logical choice. This filter provides the least overshoot as a response to transients, when compared with Tschebyscheff or Butterworth low-pass filters. The disadvantage of this filter is the less abrupt kink in the amplitude frequency response. If, however, square-wave behavior is of less importance than the attenuation of sine-wave signals, then the decision will be in favor of Tschebyscheff or Butterworth filters.

From the cutoff frequency onward, the Tschebyscheff filter has a strongly accentuated reduction in amplification. However, the amplitude frequency response within the pass band is not monotone, but instead features ripples with constant amplitude. The higher the permitted ripple of the order in question, the greater the attenuation above the cutoff frequency. The advantage of the greater reduction in amplification must be set against the higher ripple before the cutoff frequency. In contrast, the Butterworth filter features an almost linear amplitude frequency response up to the cutoff frequency. It is used mainly when a minimum distortion of the input signal is required; only the part of the signal above the cutoff frequency will be attenuated. Figure 2 shows the principal amplitude frequency response of the three types of filters.

The design proposal discussed later is based on a second-order Butterworth low-pass filter. This design offers a linear amplitude frequency response of up to the cutoff frequency of 10 MHz.

4 Low-Pass First-Order RC Filter

A low-pass first-order filter is most simply constructed with an RC network. The resistor is in the signal path, and the capacitor is in parallel with the output.

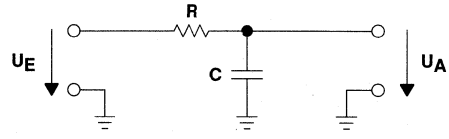


Figure 5. RC Network Used as a Low-Pass Filter

The following equation can be used to express the relationship between the output and the input voltage:

$$\underline{H}(j\omega) = \frac{\underline{U}_A}{\underline{U}_E} = \frac{1}{(1 + j\omega RC)} \tag{14}$$

By replacing $j\omega$ with s, the following transfer function results:

$$H(s) = \frac{1}{1 + sRC} \tag{15}$$

The absolute value for the amplitude response at the frequency in question can be calculated as:

$$|H(f)| = \frac{|U_A|}{|U_E|} = \frac{1}{\sqrt{1^2 + (\omega RC)^2}} \tag{16}$$

The following formula describes the phase relationship at the frequency in question:

$$\phi = -\arctan(\omega RC) \tag{17}$$

In order to derive a transfer function that is generally applicable, the frequency must be normalized. For this purpose, the cutoff frequency is usually used, but any desired frequency can be chosen. If the result is examined after normalization with the cutoff frequency, then the advantages here become clearly apparent.

After normalization ($j\omega$) with the cutoff frequency (ω_g) to $j\frac{\omega}{\omega_g} = j\Omega$ and correspondingly s to $\frac{s}{s_g} = S$, with the cutoff frequency $f_g = \frac{1}{2\pi RC}$, the transfer function (1) results in:

$$H(S) = \frac{1}{1 + S} \tag{18}$$

The formula is now universal and independent of a definite frequency. It is easier to see the behavior for different frequencies. For $\omega >> \omega_g$ the value is obtained of $H(S) = \frac{1}{S}$, the amplification is thus reduced in proportion to the frequency. This corresponds to an attenuation of 20 dB per decade of frequency.

5 Filter Orders

The order of a filter can be determined by observing the transfer function. With the power of *S*, the order of the filter can be determined at the same time. The highest power of *S* in the transfer function is a direct measure of the magnitude of the filter order. With every increase of order *n*, the attenuation at higher frequencies increases by *n* 20 dB. The order of a filter is usually the same as the number of inductors and capacitors that are found in the circuit. In this case, groups of *C* or *L*, which represent an order, are brought together as a group component. The order is then reflected in the number of components; the number of components determines the cost, as well as the size and complexity of the layout. An important advantage of a filter of higher order is the increase of attenuation of 20 dB per order.

6 Filters of Higher Order

Until this point, only passive components have been used. If an active component is employed, the expression used is of active filters. Second-order active filters can be constructed with an operational amplifier. Using the decoupling property of the operational amplifier, several filters can be connected in series. To design a filter with an order higher than two, first-order and second-order filters are connected in series to form the required order of the filter.

The general transfer function formula for low-pass filters is as follows:

$$H(S) = \frac{K}{\left(b_1 S^2 + a_1 S + 1\right)\left(b_2 S^2 + a_2 S + 1\right)\ldots\left(b_i S^2 + a_i S + 1\right)} \quad (19)$$

Taking $i = 1$ and $b = 0$ and $k = 1$ forms the transfer function (5) of a passive low-pass filter of first order having the coefficient $a_i = 1$. The behavior of this passive filter is changed when it is loaded. To prevent this from happening, a voltage follower is inserted in the circuit after the filter. From the passive filter with a coefficient of $a_i = 1$, an active filter with a coefficient of a_i , usually not equal to 1, is created.

By means of suitable coupling, a second-order low-pass filter is formed from the first-order active low-pass filter. The following transfer function is obtained:

$$H(S) = \frac{K}{\left(bS^2 + aS + 1\right)} \quad (20)$$

To obtain filters of higher order, filters of first and second order are connected in succession. The coefficients *a* and *b* determine the type of filter as a result of the transfer behavior. From filter tables (see Table 1), the coefficients can be determined for the individual types of filters: Butterworth, Tschebyscheff, or Bessel. Table 1 shows the coefficients *a* and *b* for these three types of filters.

7 Pole Quality *Q* of an Active Filter

The parameter *Q* stands for the pole quality. It indicates whether a filter has a tendency toward instability. The pole quality *Q* is defined as $Q = \frac{\sqrt{b_i}}{a_i}$. The larger the pole quality *Q*, the more abrupt will be the kink in the transfer function at the cutoff frequency. Close to the cutoff frequency (f_g), the amplification increases by a factor of *Q* when compared to the dc voltage amplification. A pole quality *Q* that is too high often gives rise to a tendency to oscillation.

Table 1. Filter Coefficients for 3 dB Cutoff Frequency

Butterworth WITH 3 dB CUTOFF FREQUENCY						
FILTER ORDER	ORDER PER FILTER	*i*	a_i	b_i	$\frac{f_{gi}}{f_g}$	Q_i
1	First	1	1.0000	0.0000	1.000	–
2	Second	1	1.4142	1.0000	1.000	0.71
3	First Second	1 2	1.0000 1.0000	0.0000 1.0000	1.000 1.272	– 1.00
4	Second Second	1 2	1.8478 0.7654	1.0000 1.0000	.719 1.390	0.54 1.31
Tschebyscheff WITH 3 dB RIPPLE						
FILTER ORDER	ORDER PER FILTER	*i*	a_i	b_i	$\frac{f_{gi}}{f_g}$	Q_i
1	First	1	1.0000	0.0000	1.000	–
2	Second	1	1.0650	1.9305	1.000	1.30
2	First Second	1 2	3.3496 0.3559	0.0000 1.1923	0.299 1.396	– 3.07
2	Second Second	1 2	2.1853 0.1964	5.5339 1.2009	0.557 1.410	1.08 5.58
Bessel WITH 3 dB CUTOFF FREQUENCY						
FILTER ORDER	ORDER PER FILTER	*i*	a_i	b_i	$\frac{f_{gi}}{f_g}$	Q_i
1	First	1	1.0000	0.0000	1.000	–
2	Second	1	1.3617	0.6180	1.000	0.58
2	First Second	1 2	0.7560 0.9996	0.0000 0.4772	1.323 1.414	– 0.69
2	Second Second	1 2	1.3397 0.7743	0.4889 0.3890	0.978 1.797	0.52 0.81

8 Filters With Simple Coupling

Designing active filters can be approached in various ways. The following example describes the layout and the calculation of the component values for an active second-order filter. The capacitor C_2 is connected in the positive feedback loop. This filter, which has simple positive feedback, is known as a Sallen-and-Key low-pass filter. Figure 4 shows the basic layout of the filter.

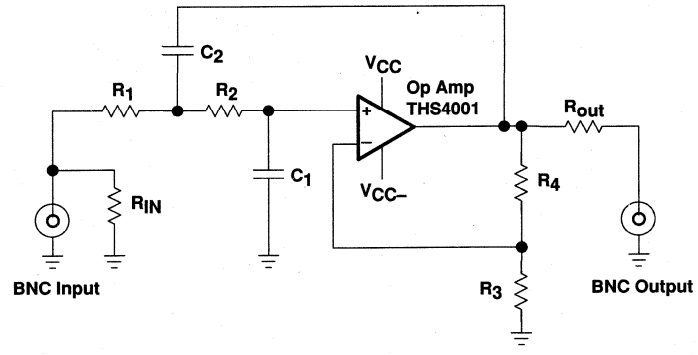


Figure 6. Active Low-Pass Filter of Second-Order With Simple Positive Feedback

The following formula gives the transfer function of an active second-order low-pass filter with simple positive feedback:

$$H(S) = \frac{K}{R_1 C_1 R_2 C_2 \omega_g^2 S^2 + [C_1(R_1 + R_2) + R_1 C_2(1-K)]\omega_g S + 1} \tag{21}$$

The desired filter type is designed by selecting the appropriate filter coefficients from Table 1. Several methods exist for finding the values for the components of the Sallen-Key filter. For two components and the factor K, a fixed value is choosen, and the other values for the missing components can be calculated.

A special case is created by choosing the same values for $R_1 = R_2 = R$ and for $C_1 = C_2 = C$. This special case results in a simplification in the choice of components and it simplifies Formula (8) as follows:

$$H(S) = \frac{K}{(RC\omega_g)^2 S^2 + RC(3-K)\omega_g S + 1} \tag{22}$$

When the Butterworth coefficients $a_1 = 1.4142$ $b_1 = 1$ from Table 1 are inserted in the normalized expression (7), the normalized form of a second order Butterworth low-pass results:

$$H(S) = \frac{K}{(1S^2 + 1.4142S + 1)} \tag{23}$$

Considering Formula (9), the calculation of the amplification factor K results in:

$$K = 3 - \frac{a_1}{\sqrt{b_i}} = 3 - \frac{1}{Q_i} = 1 + \frac{R_4}{R_3} = 1.586 \tag{24}$$

The potential divider, consisting of R_3 and R_4, results in feedback of the output signal and amplification by the circuit. For the special case using the pole quality Q, the amplification factor K for the potential divider R_3 and R_4 can be calculated. This means that the amplification depends only on the pole quality Q and not on the cutoff frequency f_g . For low frequencies the amplification results in 1.586 equal 4 dB by the special case. This amplification can be corrected with a resistor divider at the input or output.

After a comparison of the coefficients from the normalized formula (10) with the formula (9) of the special case, the following formula is obtained for the resistors:

$$R = \frac{\sqrt{b_1}}{2\pi f_g C} = \frac{1}{2\pi f_g C} \tag{25}$$

The value for the capacitors C can be freely chosen. The use of a stereo potentiometer, instead of the resistors R_1 and R_2, allows the cutoff frequency to be varied over an almost unlimited range. This is possible because the type of filter is decided exclusively by the amplification factor K, whereas C_1, C_2, R_1, and R_2 determine the cutoff frequency. A problem that arises in practice is that passive components have tolerances on their actual values. These tolerances have a considerable effect on the characteristics of the filter. In particular, filters with a high cutoff frequency exhibit RF effects that are unimportant in filters for lower frequencies. Close attention must be paid to layout when working at higher frequencies. The use of SMD components and the shortest possible signal paths are important factors in layout design. In addition, only close tolerance components should be used for the construction of filter circuits. The selection of pairs of components that determine the frequency response ensures the best possible filter characteristics. In practice, components with a maximum tolerance of 1% should be used.

9 Calculation of Filter Component Values

Because of the simplification of the formula, calculating component values for the second-order filter requires only minimal computing effort and simplifies planning and design.

A value for the capacitors $C_1 = C_2 = C$ is first determined by the user. The value must be chosen so that a positive real figure results when calculating the values for resistors. A capacitance value that is considerably higher than the input capacitance of the operational amplifier should be selected. Otherwise, the input capacitance must be taken into account. Capacitors that are available in the E6 series should be chosen. These SMD chip capacitors are available from many suppliers with 1% tolerance.

In this particular case, a capacitance of 15 pF was chosen for C_1 and C_2. If higher values are chosen for the capacitors, then the resistor values decrease. However, resistor values that are too low are also a load for the output and result in additional phase shifting. Testing showed that 15 pF is the best value for a 10 MHz cutoff frequency.

To calculate the values of the resistors R_1 and R_2, only the values for the cutoff frequency, the capacitance, and the quadratic factor b_1 are needed from Table 1.

$$R = \frac{\sqrt{b_1}}{2\pi f_g C} \tag{26}$$

$$R = \frac{\sqrt{1}}{2\pi \times 10 \times 10^6 \times 15 \times 10^{-12}}\Omega \tag{27}$$

$$R = 1061\ \Omega \tag{28}$$

Table 2. Component Values That Result for the Low-Pass Filter

COMPONENTS DESIGNATION	VALUES OF COMPONENTS	
	CALCULATED OR FIXED	USED
C_1 , C_2	15 pF	15 pF
R_1 , R_2	1061 Ω	1k Ω
R_{out} , R_{in}	50 Ω	51 Ω
R_3	1.3 Ω	1.3 kΩ
R_4	761.5 Ω	750 Ω
C_3, C_5	100 nF	100 nF
C_4, C_6	6.8 µF	6.8 µF/35 V Tantalum

The amplification factor K is calculated according to the formula $K = 1 + \frac{R_4}{R_3}$. By deriving a figure for K from Formula (11) and inserting R_3, the value for R_4 can be calculated.

The value for R_3 must be selected carefully because the –3 dB bandwidth of the THS4001 is depending on the value of the feedback resistor. Because of the stray capacitances and their influence on high-speed designs, low value resistors should be chosen to minimize the effects of stray capacitances. Measurements showed best results for values of 1300 Ω (R_3) and 750 Ω (R_4).

The component values used for the test circuit are shown in Table 2.

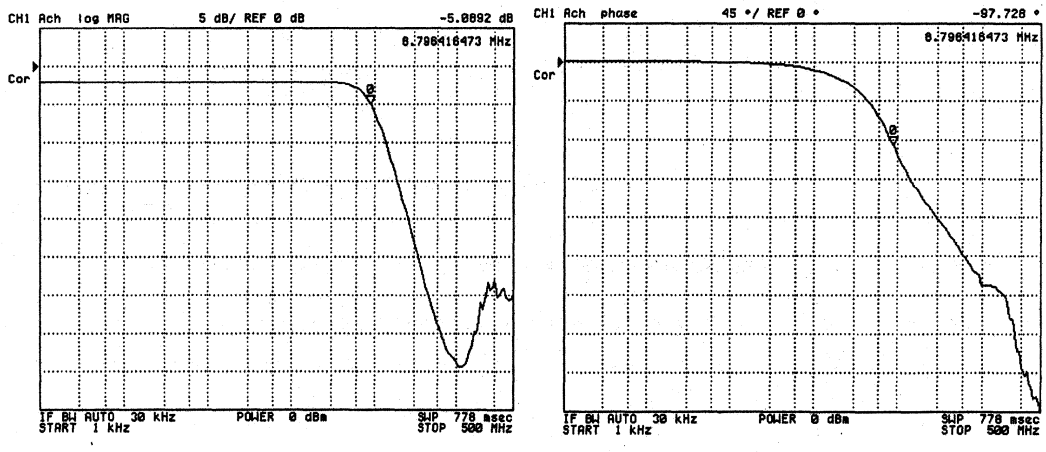


Figure 7. Amplitude and Phase Response of the Filter With R_1 , R_2 = 1 kΩ

The above diagrams (Figure 5) were recorded with a Network Analyzer Type 4395A from Hewlett-Packard. The first diagram shows the amplitude response of the signal versus frequency. The corresponding phase response can be seen on the other diagram.

The results of measurement showed a cutoff frequency of 8.8 MHz with a corresponding phase response of –97.7°. This deviation of 12% from the calculated cutoff frequency has several causes. The THS4001 has an input capacitance of typical 1.5 pF and an open loop gain of 20 dB at 10 MHz. The output capacitance still occurs for this, the load of 100 Ω, and the impedance depending on the layout. To achieve a cutoff frequency of 10 MHz, the measured frequency of 8.8 MHz has to increase by 13.4%. According to Equation 12, the frequency is proportionally opposite to resistance. Since the capacity of 15 pF has a small value against the input capacitance, it is the only possibility for increasing the frequency by decreasing the resistance values by 13.4% (866 Ω). However, lower resistance values result in an increase of the output load with a simultaneous phase shifting. A resistance value of 910 Ω from the E24 series is selected so that the THS4001 output is not burdened too strongly.

Table 3. Modified Values of the Components for a Cut-Off Frequency of 10 MHz

COMPONENTS DESIGNATION	VALUES OF COMPONENTS	
	CALCULATED OR FIXED	USED
C_1 , C_2	15 pF	15 pF
R_1 , R_2	1061 Ω	910 Ω

Using the values shown in Table 3 yields the following results:

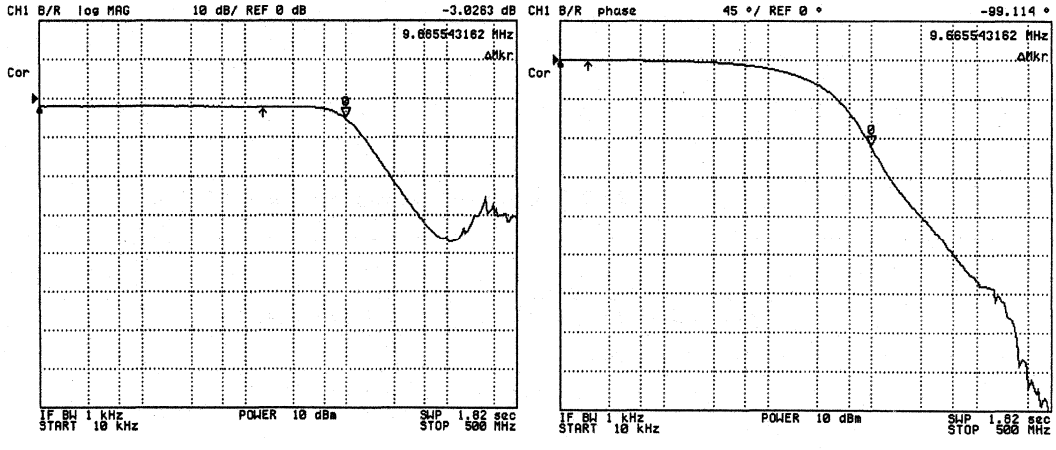


Figure 8. Amplitude and Phase Response of the Filter With R_1 and R_2=910 Ω

The measured response curve agrees with the response expected from a Butterworth filter. The cutoff frequency is 9.7 MHz at a corresponding phase shift of –99°.

The THS4001 has an open loop gain at 100 MHz below 4 dB, according to the data sheet. From this frequency, the acting circuit loses its influence on the frequency response. Without the influence of the THS4001, a passive high-pass filter is formed (see Figure 7). This circuit has a frequency response, which is shown in Figure 8.

The sinking amplification of the THS4001 and the increasing influence of the high-pass filter resulted in a decreasing attenuation. This behavior starts around 100 MHz and can be seen in Figure 6.

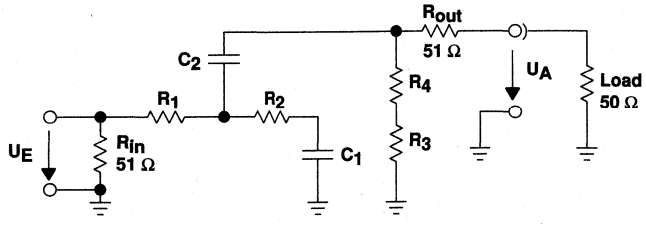


Figure 9. Passive Circuit Around the THS4001

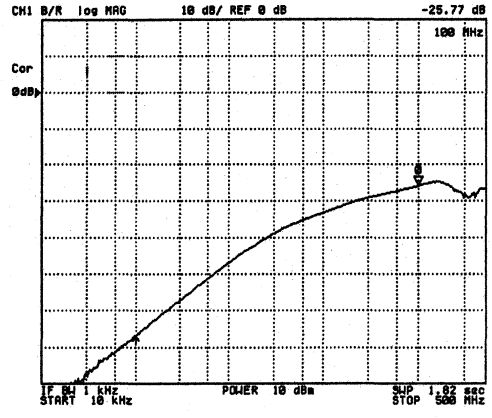


Figure 10. Frequency Responses of Passive Circuit

10 Printed Circuit Board

Figure 9 shows printed-circuit boards as an example of the actual construction of a filter design. In this application, resistors of type 1206 SMD from the E24 series having a tolerance of 1% are used. The inserted capacitors are a part of the E6 series.

In order to decouple and stabilize the supply voltage and prevent any tendency to oscillation, the ceramic 100 nF SMD capacitors C_3 and C_5, having a tolerance of ±5%, are used. For C_4 and C_6, two tantalum chip capacitors with a value of 6.8 µF and a voltage rating of 35 V were chosen. As specified in the data sheet, the supply voltage should be a maximum of ±15 V.

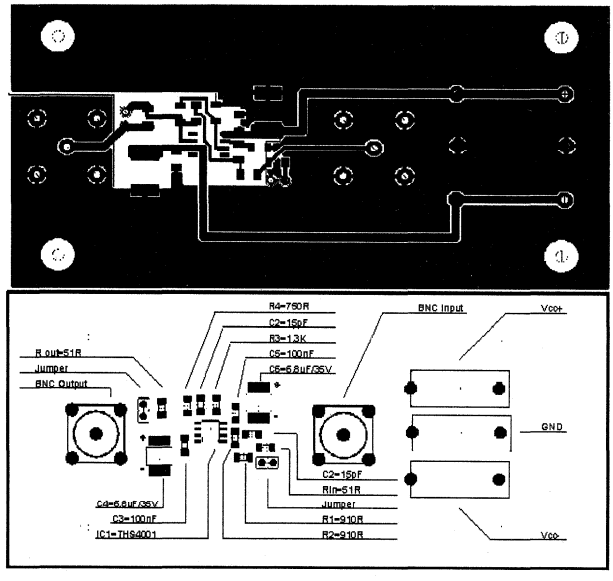


Figure 11. Circuit Board Layout and Component Placement Plan

11 Summary

High frequency filters are typically designed with passive components. But depending on parasitic impedances they are sometimes difficult to design.

Another design uses the THS4001 to build a low-pass filter up to 10 MHz. However, at frequencies above 1 MHz the component values have to be changed from the calculated values. Making C too large has consequences in that R may become so small that additional phases and amplification shift causes errors. If R is too large C may become so small that the parasitic capacitors, together with the amplifier input capacitor, cause errors. A small change in the component values brings the cutoff frequency in the desired direction.

The THS4001 can build an active 2nd order low-pass for high frequencies.

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TEXAS INSTRUMENTS

Application Report
SLOA040 - November 1999

Measuring Differential Gain and Phase

Randy Stephens *Mixed Signal Products*

ABSTRACT

Standard video signals are based on a system developed in the 1950's. The colors and brightness we see on a television screen are encoded within an analog signal. How well an amplifier reproduces this video signal is the foundation for the measurement of differential gain and phase.

The topic of this discussion is the basic concept of differential gain and phase. This discussion will then lead to the analysis of the method used by Texas Instruments to measure differential gain and phase for the high speed amplifier product line—the THS family.

Contents

List of Figures

List of Tables

1 Introduction

Composite video contains the two parts of the video signal—the subcarrier portion and a broadband portion. The broadband portion of the composite video signal controls the brightness, or luminance, of the picture to be displayed. The subcarrier portion of the composite video signal controls the color, or chrominance, of the picture to be displayed. In turn, this color information has two parts to it: the amplitude and the phase. Together, all of these constitute what we see on our television or monitor screens. If any part of the signal is not reproduced correctly, the picture will not be displayed correctly. It could show sunny images as night scenes, or it could show the bright yellow sun as a blue sphere.

One of the most critical factors within a composite video system is how well an amplifier reproduces the composite video signal. A series of tests were conducted to verify if an operational amplifier is useful for video signals. These are called differential gain and phase tests. Even though this is a standardized specification for all manufacturers data sheets, not everyone does it the same way.

Because video information can cover a range from 0 Hz to 6 MHz or greater, the amplifier must have a frequency response of at least 50 MHz to 60 MHz. This precludes the vast majority of amplifiers, and typically leaves the high-speed amplifier product group as the only viable solution for amplifiers within a video system. It may be best to start with the definitions for differential gain and phase.

2 Differential Gain and Phase Definitions

Differential gain is the error in the amplitude of the color signal due to a change in luminance (brightness) level. Basically, the subcarrier reference signal (3.58 MHz or 4.43 MHz) is being offset by a low-frequency ramp going from 0 IRE (0 V) to 100 IRE (714 mV). This signal is then fed through an amplifier configured for a gain of +2 with a fixed load resistance (typically 150 Ω). The change in the amplitude of the subcarrier reference signal being offset by the ramp is called differential gain error. It is usually expressed as a percent error.

Differential gain is important to video signals because if the amplitude of the subcarrier signal changes with a change in luminance level, then the picture being displayed will have color saturation problems. A color with 100% saturation is commonly called a *deep* color. A deep red ball being displayed with bright lights shining on it should not turn dull red when the lights start to dim. It may turn dull red if the saturation level of the base color (red) decreases as the luminance level decreases.

Differential phase is the error in the phase of the color signal due to a change in luminance (brightness) level. The phase of the color signal is responsible for displaying the proper hue, or base color. This measurement follows the exact same procedure as the differential gain measurement, but only looks for the change in phase of the subcarrier reference signal as the offset level changes. Differential phase is usually expressed in degrees.

Differential phase is important to video signals because if the phase of the subcarrier signal changes with a change in luminance level, then the picture being displayed will have color selection problems. For example, a red ball being displayed with bright lights shining on it should not turn orange when the lights start to dim. It may turn orange if the base color information starts to add some green to the image.

Typically, the human eye cannot discern the difference of color saturation if the differential gain error is 1% or lower. Additionally, the human eye cannot discern a hue error of less than 1%. If this is true, then why would anyone want an amplifier with less than 0.5% differential gain or phase error? The reasoning is that there can be several amplifiers along the video signal path. Cascading multiple amplifiers adds both positive and negative differential gain and differential phase errors together. A typical video system will consist of the recording equipment, the transmitter, the receiver, and the display device. So, if there are 20 amplifiers in the entire video signal chain, with each one having a 0.1% differential gain and phase error, then it is probable that the total system will have a differential gain and phase error of 20 × 0.1% or 2%. This is way too high for a good system, not to mention a studio quality system.

3 Differential Gain and Phase Test Setup

Testing differential gain and phase is typically done at the same time. We are interested in the amplitude and phase changes as the offset level is shifted. Because operational amplifiers are commonly used as inverting amplifiers to sum signals together, the offset level will then become inverted. To account for this, Texas Instruments uses a modulated saw-tooth ramp, as shown in Figure 1. It consists of a subcarrier reference signal at either 3.58 MHz (NTSC) or 4.43 MHz (PAL/SECAM) with an amplitude of 40 IRE. A ±100-IRE low-frequency saw-tooth waveform is then used to perform the offset function. This is a standard test signal for both NTSC and PAL. The only slight difference is that PAL uses a 43-IRE subcarrier level instead of the 40-IRE level used by NTSC; but this difference is negligible. Additionally, 100-IRE levels were used instead of 80-IRE levels to fully test the entire operating range of the amplifier under test (AUT).

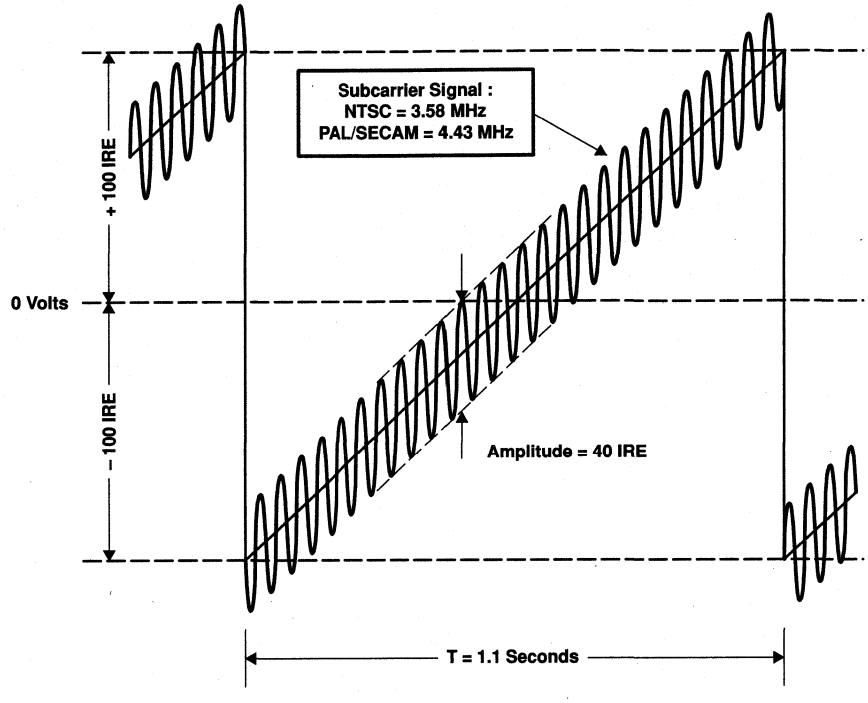


Figure 1. Differential Gain and Phase Test Signal

Some test setups use a staircase ramp instead of the linear ramp. The problem with a staircase ramp is that it does not measure every point. Differential gain and phase errors are not usually proportional to the offset level. In fact, it has been observed on numerous occasions that the maximum errors occurred somewhere between the two end points and not at the ends of the ramp. Considering the unpredictability of the amplifier, discrete steps may not give a true representation of the real differential gain and phase errors.

To accomplish the test using this waveform and to perform the analysis of the operational amplifier, an HP8753D (or E) network analyzer was chosen. An HP3325A function generator is then connected into the bias input port of the network analyzer (see Figure 2). To keep everything correctly timed, the sync output of the function generator is connected to the sync input of the network analyzer. The HP3325A generates the low-frequency saw-tooth waveform, while the HP8753D (or E) applies the high-frequency reference signal (3.58 MHz or 4.43 MHz) on top of the saw tooth. The HP3325A function generator was chosen because it is not influenced by the high-frequency signal being generated by the network analyzer. It was found that other function-generator outputs would be influenced by the subcarrier frequency and would cause the saw-tooth waveform to behave unpredictably.

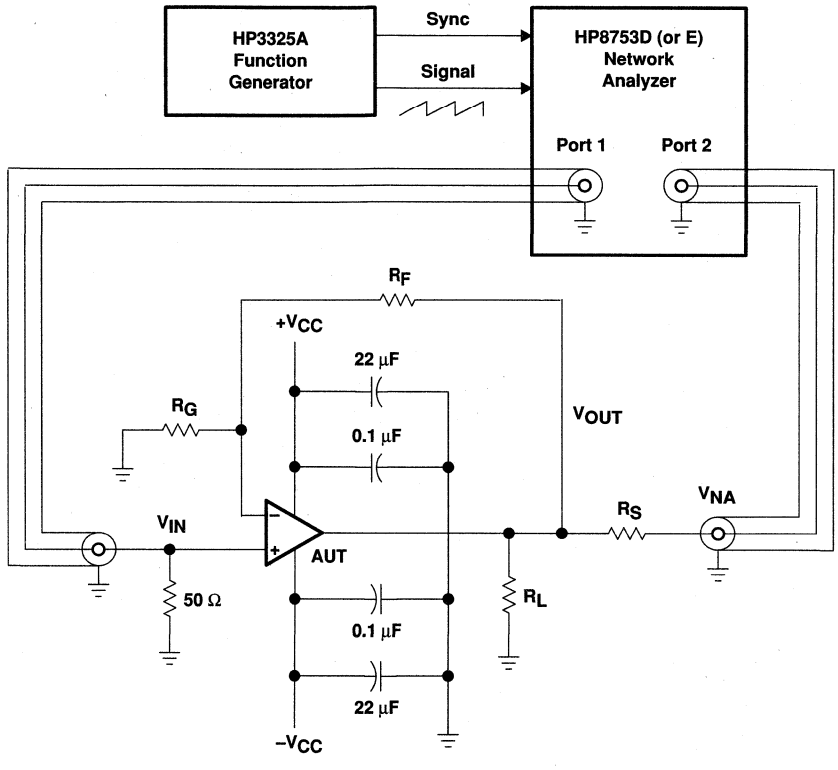


Figure 2. Differential Gain and Phase Test Setup

The AUT is usually set up with a gain of +2 ($R_F = R_G$). This is done because most video systems, not to mention most transmission-line systems, use double termination on the amplifier output. When a double termination is performed, the signal amplitude at the receiving side is reduced by a factor of two. To compensate for this, the driving amplifier is set to a gain of +2.

Although it is realistic to see an amplifier in the inverting configuration, the differential gain and phase tests are done in the noninverting configuration. There are two reasons for this: first, the noise gain of an amplifier is always referred to the noninverting input; so an amplifier set to a gain of –1 is equivalent to a gain of +2 configuration when it comes to amplifier noise gain; the second reason is that a noninverting configuration should theoretically have worse errors than an inverting configuration because the input terminals of the amplifier are held at a fixed reference point (a virtual ground for the inverting terminal). But, in the noninverting gain of +2 configuration, the amplifier's input-circuitry voltage fluctuation is directly proportional to the applied input-signal voltage. If the voltage of the amplifier's input circuitry changes, there is more room for errors to occur due to the reduced common-mode rejection ratio of the op-amp. For these reasons, the AUT is tested with a gain of +2 to provide the worst-case conditions for errors to occur.

Experimentation has shown that the load placed on the amplifier will affect its differential gain and phase measurements. This makes sense, since loading also affects harmonic distortion measurements. Because this is a video specification, a doubly-terminated 75-Ω load, which is the standard video termination, results in an equivalent 150-Ω load to the amplifier. A load higher than 150 Ω should never be used in testing of standard differential gain and phase. The network analyzer has a built-in 50-Ω termination to ground that is always present. So, to accomplish the 150-Ω load, a 100-Ω resistor is used for R_S. A question often asked is will the resistor divider on the output of the AUT affect the differential measurements? The answer is no. It will not affect the measurements because we are dealing with ratios of AUT signals. Since the differential gain (in dB) is found by dividing two ratios, the influence of the resistor divider cancels out.

It is common to use amplifiers to drive multiple video lines. The differential gain and phase measurements are taken for each load to evaluate the effects of driving lower-impedance loads. The equivalent resistance load presented to the AUT is simply 150 Ω divided by the number of lines being driven. To simulate this, the values for R_S and R_L are chosen as follows:

Table 1. AUT Loads for Measuring Differential Gain and Phase

NUMBER OF LINES	EQUIVALENT RESISTANCE (Ω)	R_S (Ω)	R_L (Ω)
1	150	100	–
2	75	50	300
3	50	50	100
4	37.5	50	62
6	25	50	33
8	18.75	50	23

Experience shows that resolution is the most important factor when selecting the measuring instrument to perform these tests. The most common piece of video test equipment found was the Tektronix VM700. But its resolution is only around 0.03% for differential gain, and 0.03° for differential phase. This may be acceptable for many video systems, but not for very high-speed, ultra-low distortion amplifiers.

The HP8753D (or E) was chosen for its great versatility and high resolution. The minimum resolution is 0.001 dB/division for amplitude measurements, and 0.01°/division for phase measurements. A simple mathematical calculation is used to convert from dB to percent error. The details are left to the reader.

$$\%\ Error = \left[10^{(|Gain\ Error\ (dB)|/20)} - 1\right] \times 100 \qquad (1)$$

Where

Gain Error = maximum gain reading—reading at 0 IRE (reference)

When this equation is used, the calculated gain error resolution is approximately 0.0115%/division. This is a respectable figure, but it still has some limitations. Especially when it comes to the high-quality amplifiers produce by Texas Instruments.

4 Testing Differential Gain and Phase

To properly measure differential gain and phase, the test setup should be calibrated first. This is accomplished by first adjusting both channels of the HP8753D (or E) network analyzer to the following settings:

- Sweep type = CW time
- CW frequency = 3.58 MHz (or 4.43 MHz)
- Power = –6.9 dBm (40 IRE)
- IF = 300 Hz
- Number of data points = 401
- Averaging factor = 20 (sometimes higher, depending on signal)
- Smoothing factor = 1% to 5% (depending on amplitude)
- External trigger on sweep

The HP3325A function generator is then adjusted to the following settings:

- Frequency = 0.905 Hz
- Amplitude = 1.428 V_{PP} (± 100 IRE)
- Offset = 0 V
- Function = saw tooth

Once this setup is complete, the output cable on port 1 is connected to the input cable on port 2 with a double female SMA adapter. The network analyzer is set to calibrate mode and allowed to calibrate itself. Then the AUT circuit is place in the test path as shown in Figure 2.

The tests are conducted for both the NTSC subcarrier at 3.58 MHz, and the PAL subcarrier at 4.43 MHz. Additionally, the AUT's power-supply voltages are run at ±15 V and ±5 V at each subcarrier frequency. All of these tests are then repeated using the equivalent loads specified in Table 1. The network analyzer is recalibrated whenever the subcarrier frequency is changed to ensure reliable measurement results.

Once all of the data is taken, the differential gain and phase numbers are extracted. Because differential gain and phase are measurements of error caused by a change in offset voltage, Texas Instruments looks only for the largest change along each of the ±100 IRE signals with the reference signal level at 0 IRE (0 V). The largest difference on gain may be on the +100-IRE magnitude, and on the –100-IRE magnitude for phase. It does not matter where it is, we are simply looking for the worst-case condition. The differential gain error is calculated by using formula (1) for the absolute-maximum difference in gain signal. The differential-phase error is calculated by simply subtracting the absolute-maximum difference from the reference value.

Depending on the signal coming through the setup, the number of averages may need to be increased. This is done specifically when the network analyzer is at its highest resolution settings (0.001 dB and 0.01°). The signal may be very choppy, and increasing the averages will tend to average out random noise from the system.

For very low distortion amplifiers driving a 150-Ω load, the error signal may still be too hard to see. This is where the smoothing function plays a role. Smoothing computes a displayed data point based on a moving average of several adjacent points. Its function is to reduce relatively-small peak-to-peak noise values in the measured data. The minimum smoothing value is used

as much as possible in order to provide accurate results. The drawback to using the smooth function is that the values at the very beginning and the very end of the time-base measurement results may be incorrect. To compensate for this, TI ignores the first and last divisions on the time base results. Since these divisions are ignored, the function-generator frequency is selected so that the offset ramp signal is at –100 IRE (–0.714 V) at 0 seconds, crosses the 0 IRE (0 V) reference point at 0.55 seconds, and is at +100 IRE (+0.714 V) at 1.1 seconds (see Figure 3). The ramp starts at –100 IRE again and continues to rise while the data is still coming through. This compensates for the fact that for the first 0.14 seconds, the data due to possible smoothing errors is ignored. The data from 1.1 to 1.24 seconds is used instead of the data for the first 0.14 seconds. Keeping the smoothing value to 5% or below ensures that no errors are introduced into the readings.

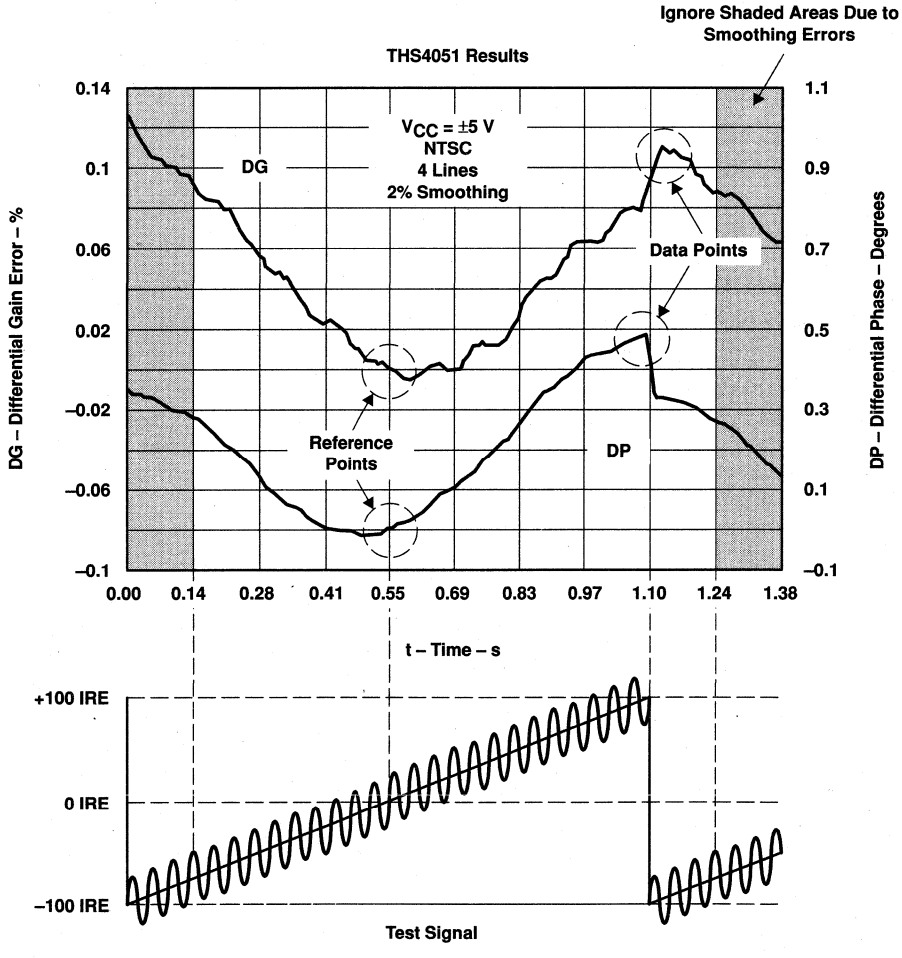


Figure 3. Actual Differential Gain and Phase Results (4 lines = 37.5 Ω)

Figure 3 shows the data points used to find the actual differential gain and phase numbers. These include the 0-IRE reference point and the maximum deviation from each reference point, as indicated in the graph. This graph shows that the worst-case differential gain occurred at –100 IRE (0.11%), and the worst-case differential phase occurred at +100 IRE (0.5°). It does not matter where the maximum error point is relative to the IRE level; only the maximum error relative to the reference points is relevant. For example, the same amplifier was tested with only 2 lines (75-Ω equivalent load). The maximum differential-gain error just happened to occur at +100 IRE (0.02%), and the maximum differential phase error occurred at +100 IRE (0.075°).

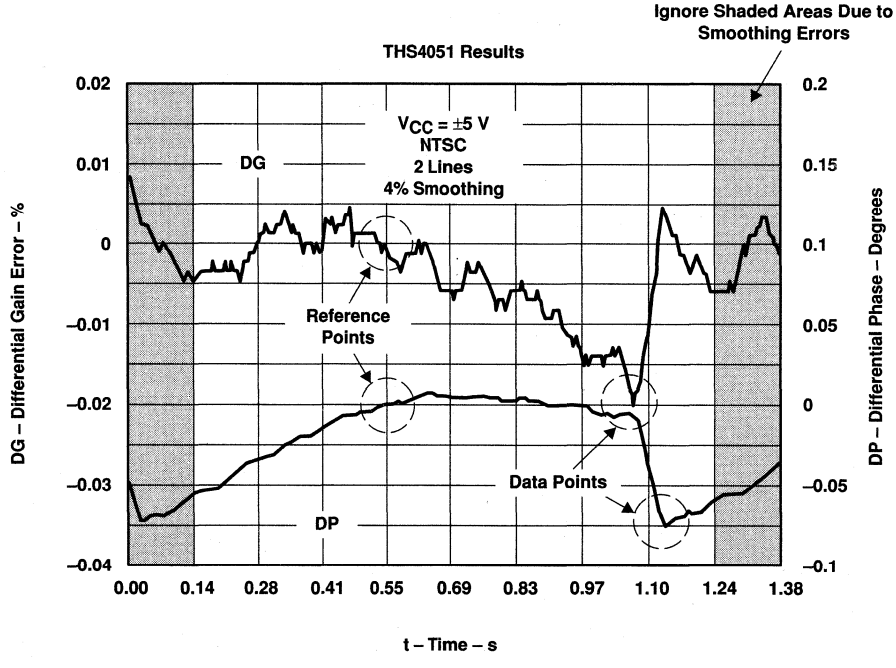


Figure 4. Actual Differential Gain and Phase Results (2 lines = 75 Ω)

There are two network-analyzer settings that may need additional explanation—the 401 data points and the 300-Hz IF bandwidth. The number of data points was selected so that enough points were taken to allow the smoothing factor to average out any random noise within the entire system. If enough data is collected, then random noise should average to a specific level. This level is subtracted from the AUT measurement by the network analyzer after calibration. This subtraction factor should become more consistent from test-to-test as the number of data points is increased. Misleading results will occur if the number of data points is too small.

The 300-Hz IF bandwidth was selected to allow the measurement of extremely small errors. Lowering the IF bandwidth from the network analyzer's default setting of 3,000 Hz will lower the noise floor of the system by about 10 dB. Additionally, lowering the IF bandwidth is better than averaging because it filters out spurious responses, odd harmonics, higher-frequency spectral noise, and line-related noise. When we are looking at operational amplifiers with differential gain and phase errors better than 0.01% and 0.01°, respectively, any reduction in system noise is extremely valuable. The drawback of lowering the IF bandwidth is a dramatic increase in the amount of time required to make one sweep. But this is a small price to pay for good results.

The base-line data in Figure 5 show the actual results after calibrating the system and bypassing the AUT. This was taken with 5% smoothing and 25 averages. The maximum differential gain error shown is 0.0034%, and the maximum differential phase error is 0.0027°.

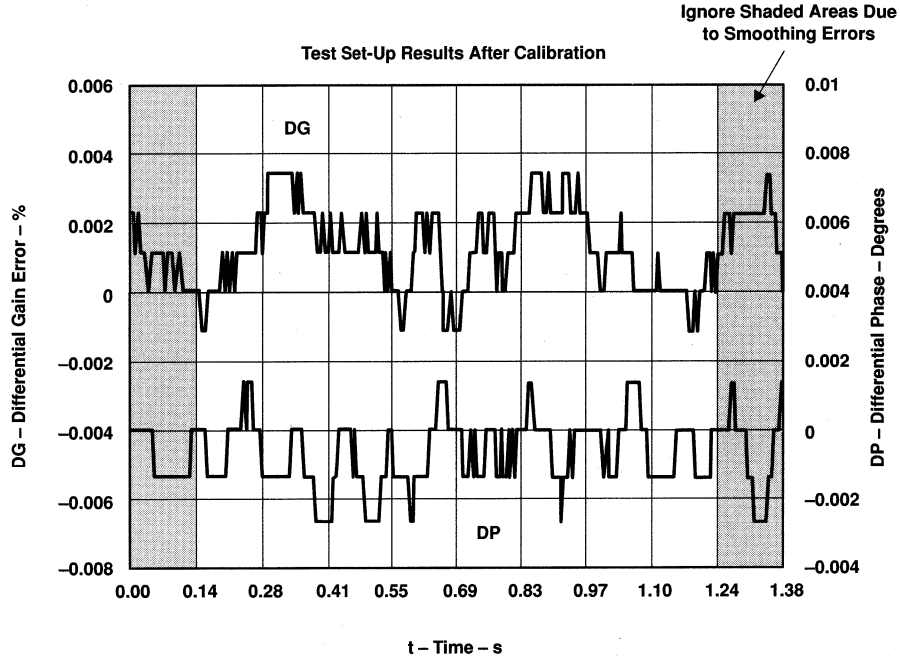


Figure 5. Base-Line Results After System Calibration

Due to the random nature of these values and the amount of uncertainty within the network analyzer, Texas Instruments will not typically publish numbers less than 0.01% and 0.01°. Even though it is quite possible for an amplifier to exhibit better results than these, it would be extremely difficult to prove time-and-time again that the errors are better than 0.01% and 0.01°. Until a new measuring device of higher precision is used, the limits previously shown shall remain a constraint.

5 Summary

The measurement techniques used at Texas Instruments are based on sound engineering methodology. The worst-case errors are used to obtain the values published in any Texas Instruments amplifier data sheet. This is the kind of data any designer should look for when selecting the proper amplifier for a system. Be sure to look at all the test conditions before making any decision on a particular video amplifier. This includes NTSC or PAL subcarrier reference at the 40-IRE amplitude, both +100-IRE and –100-IRE offset tests, proper power supply voltages for the amplifier, amplifier gain, and the load placed on the amplifier's output. Failure to do so may result in unpredictable, and possibly unacceptable, system performance.

Appendix A A Primer for the Composite Video Signal

A.1 Definitions

It is often helpful to understand the composite video signal in its entirety. The National Television System Committee (NTSC) developed this structure in 1953 with approval by the Federal Communications Commission (FCC) in 1954. The NTSC stipulated that the color composite video signal must occupy the same bandwidth as the existing monochrome video signal (for use with black-and-white television sets). Because of this constraint, the video signal (with or without color information) must use the same 0 to 4.2-MHz frequency range. The reasoning is quite simple: it allows both black-and-white and color television sets to use the exact same video signal, while the audio information uses the 4.5-MHz subcarrier.

Another video standard is the phase alternation line (PAL) system. Broadcast of the PAL system in Europe began in 1967. One of the more notable differences was the NTSC use of a 525-line, 60-fields/second, 2:1-interlaced system, while PAL uses a 625-line, 50-fields/second, 2:1-interlaced system. The other big difference that PAL attempted to overcome was the NTSC requirement for very high-quality components in-order to reproduce a video signal with high repeatability. To accomplish this, PAL uses a line-by-line phase reversal of one of the color signal components. The human eye will then hopefully average the potential differences in color lines to reproduce a better picture than NTSC. Despite these differences, both NTSC and PAL have very similar composite video signal wave-shapes and attributes. This primer will concentrate on the NTSC composite video signal for simplicity sake.

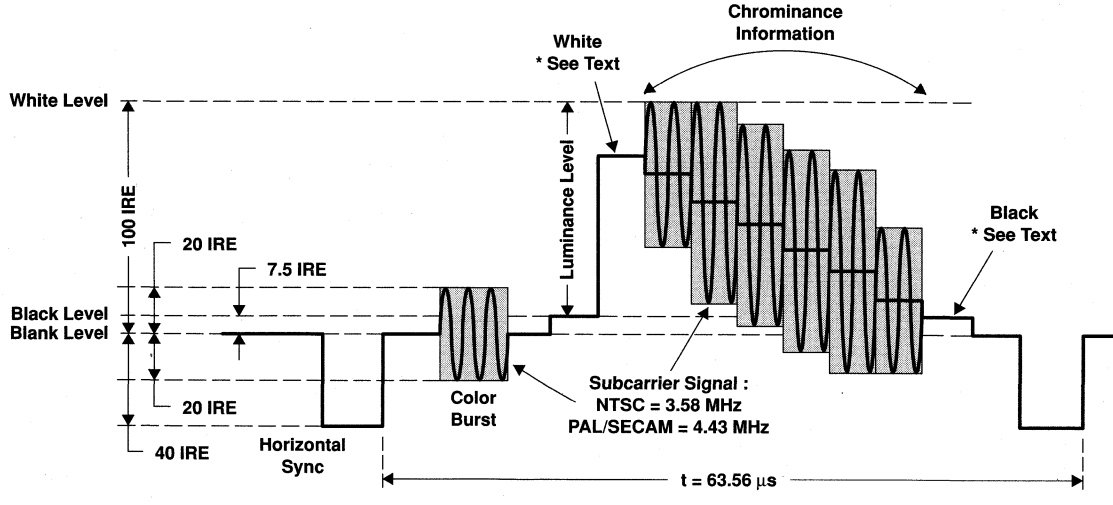


Figure A–1. A Typical 75%-Amplitude, 100%-Saturation Composite Video Signal

The composite video signal includes timing (sync), brightness (luminance), color (chrominance), and color burst information—see Figure A–1. The horizontal-sync pulse is used to keep everything within a video system at the right point in time. It tells the display device where the beginning of a new scan line is. A new scan line is generated every 63.556 µs (15.734 kHz). This concept is very similar to the use of a digital-clock in logic circuitry to keep all the signals at a common reference point in time.

The brightness information is the luminance portion of the composite video signal. Because the human eye is more sensitive to brightness variations, the entire bandwidth (0 to 4.2 MHz) is allocated to reproducing the luminance information. The brighter (or whiter) the picture is, the higher the video-signal amplitude. Video signals use the arbitrary IRE unit for amplitude measurements. A pure-white signal corresponds to a 100-IRE level, while the blanking level, which is blacker than black, corresponds to a 0-IRE level. Sometimes it is required to relate the IRE measurement to volts. The NTSC standard states that 100 IRE should correspond to 714 ±7 mV, while the PAL standard establishes it at 700 ± 7 mV. This difference is generally ignored to keep things simple. The most common conversion used is 1 V_{PP} = 140 IRE, or 1 IRE = 7.14 mV.

The color information (chrominance) is encoded within a subcarrier frequency. For most systems, this subcarrier frequency is 3.579545 MHz ±10 Hz for the NTSC standard, and 4.43361875 MHz ±5 Hz for the PAL standard. There are two parts to the color information: hue and saturation. Hue is technically the wavelength of a color. It can be thought of as the base color within the whole color spectrum. The other part to the color information, saturation, determines the intensity of a specific color. For example, the color red may look very dull with very little saturation, or it may look deep red with very high saturation. The fact that its base color is red still remains.

If the luminance portion takes up the full 0 to 4.2 MHz band, then what is the bandwidth for the color portion? To help answer this, we need to know how the color subcarrier came to be. The first thing to realize is that the NTSC color subcarrier was chosen for a reason. The audio carrier is at 4.5 MHz. The 286^{th} harmonic of the already existing 15.75-kHz monochrome horizontal-scan frequency is about 4.5 MHz. In the color system, this 4.5-MHz frequency is divided by 286 to obtain the new horizontal-scan frequency of 15.743 kHz. This result is within the deviation limit originally set by the NTSC monochrome standards. The luminance information is then based on this 15.743-kHz separation. To minimize the visibility of the color subcarrier, its frequency is chosen to be an odd multiple of one-half the horizontal scan rate. This then performs frequency interleaving (see Figure A–2). The color information is also allowed to have a 0.6 MHz side band. This leaves a maximum upper frequency of 4.2 MHz (from the luminance bandwidth limit)—0.6 MHz = 3.6 MHz. It was found that the 455^{th} harmonic ($5 \times 7 \times 13 = 455$) of one-half the color scan rate (15.743 kHz/2) is equal to 3.579545 MHz.

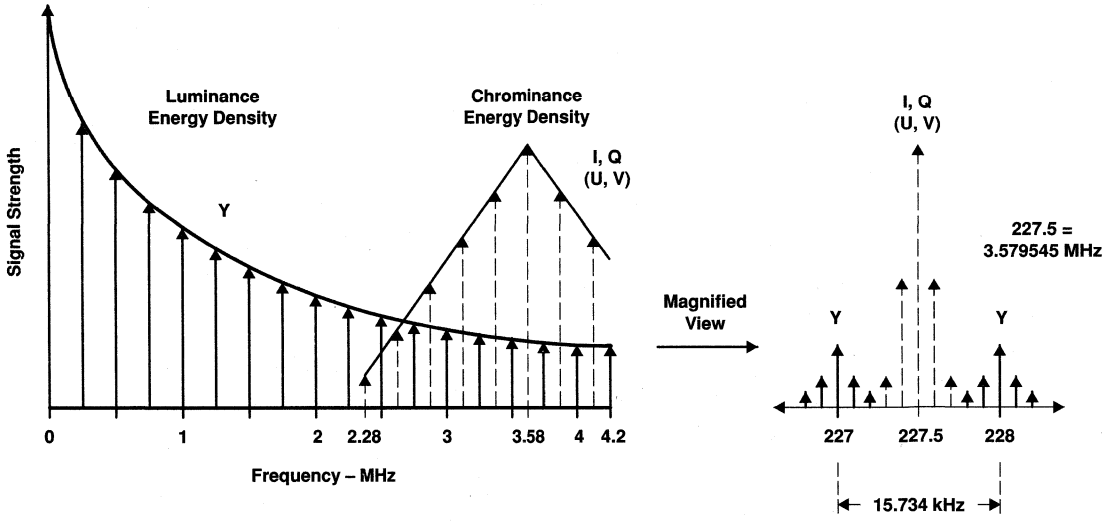


Figure A–2. Frequency Interleaving Spectrum

Let's now find the color information bandwidth. As stated earlier, the color information is allowed a 0.6-MHz side band. All three color components are allowed to use the entire bandwidth for large objects. For medium-sized objects a 1.3-MHz bandwidth is allowed, but is generally limited to two colors. The choice of these colors is discussed further in this document. A filter is placed at 4.2 MHz to insure that the 1.3-MHz upper-side band does not interfere with the sound carrier. Most consumer-grade equipment uses only the 0.6-MHz side bands, while studio quality equipment generally use the fully-allotted spectrum (see Figure A–3).

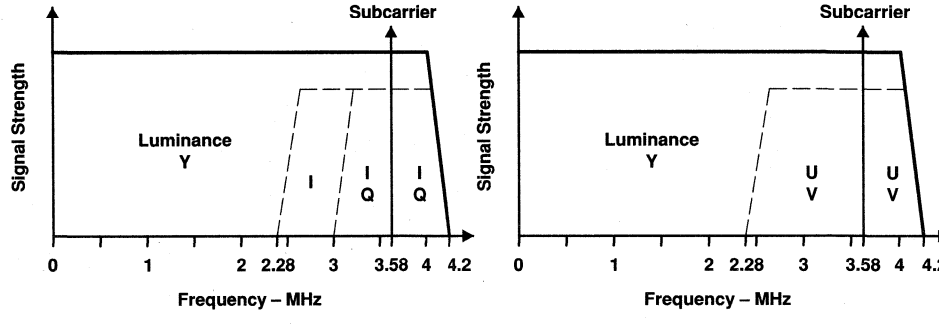


Figure A–3. NTSC Composite Video Frequency Spectrum

The last part to a composite-video signal is the color burst. The color burst tells the video circuit color decoder how to decode the color information contained within the following line of video. It ensures that the colors displayed match those of the original source material. This is accomplished by sending 8 to 11 subcarrier cycles. These cycles are sent in phase with the subcarrier used to record the original picture. The receiving circuitry can then lock this frequency and phase for its own subcarrier oscillator. Because the color burst is only transmitted with color material, the decoding circuitry can tell if the composite video signal is black-and-white or color and adjust its compensation accordingly.

A.2 Creating the Composite Video Signal

Now that we know what the composite-video signal components are, let us see how the picture information is encoded. If the signal is purely monochrome, the video signal only has the luminance component and no color subcarrier component. This is quite straightforward and should be easy to see how a monochrome signal is encoded. The tricky part is getting the hue and saturation components into the composite video signal.

The first and most important part of the composite video signal is the luminance information. The luminance (or brightness) is derived from the gamma-corrected red (R'), green (G'), and blue (B') signals. Gamma correction takes into account the fact that the intensity of the display device (typically a cathode-ray tube—CRT) is proportional to the signal voltage raised to some power (typically 2.2 to 2.6). As a result of this relationship, high-intensity images are even brighter, and low-intensity ones become even darker. To correct for this, the red, green, and blue (RGB) transmitted signal levels are reduced by a factor of 1/2.2 = 0.45. An advantage of this correction is an increase in the signal-to-noise ratio during transmission. For clarification purposes, the component signals are shown below.

$$R_{DISPLAYED} = \left(R_{SIGNAL}\right)^{2.2} \text{ and } R_{TRANSMIT} = \left(R_{SIGNAL}\right)^{0.45} = R' \tag{2}$$

$$G_{DISPLAYED} = \left(G_{SIGNAL}\right)^{2.2} \text{ and } G_{TRANSMIT} = \left(G_{SIGNAL}\right)^{0.45} = G' \tag{3}$$

$$B_{DISPLAYED} = \left(B_{SIGNAL}\right)^{2.2} \text{ and } B_{TRANSMIT} = \left(B_{SIGNAL}\right)^{0.45} = B' \tag{4}$$

When talking about transmitted color components, the gamma-corrected color components (R'G'B') are used for all of the signal levels in the composite-video signal.

The luminance information (or brightness) is formed by the basic R'G'B' color combination. When these signals are set to zero, the luminance information portrays a black color. When the three signals are set to 100% level, the luminance information portrays a white color. It then becomes clear that every other color falling between black and white can be encoded. This allows a black-and-white television set to reproduce an image created from a color source.

The formula for luminance is:

$$Y\ (luminance) = 0.299\ R' + 0.587\ G' + 0.114\ B' \tag{5}$$

We can also see that color weighting is used for the transmission of each color. This is because the human eye is more sensitive to green than to red, and more sensitive to red than to blue. It makes sense to have the dominant portion of the signal be the color that our eyes are most sensitive to. This naturally brings us to how the rest of the color information is encoded.

The hue and saturation information is encoded by using a color-difference formula. This is done by running the luminance (Y) information through an inverter to obtain –Y. This signal is then added to the R' and B' color signals to get:

$$R' - Y = 0.701\ R' + 0.587\ G' + 0.114\ B' \tag{6}$$

$$B' - Y = 0.299\ R' + 0.587\ G' + 0.886\ B' \tag{7}$$

But what about the third color-difference signal, G' – Y? Because the luminance signal incorporates the G' component, sending the G' – Y portion is not required. At the receiver side, to extract the original R'G'B' components, we simply do the following:

$$(R' - Y) + Y = R' \tag{8}$$

$$(B' - Y) + Y = B' \tag{9}$$

$$(Y - R' - B') \times 1.704 = G' \tag{10}$$

or

$$Y - 0.510\ (R' - Y) - 0.194\ (B' - Y) = G' \tag{11}$$

Equations (5) through (11) show that it is only necessary to send two parts of the R'G'B' signal instead of all three. To simplify equations (6) and (7) even further, the color-difference components U and V were created

$$U = 0.492\ (B' - Y) \tag{12}$$

$$V = 0.877\ (R' - Y) \tag{13}$$

To get back to the R'G'B' discrete signals using the U and V methodology, use the following:

$$R' = Y + 1.140\ V \tag{14}$$

$$B' = Y + 2.032\ U \tag{15}$$

$$G' = Y - 0.394\ U - 0.581\ V \tag{16}$$

It is also common to see the I and Q components used in place of U and V. This is done because when medium-size objects are displayed on a screen, the eye is more sensitive to certain colors. These colors are the bluish-greens and the reddish-oranges. Medium-size objects use the full 1.3-MHz lower-side band (LSB) of the subcarrier energy distribution (see Figure A–3). However, the Q signal is filtered to show only the 0.6-MHz LSB portion. So, for medium-size objects, the Q-signal amplitude is reduced to zero. On the other hand, the I signal is allowed to use the full 1.3-MHz LSB spectrum. When only the I signal is used, just the sensitive color range from the bluish-greens to the reddish-oranges is shown (see Figure A–4). Hence, the I and Q scheme was created to exploit the sensitivity of the human eye beyond what the U and V formulas provide.

$$I = 0.596\ R' - 0.275\ G' - 0.321\ B' \tag{17}$$

$$= V\ cos\ 33° - U\ sin\ 33° \tag{18}$$

$$= 0.736\ (R' - Y) - 0.268\ (B' - Y) \tag{19}$$

and

$$Q = 0.212\ R' - 0.523\ G' - 0.311\ B' \tag{20}$$

$$= V\ sin\ 33° - U\ cos\ 33° \tag{21}$$

$$= 0.478\ (R' - Y) + 0.413\ (B' - Y) \tag{22}$$

To get back to the R'G'B' discrete signals using the I and Q methodology, we perform the following:

$$R' = Y + 0.956\ I + 0.620\ Q \quad (23)$$

$$B' = Y - 1.108\ I + 1.705\ Q \quad (24)$$

$$G' = Y - 0.272\ I - 0.647\ Q \quad (25)$$

The I and Q (or U and V) signals are then used to modulate the subcarrier frequency. Using a phase-quadrature mixing scheme produces the chrominance signal. Modulating one signal at a sine phase and adding the other signal, which is modulated with a cosine phase, results in the chrominance-signal formulas:

$$Chrominance\ signal = Q\ sin\ (\omega t + 33°) + I\ cos\ (\omega t + 33°) \quad (26)$$

or

$$Chrominance\ signal = U\ sin\ \omega t + V\ cos\ \omega t \quad (27)$$

Where $\omega = 2\pi F_{SUBCARRIER}$

The hue information is introduced into the signal by a phase shift relative to the subcarrier reference signal, as shown in Equations 26 and 27. For example, the color red is at a phase-shift of 103° relative to the sub-carrier, green is at 241° relative to the subcarrier, and blue is 347° relative to the subcarrier. By setting the correct phase relative to the subcarrier reference signal, any color can be realized on a vector diagram (see Figure A–4). The only thing left to produce the proper color is to find the proper color saturation.

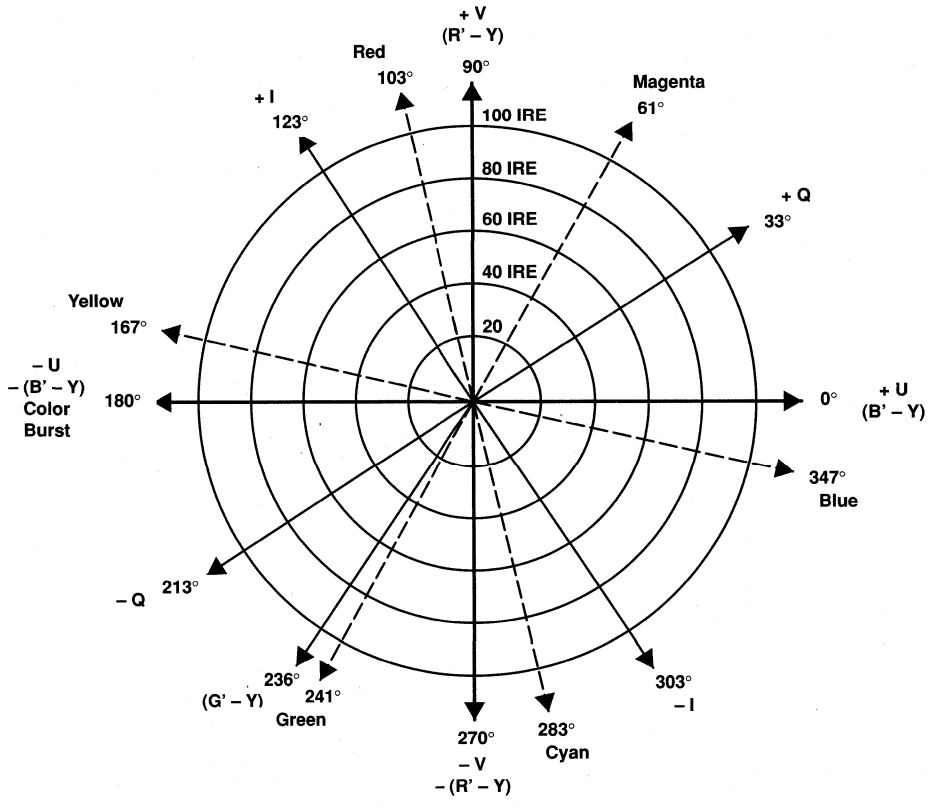


Figure A–4. Vector Diagram

The saturation information is introduced by the ratio of the chrominance amplitude (both hue and saturation) and the corresponding luminance level (see Figure A–5). The chrominance amplitude is easily obtained from the previous formulas by simply using the square root of the sum-of-the-squares method:

$$\textit{Chrominance amplitude} = \sqrt{\left(I^2 + Q^2\right)} = \sqrt{\left(U^2 + V^2\right)} \tag{28}$$

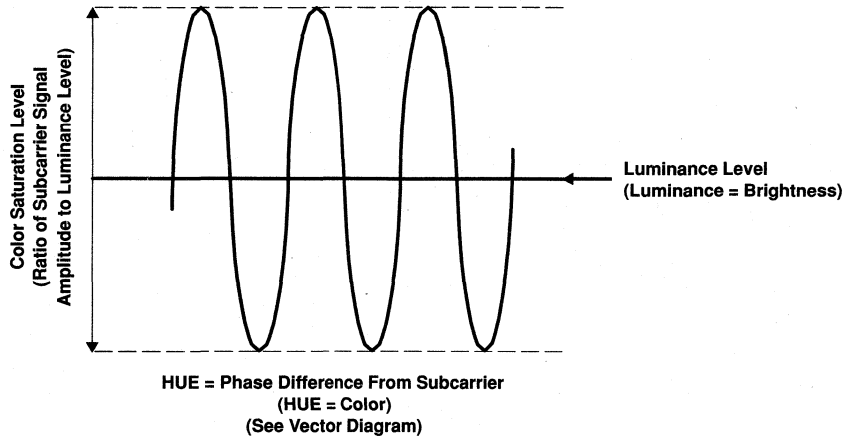


Figure A–5. Chrominance Signal Components

This chrominance signal is then added to the luminance (Y) signal to create the composite-video signal shown in Figure A–1. The additional portions to the composite-video signal are added by different means generally not related to the encoding algorithm. These portions include, but are not limited to, the horizontal sync, color burst, and blanking signals. The exact formula for the composite-video signal is:

$$Chrominance\ NTSC = Y + Q\ sin\ (\omega t + 33°) + I\ cos\ (\omega t + 33°) \tag{29}$$

or

$$Chrominance\ NTSC = Y + U\ sin\ \omega t + V\ cos\ \omega t \tag{30}$$

It may be helpful to note that if no color is encoded, there will be no subcarrier modulation within the composite-video signal. This can be seen in the example composite-video line shown in Figure A–1. The first section within the video information portion shows a flat-luminance line, coupled with no subcarrier amplitude and a high IRE level. This will produce the color white on a screen. Additionally, the last portion shown within the video information with a 7.5 IRE level will show the color black on the screen.

To see all of these concepts and equations in action, let us look at the standard test pattern shown in A of Figure A–6. This represents a single horizontal line being scanned from left to right across the screen. It consists of every combination of the three basic colors; red, green, and blue. B, C, and D of Figure A–6 show the relative saturation levels of the three basic colors using 100% as the maximum saturation level. The luminance formula of Equation 5 using the saturation levels shown results in E of Figure A–6. The next step is to create the I and Q signals using Equations 17 and 20, as shown in F and G of Figure A–6. Using Equations 26 and 27 results in the 3.58-MHz modulated-subcarrier waveform shown in H and I of Figure A–6. Next, combine the chrominance signal (H and I) with the luminance signal (E). Before the final composite waveform is produced, we should take into account that the black level is at 7.5 IRE and not at 0 IRE as mandated by the NTSC. A small correction factor has to be added to account for the 92.5 IRE full scale instead of a 100 IRE full scale. The resulting corrected composite waveform is shown in J of Figure A–6.

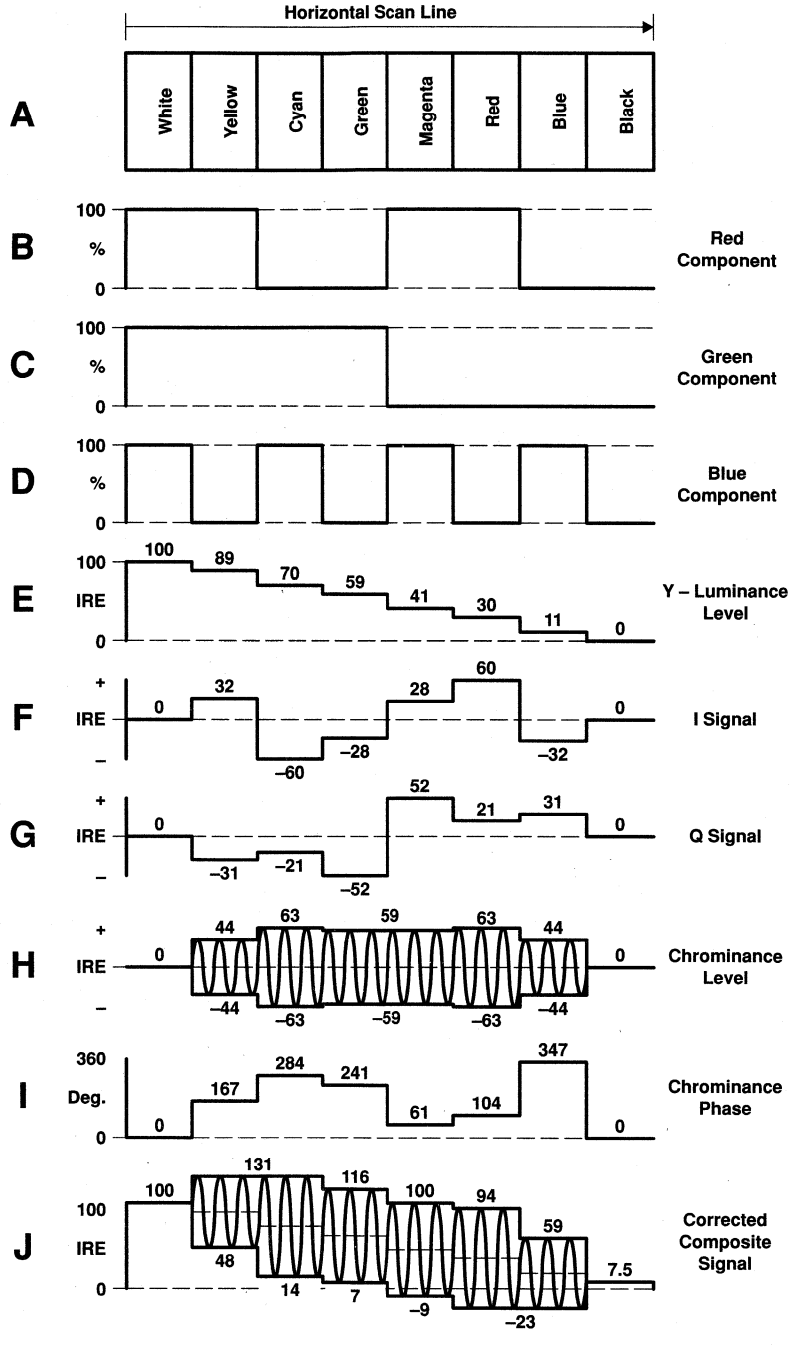


Figure A–6. The Construction of an NTSC Composite Video Signal

There are two standard test-bar patterns used for the NTSC signal. The two types are the 75% amplitude-100% saturation, which is most commonly used, and the 100% amplitude-100% saturation shown in Figure A–6. The *amplitude* number refers to the IRE level required for the color white. The luminance and chrominance levels for the two basic types of color bar formats are listed in Tables A–1 and A–2.

Table A–1. 75% Amplitude, 100% Saturation NTSC Color Bars

COLOR	LUMINANCE (IRE)	CHROMINANCE LEVEL (IRE)	CHROMINANCE PHASE (degrees)
White	76.9	0	0
Yellow	69.0	62.1	167.1
Cyan	56.1	87.7	283.5
Green	48.2	81.9	240.7
Magenta	36.2	81.9	60.7
Red	28.2	87.7	103.5
Blue	15.4	62.1	347.1
Black	7.5	0	0

Table A–2. 100% Amplitude, 100% Saturation NTSC Color Bars

COLOR	LUMINANCE (IRE)	CHROMINANCE LEVEL (IRE)	CHROMINANCE PHASE (degrees)
White	100.0	0	0
Yellow	89.5	82.8	167.1
Cyan	72.3	117.0	283.5
Green	61.8	109.2	240.7
Magenta	45.7	109.2	60.7
Red	35.2	117.0	103.5
Blue	18.0	82.8	347.1
Black	7.5	0	0

PowerPAD™ Made Easy

What is PowerPAD

The PowerPAD package is a thermally enhanced standard size IC package designed to eliminate the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard printed circuit board (PCB) assembly techniques, and can be removed and replaced using standard repair procedures.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC. This provides an extremely low thermal resistance (θ_{JC}) path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the printed circuit board (PCB), using the PCB as a heatsink. In addition, through the use of thermal vias, the thermal pad can be directly connected to a ground plane or special heat sink structure designed into the PCB.

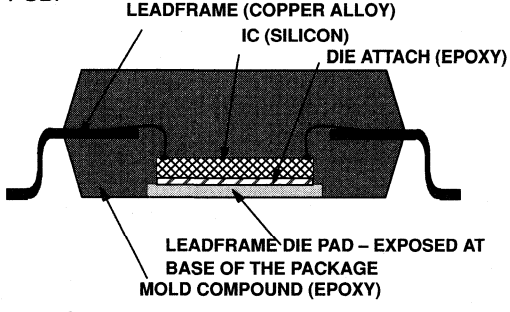


Figure 1. Section View of a PowerPAD Package

PowerPAD Assembly Process

1. Prepare the PCB with a top side etch pattern as shown in Figure 2. There should be etch for the leads as well as etch for the thermal land.
2. Place the recommended number of holes (or thermal vias) in the area of the thermal pad. These holes should be 13 mils in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow. The recommended number of holes for the each of the PowerPAD packages can be located in the application section of the data sheet.
3. It is recommended, but not required, to place a small number of the holes under the package, but outside the thermal pad area. These holes provide additional heat path between the copper land and ground plane and are 25 mils in diameter. They may be larger because they are not in the area to be soldered, so wicking is not a problem. This is illustrated in Figure 2.

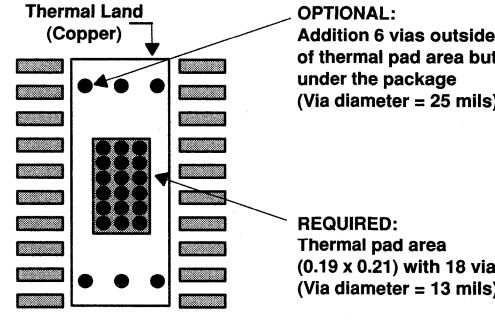


Figure 2. 20-Pin DWP PowerPAD PCB Etch and Via Pattern

4. Connect all holes, including those within the thermal pad area and outside the pad area, to the internal ground plane or other internal copper plane.
5. When connecting these holes to the ground plane, do **not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated through hole.

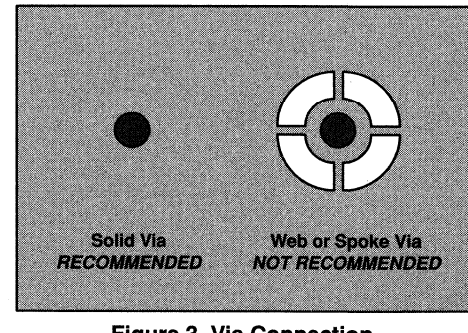


Figure 3. Via Connection

6. As illustrated in Figure 2, the top-side solder mask should leave exposed the terminals of the package and the thermal pad area. The thermal pad area should leave the 13 mil holes exposed. The larger 25 mil holes outside the thermal pad area should be covered with solder mask.
7. Apply solder paste to the exposed thermal pad area and all of the package terminals.
8. With these preparatory steps in place, the PowerPAD IC is simply placed in position and run through the solder reflow operation as any standard surface mount component. This results in a part that is properly installed.

For detailed information on the PowerPAD package including thermal modeling considerations and repair procedures, please see SLMA002 Technical Brief *PowerPAD Thermally Enhanced Package.*

TEXAS INSTRUMENTS

Application Report
SLOA035 - October 1999

Selecting an Amplifier for a Data Converter

Patrick Rowland *Mixed Signal Products*

ABSTRACT

This application report discusses various considerations that must be taken into account when interfacing general-purpose amplifiers and analog-to-digital converters. The report discusses bandwidth, resolution, analog ADC input drive, and power supply considerations for both parts.

Contents

List of Figures

1 Introduction

This application report discusses various considerations that must be taken into account when interfacing general-purpose amplifiers and analog-to-digital converters (ADC). As used here, *general-purpose* means voltage feedback (VFB) amplifiers of a bandwidth <10 MHz, and, typically, successive approximation ADCs between 8–12 bits with speeds <2 MSPS. Many of these same items can be applied to higher-speed or higher-resolution systems, but there are other design considerations specific to such systems that this report does not address.

This report discusses bandwidth, resolution, analog ADC input drive, and power supply considerations for both parts.

Figure 1 shows the amplifier – ADC interface.

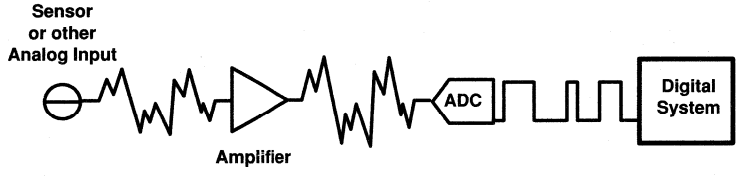


Figure 1. Amplifier and ADC

2 Bandwidth

Choosing an ADC that meets the system requirements for resolution and speed is the first priority. Other considerations such as power or interface will also come into play, but once the bandwidth of the ADC has been determined, an amplifier can be chosen to go with it. With regard to bandwidth, most applications using general-purpose ADCs will observe Nyquist and sample at greater than twice the highest frequency of interest to avoid aliasing.

With VFB amplifiers, gain bandwidth product (GBP) is the specification of interest when looking at small signal bandwidth. Because the VFB amplifier is dependent on the gain that is being employed, the frequency of the signal of interest multiplied by the gain must be less than the GBP for the amplifier.

$$Frequency \times Gain < GBP \quad (1)$$

It is good design practice to ensure the GBP of the amplifier has some amount of extra margin. This ensures that system variability does not press beyond the amplifier's capability.

When referring to GBP, use the graphs in the back of most amplifier datasheets, because GBP is often dependent on the supply voltage. As an example, Figure 2 shows that the TLV2460 has a delta of 40 kHz of GBP across the full Vcc range for the device.

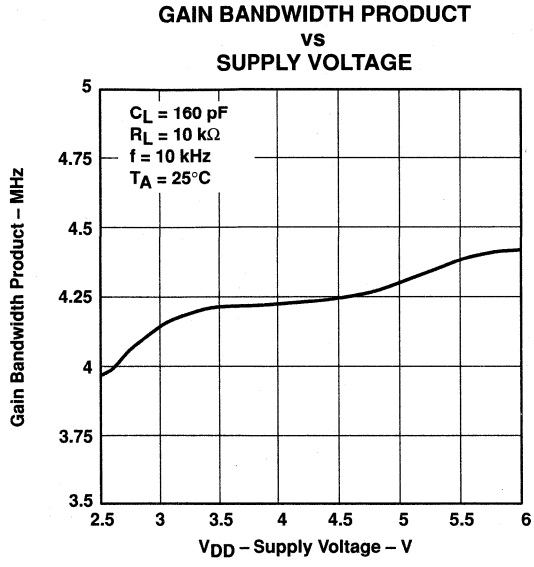


Figure 2. Typical Gain Bandwidth Product Graph (TLV2460)

The other specification that is of interest with respect to large signal bandwidth is slew rate. Denoted in volts per microsecond (V/μs), slew rate is the ability of the amplifier to react to step inputs and slew an output across the amplifier's dynamic range. To ensure an amplifier has sufficient slew rate for a given application, a rough calculation can be made.

For example, consider the TLV2460 again with a typical slew rate of 1.6 V/μs. The graph in the datasheet shows that using this part with a 3-V supply will result in roughly 1.6 V/μs or greater. Now, using a signal with frequency (f) equal to 2 MHz is well within the GBP of the amplifier at 3 V. Since f = 2 MHz and is equal to f = 1/0.05 μs we can compare the amplifier's slew rate and calculate what it can support in signal slew rate. Amplifier slew rate must be greater than or equal to the signal slew rate in this case:

$$\frac{1.6\ V}{1\ \mu s} > \frac{x}{0.5\ \mu s} \tag{2}$$

Where solving shows that x is less than or equal to 0.8 V. Thus, the largest peak-to-peak voltage the TLV2460 can support at 2 MHz is 0.8 V.

3 Resolution and Amplifiers

Other product specifications are used to choose an amplifier that matches the resolution of the ADC. A familiar formula is:

$$SNR\ dB = 6.02 \times n\text{–}1.76 \tag{3}$$

OR

$$n = \frac{(SNR\ dB + 1.76)}{6.02} \tag{4}$$

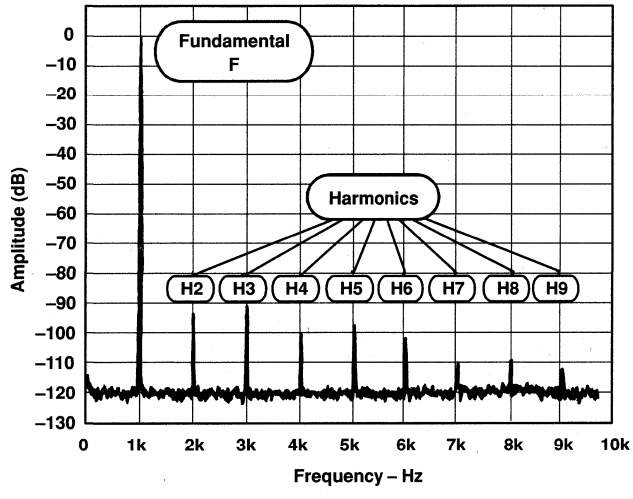
and is used to estimate the resolution needed in an application. In this equation, signal-to-noise ratio (SNR) is an ideal ratio in decibels, and n is an ideal number of bits. This equation offers a mathematical baseline, though *real* SNR must be used to match an amplifier with an ADC.

SINAD offers this real SNR, since it takes into account noise and distortion. SINAD is defined as:

$$SINAD = SNR + D = \frac{1}{THD + N} \tag{5}$$

NOTE: These numbers are scalar and not in dB.

SNR is the ratio of energy in the fundamental signal and the energy in noise. Total harmonic distortion (THD) is a similar ratio between the energy in the harmonics and the energy in the fundamental.



$$\text{SNR (dB)} = 20 \times \log \frac{E_F}{E_N}$$

$$\text{THD (dB)} = 20 \times \log \frac{\sqrt{E_{H2}{}^2 + \ldots + E_{H9}{}^2}}{E_F}$$

$$\text{THD+N (dB)} = 20 \times \log \frac{\sqrt{E_{H2}{}^2 + \ldots + E_{H9}{}^2 + E_N{}^2}}{E_F}$$

$$\text{SINAD} = \text{SNR} + \text{D} = \frac{1}{\text{THD} + \text{N}}$$

Figure 3. SNR and THD Pictorial

SINAD takes into account the harmonics and the noise energy, and thus produces a real SNR that can lead to the effective number of bits (ENOB) in ADCs and amplifiers. ENOB is defined as:

$$ENOB = \frac{[(SINAD\ dB) - 1.76]}{6.02} \tag{6}$$

Data converter specifications will offer either SNR + D or THD + N in dB; thus, this equation is easy to use. Conversely, amplifier specifications usually specify SNR + D or THD + N in percent instead of dB. This requires some mathematical manipulation to use the same equations.

Translating percent to dB is straightforward. For example, the following steps translate THD + N% to THD + N dB, but the same steps can be used to translate SNR + D or SINAD from percent to dB.

$$\frac{THD + N\%}{100} = THD + N \tag{7}$$

Then

$$20\ log\ (THD + N) = THD + N\ dB \tag{8}$$

This can be put into one mathematical expression,

$$20\ log_{10}\left(\frac{THD + N\%}{100}\right) = THD + N\ dB \tag{9}$$

but it is often useful to have the intermediate step of a scalar number, because equation (5) is also stated in scalar numbers. To use this equation in dB, remember:

$logB^A = A \times logB$ and thus, equation (5) in dB is :

$$SINAD\ dB = SNR + D\ dB = (THD + N\ dB)^{-1} = -(THD + N\ dB) \tag{10}$$

The ability to convert between percent and dB simplifies matching the appropriate SINAD specifications between an amplifier and an ADC without. Ideally, choosing an amplifier and an ADC that have the same SINAD realizes the full potential of the signal chain. In practice, choosing an amplifier that has a slightly higher SINAD ensures that it does not degrade the system performance.

For example, the TLV1572 ADC has a typical SNR+D of 58 dB that equates to an ENOB of 9.35 bits. An amplifier like the TLV2770 is an excellent choice to drive this ADC. The TLV2770 has more than sufficient GBP (5.1 MHz typical) to place significant gain on the input signal. Also, the THD+N graphs in the back of the TLV2770 datasheet match the performance of the TLV1572 in nearly all cases, with the only exception being a relatively high supply voltage and high signal gain.

4 Analog-to-Digital Converter Analog Input

Figure 4 shows an example of driving the input of an ADC.

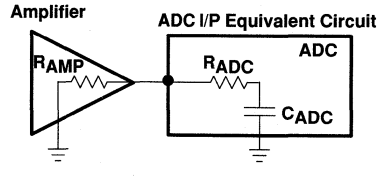


Figure 4. Amplifier–ADC Interface

Figure 5 shows the simplified equivalent RC circuit.

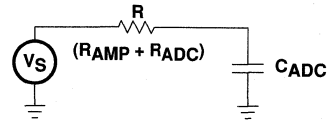


Figure 5. Amplifier–ADC Interface Equivalent Circuit

This assumes that R is the combination of the internal ADC equivalent resistance and the amplifier output resistance. If a significant external resistance were present in series between the two devices, such as PCB trace impedance, it would also need to be added. This gives a simple equivalent circuit model for the system. In this model, three items need to be accounted for with respect to the analog input of the ADC:

- The RC time constant created
- Having sufficient drive current
- Correctly biasing the input signal to the ADC

4.1 RC Time Constant

The following equation can be used to calculate the time constant for the circuit:

$$\tau = RC \tag{11}$$

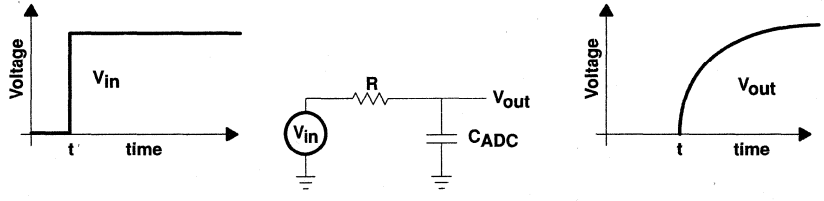


Figure 6. RC Pictorial

The optimal configuration is to have the amplifier drive directly into the ADC, as any additional external resistance will affect τ . If additional external resistance exceeding that specified in the ADC datasheet is necessary, it is extremely important to calculate τ and check it against the sample time of the ADC. This ensures the circuit has time to charge the input capacitor before the input signal is held by sample-and-hold circuitry, and the analog-to-digital conversion begins.

4.2 Drive Current

Drive current from the amplifier is another consideration in driving the analog input of an ADC. Without enough drive current, the same issue of not presenting the correct signal to the ADC occurs as mentioned previously with respect to τ. Looking again at the simplified circuit, there are many equations that govern what current is flowing at any given time.

Considering only the worst-case current demand ensures that the amplifier can help us get a rough idea of the appropriate amount of current needed. Using the simplified model circuit permits examining this circuit with a step function response between the two most extreme potentials.

For example, consider the case where the circuit is in steady state at the highest potential and immediately switches to the lowest.

This circuit is governed over time by the equation:

$$V(t) = V_o e^{\pm(t/RC)} \tag{12}$$

where V_O is the steady state V on the capacitor. Assuming the input voltage at the voltage source (V_S) is steady from $t = -\infty$ up until $t = 0$, it can be determined that $V_O = V_S$. The simple explanation is that, in a dc steady state, the capacitor acts like an open circuit, thus having the same voltage as V_S.

To further simplify the analysis, assume that V_S switches from a known voltage to ground. Thus the circuit turns into a simple RC circuit.

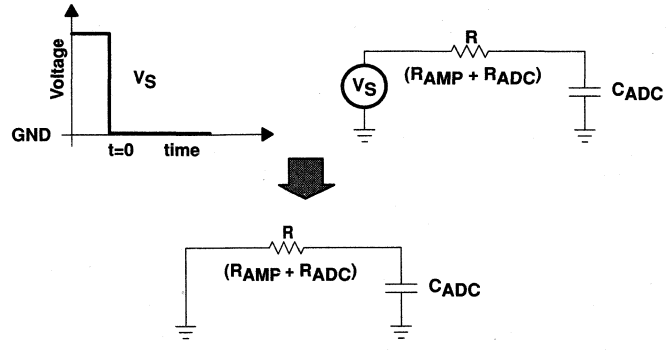


Figure 7. Circuit Simplification

It is intuitive that where t = 0, or right at the switch in potential, the current is the greatest while the voltage exponentially decays over time. The largest current the amplifier needs to handle can then be calculated roughly as:

$$I = \frac{V(t)}{R} \quad \text{Where } t = 0. \tag{13}$$

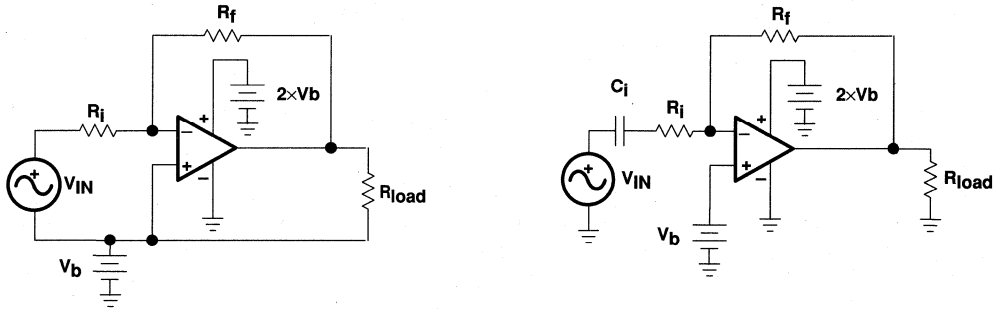
For example, using the TLV1544 ADC gives approximate values of R=1 kΩ and C=55 pF. The time constant τ can then be calculated as in the previous section, given the input resistance on a prospective amplifier. If the largest input voltage to the TLV1544 will be 3 V, the amplifier needs to source roughly 3 mA, again depending on the output resistance of the amplifier.

4.3 Signal Bias

Using the proper signal bias to the input waveform is another important consideration regarding the analog input of the ADC. Different ADCs have different analog input ranges.

For example, the TLV1572 has a single-ended analog input with a voltage range that extends .3 V beyond each rail. Conversely, the TLV1562 allows single-ended inputs similar to the TLV1572, and differential inputs (approximately 2 Vpp) operated in a different mode. Furthermore, some converters like the TLC320AD50 use a completely differential input structure. Understanding what the analog input voltage range looks like allows the designer to properly gain and bias an input signal and take advantage of the full dynamic range of the ADC.

Many circuits exist that properly bias an analog input signal. Two proven circuits for this function per the 1998 TI Analog Seminar are included below. Both circuits bias an ac input signal at mid-rail on a single supply amplifier.



Two examples for proper signal biasing fora single supply amplifier application

Figure 8. Input Signal Biasing Circuits

Input offset voltage (V_{io}) is another parameter to consider on the amplifier. Even in a simple biasing or buffering application the amplifier introduces a dc error induced by the voltage difference inherent to the amplifier inputs and denoted in the datasheet by V_{io}.

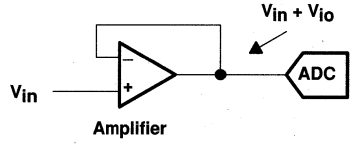


Figure 9. Input Offset Voltage (V_{io})

5 Power Supply

Of course, devices used in the design must be able to withstand and function with the voltages used on a board. While this is obvious, there are other less obvious points that need to be explored, including power and ground planes, input/output voltage range, and the size of 1 LSB on the ADC.

5.1 Power and Ground Planes

Ideally, a board has both an analog and a digital ground plane. This helps isolate sensitive analog circuits—like an amplifier-from switching noise associated with the digital circuits. If a separate analog supply and ground plane are not possible, the power supply rejection ratio (PSRR) specification identifies problems that may be encountered from power supply noise. For newer amplifiers like the TLV2450, there is often a PSRR vs frequency graph in the back of the datasheet that can help if a designer understands the frequency characteristics of noise being encountered on the power rail.

5.2 Input/Output Voltage Range

Another effect of choosing any V_{CC} can be the input and output voltage range on the amplifier. Up until relatively recently, most amplifiers did not supply inputs and outputs that could swing to both rails. For example, the TLC2272 provides rail-to-rail outputs (RRO) but not rail-to-rail inputs (RRI). Instead, the TLC2272 has 1.5 V of headroom on the upper rail of the input. Thus, on a 10 V supply, the TLC2272 has an input range from GND to 8.5 V. Similarly, for a V_{CC} of 5 V, the TLC2272 still has 1.5 V of headroom and an input range from GND to 3.5 V.

The evolution of the amplifier has led to the innovation of rail-to-rail input and output (RRIO) amplifiers such as the TLV2462. RRIO amplifiers allow signals to swing between both rails, thus eliminating headroom on the inputs or outputs. This becomes increasingly important in low voltage applications, as a designer has a smaller input/output range with which to work.

5.3 LSB on the ADC

An ADC specification that varies with Vcc levels is the size of one least significant bit (LSB). This becomes clear with the following equation:

$$1\ LSB = \frac{Vfullscale}{2^N - 1} \tag{14}$$

Where n = resolution of the ADC

For the case of a 12-bit (ENOB) ADC, moving from a 5-V to 3-V full scale range results in a reduction in size of 1 LSB from 1.22 mV to 732 μV. For an ADC like the TLV1572 with a V_{CC} range of 2.7 to 5.5 V, this results in a range of LSB size (5.37 mV to 2.64 mV). The main concern is that, particularly in moving a system to a lower voltage, the LSB does not shrink to the point of being susceptible to system parasitics.

6 Summary

This report briefly covered various considerations to consider when interfacing a general-purpose amplifier to a general-purpose ADC. With these things in mind, it should be straightforward to sift through many amplifier choices and find parts that interface nicely to an ADC and optimize system performance.

Summary Checklist

- Bandwidth – amplifier GBP vs ADC speed
- Resolution – amplifier SINAD vs ADC ENOB
- Analog Input – τ, drive current, and input signal vs ADC analog input range
- Power – amplifier PSRR, amplifier I/O voltage range, and ADC LSB

7 References

5. *Electric Circuit Analysis Second Edition*, by Johnson, Johnson, and Hilburn Copywrite 1992, Prentice Hall, Englewood Cliffs NJ
6. *DSP/Analog Technologies 1998 Seminar Series*, by Texas Instruments Incorporated Copywrite 1998

Stability Analysis of Voltage-Feedback Op Amps Application Report

Including Compensation Techniques

Ron Mancini

Literature Number: SLOA020
July 1999

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Contents

List of Figures

Stability Analysis of Voltage-Feedback Op Amps Including Compensation Techniques

Ron Mancini

ABSTRACT

This report presents an analysis of the stability of voltage-feedback operational amplifiers (op amp) using circuit performance as the criteria to attain a successful design. It discusses several compensation techniques for op amps with and without internal compensation.

Introduction

Voltage feedback amplifiers (VFA) have been with us for about 60 years, and they have been problems for circuit designers since the first day. You see, the feedback that makes them versatile and accurate also has a tendency to make them unstable. The operational amplifier (op amp) circuit configuration uses a high gain amplifier whose parameters are determined by external feedback components. The amplifier gain is so high that without these external feedback components, the slightest input signal would saturate the amplifier output. The op amp is in common usage, so this configuration is examined in detail, but the results are applicable to many other voltage feedback circuits. Current feedback amplifiers (CFA) are similar to VFAs, but the differences are important enough to warrant CFAs being handled in a separate application note.

Stability as used in electronic circuit terminology is often defined as achieving a nonoscillatory state. This is a poor, inaccurate definition of the word. Stability is a relative term, and this situation makes people uneasy because relative judgments are exhaustive. It's easy to draw the line between a circuit that oscillates and one that does not oscillate, so we can understand why some people believe that oscillation is a natural boundary between stability and instability.

Feedback circuits exhibit poor phase response, overshoot, and ringing long before oscillation occurs, and these effects are considered undesirable by circuit designers. This application note is not concerned with oscillators; thus, relative stability is defined in terms of performance. By definition, when designers decide what tradeoffs are acceptable they determine what the relative stability of the circuit is. A relative stability measurement is the damping ratio (ζ) and the damping ratio is discussed in detail in Reference 1. The damping ratio is related to phase margin, hence phase margin is another measure of relative stability. The most stable circuits have the longest response times, lowest bandwidth, highest accuracy, and least overshoot. The least stable circuits have the fastest response times, highest bandwidth, lowest accuracy, and some overshoot.

Amplifiers are built with active components such as transistors. Pertinent transistor parameters like transistor gain are subject to drift and initial inaccuracies from many sources, so amplifiers being built from these components are subject to drift and inaccuracies. The drift and inaccuracy is minimized or eliminated by using negative feedback. The op amp circuit configuration employs feedback to make the transfer equation of the circuit independent of the amplifier parameters (well almost), and while doing this, the circuit transfer function is made dependent on external passive components. The external passive components can be purchased to meet almost any drift or accuracy specification; only the cost and size of the passive components limit their use.

Once feedback is applied to the op amp it is possible for the op amp circuit to become unstable. Certain amplifiers belong to a family called internally compensated op amps; they contain internal capacitors which are sometimes advertised as precluding instabilities. Although internally compensated op amps should not oscillate when operated under specified conditions, many have relative stability problems that manifest themselves as poor phase response, ringing, and overshoot. The only absolutely stable internally compensated op amp is the one lying on the workbench without power applied! All other internally compensated op amps oscillate under some external circuit conditions.

Noninternally compensated or *externally* compensated op amps are unstable without the addition of external stabilizing components. This situation is a disadvantage in many cases because they require additional components, but the lack of internal compensation enables the top-drawer circuit designer to squeeze the last drop of performance from the op amp. You have two options: op amps internally compensated by the IC manufacturer, or op amps externally compensated by you. Compensation, except that done by the op amp manufacturer, must be done external to the IC. Surprisingly enough, internally compensated op amps require external compensation for demanding applications.

Compensation is achieved by adding external components that modify the circuit transfer function so that it becomes unconditionally stable. There are several different methods of compensating an op amp, and as you might suspect, there are pros and cons associated with each method of compensation. Teaching you how to compensate and how to evaluate the results of compensation is the intent of this application note. After the op amp circuit is compensated, it must be analyzed to determine the effects of compensation. The modifications that compensation have on the closed loop transfer function often determine which compensation scheme is most profitably employed.

Development of the Circuit Equations

A block diagram for a generalized feedback system is shown in Figure 1. This simple block diagram is sufficient to determine the stability status of any system.

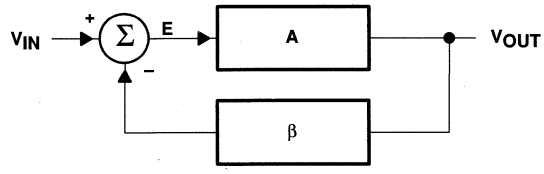

Figure 1. Feedback System Block Diagram

The output and error equations are written below.

$$V_{OUT} = EA \tag{1}$$

$$E = V_{IN} - \beta V_{OUT} \tag{2}$$

Combining equations 1 and 2 yields equation 3:

$$\frac{V_{OUT}}{A} = V_{IN} - \beta V_{OUT} \tag{3}$$

Collecting terms yields equation 4:

$$V_{OUT}\left(\frac{1}{A} + \beta\right) = V_{IN} \tag{4}$$

Rearranging terms yields the classic form of the feedback equation.

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \tag{5}$$

Notice that equation 5 reduces to equation 6 when the term Aβ in equation 5 becomes very large with respect to one. Equation 6 is called the ideal feedback equation because it depends on the assumption that Aβ >>1, and it finds extensive use when amplifiers are assumed to have ideal qualities. Under the conditions that Aβ >>1, the system gain is determined by the feedback factor β. Stable passive circuit components are used to implement the feedback factor, thus the ideal closed loop gain is predictable and stable because β is predictable and stable.

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{\beta} \tag{6}$$

The quantity Aβ is so important that it has been given a special name, loop gain. Consider Figure 2; when the voltage inputs are grounded (current inputs are opened) and the loop is broken, the calculated gain is the loop gain, Aβ. Now, keep in mind that this is a mathematics of complex numbers which have magnitude and direction. When the loop gain approaches minus one, or to express it mathematically $1\angle 180°$, equation 5 approaches infinity because $1/0 \Rightarrow \infty$. The circuit output heads for infinity as fast as it can using the equation of a straight line. If the output were not energy limited the circuit would explode the world, but it is energy limited by the power supplies so the world stays intact.

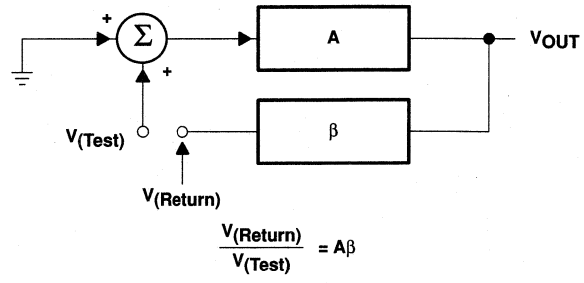

Figure 2. Feedback Loop Broken to Calculate Loop Gain

Active devices in electronic circuits exhibit nonlinear behavior when their output approaches a power supply rail, and the nonlinearity reduces the amplifier gain until the loop gain no longer equals $1\angle 180°$. Now the circuit can do two things: first, it could become stable at the power supply limit, or second, it can reverse direction (because stored charge keeps the output voltage changing) and head for the negative power supply rail.

The first state where the circuit becomes stable at a power supply limit is named lockup; the circuit will remain in the locked up state until power is removed. The second state where the circuit bounces between power supply limits is named oscillatory. Remember, the loop gain, Aβ, is the sole factor that determines stability for a circuit or system. Inputs are grounded or disconnected when the loop gain is calculated, so they have no effect on stability. The loop gain criteria is analyzed in depth later.

Equations 1 and 2 are combined and rearranged to yield equation 7 which gives an indication of system or circuit error.

$$E = \frac{V_{IN}}{1 + A\beta} \tag{7}$$

First, notice that the error is proportional to the input signal. This is the expected result because a bigger input signal results in a bigger output signal, and bigger output signals require more drive voltage. Second, the loop gain is inversely proportional to the error. As the loop gain increases the error decreases, thus large loop gains are attractive for minimizing errors. Large loop gains also decrease stability, thus there is always a tradeoff between error and stability.

A noninverting op amp is shown in Figure 3.

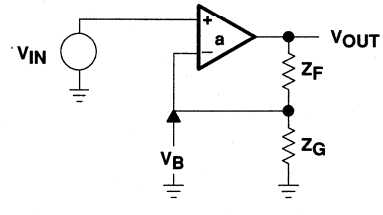

Figure 3. Noninverting Op Amp

Equation 8 is the amplifier transfer equation:

$$V_{OUT} = a\left(V_{IN} - V_B\right) \tag{8}$$

Equation 9 is the output equation:

$$V_B = \frac{V_{OUT} Z_G}{Z_F + Z_G} \text{ for } I_B = 0 \tag{9}$$

Combining equations 8 and 9 yields equation 10:

$$V_{OUT} = aV_{IN} - \frac{aZ_G\ V_{OUT}}{Z_G + Z_F} \tag{10}$$

Rearranging terms in equation 10 yields equation 11, which describes the transfer function of the circuit:

$$\frac{V_{OUT}}{V_{IN}} = \frac{a}{1 + \frac{aZ_G}{Z_G + Z_F}} \tag{11}$$

Equation 5 is repeated as equation 12 to make a term by term comparison of the equations easy.

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \tag{12}$$

By virtue of the comparison we get equation 13, which is the loop-gain equation for the noninverting op amp. The loop-gain equation determines the stability of the circuit.

$$A\beta = \frac{aZ_G}{Z_G + Z_F} \tag{13}$$

Equation 13 could have been derived by breaking the op amp feedback loop, say at point B, and calculating the loop gain. This procedure is used later to derive the inverting loop gain. Also, by comparison the direct gain A is seen to be A = *a*, or the direct gain for the noninverting op amp is the same as the op amp gain. The inverting op amp circuit is shown in Figure 4.

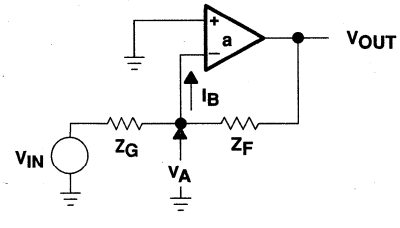

Figure 4. Inverting Op Amp

The transfer equation is given in equation 14:

$$V_{OUT} = -aV_A \tag{14}$$

The node voltage is described by equation 15, and equation 16 is obtained by combining equations 14 and 15.

$$V_A = \frac{V_{IN}\, Z_F}{Z_G + Z_F} + \frac{V_{OUT}\, Z_G}{Z_G + Z_F} \quad \text{for } I_B = 0 \tag{15}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{\dfrac{-aZ_F}{Z_G + Z_F}}{1 + \dfrac{aZ_G}{Z_G + Z_F}} \tag{16}$$

Equation 16 is the transfer function of the inverting op amp. The direct gain garnered by the comparison method is $aZ_G/(Z_G + Z_F)$. The inverting op amp with the feedback loop broken is shown in Figure 5, and this circuit is used to calculate the loop-gain given in equation 17.

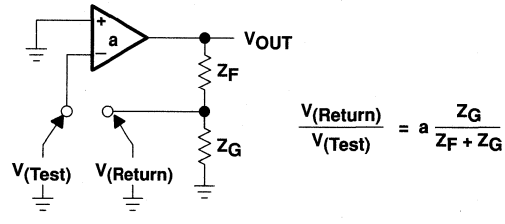

Figure 5. Inverting Op Amp: Feedback Loop Broken for Loop Gain Calculation

$$\frac{V_{RETURN}}{V_{TEST}} = \frac{aZ_G}{V_G + V_F} = A\beta \tag{17}$$

Several things must be mentioned at this point in the analysis. First, the transfer functions for the noninverting and inverting equations, 11 and 16, are different. For a common set of Z_G and Z_F values, the magnitude and polarity of the gains are different. Second, the loop gain of both circuits, as given by equations 13 and 17, is identical. Thus, the stability performance of both circuits is identical although their transfer equations are different. This makes the important point that *stability is not dependent on the circuit inputs.* Third, the A gain block shown in Figure 1 is different for each op amp circuit. By comparison of equations 5, 11, and 16 we see that $A_{NON-INV} = a$ and $A_{INV} = aZ_F \div (Z_G + Z_F)$. Equation 7 shows that the error is inversely proportional to the loop gain; thus, the accuracy of identical closed loop gain inverting and noninverting op amp circuits is different.

Equation 17 is used to compensate all op amp circuits. First, we determine what compensation method to use. Second, we derive the compensation equations. Third, we analyze the closed loop transfer function to determine how it is modified by the compensation. The effect of the compensation on the closed loop transfer function often determines which compensation technique will be used.

Internal Compensation

Op amps are internally compensated to save external components and to enable their use by less knowledgeable people. It takes some measure of analog knowledge to compensate an analog circuit. Internally compensated op amps normally are stable when they are used in accordance with the applications instructions. Internally compensated op amps are not unconditionally stable. They are multiple pole systems, but they are internally compensated such that they appear as a single pole system over much of the frequency range. The cost of internal compensation is that it severely decreases the closed loop bandwidth of the op amp.

Internal compensation is accomplished in several ways, but the most common method is to connect a capacitor across the collector–base junction of a voltage gain transistor (see Figure 6). The Miller effect multiplies the capacitor value by an amount approximately equal to the stage gain, thus the Miller effect uses small value capacitors for compensation. Figure 7 shows the gain/phase diagram for an older op amp (TL03X). When the gain crosses the 0 dB axis (gain equal to one) the phase shift is about 100°, thus the op amp must be modeled as a second order system because the phase shift is more than 90°.

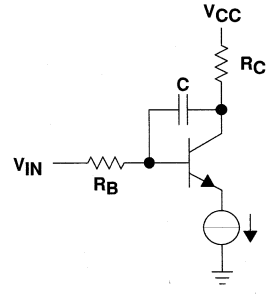

Figure 6. Miller Effect Compensation

This yields a phase margin of $\phi = 180° - 100° = 80°$, thus the circuit should be very stable (Reference 1 explains feedback analysis tools). Referring to Figure 8, the damping ratio is one and the expected overshoot is zero. Figure 7 shows approximately 10% overshoot which is unexpected, but inspecting Figure 7 further reveals that the loading capacitance for the two plots is different. The pulse response is loaded with 100 pF rather than 25 pF shown for the gain/phase plot, and this extra loading capacitance accounts for the loss of phase margin.

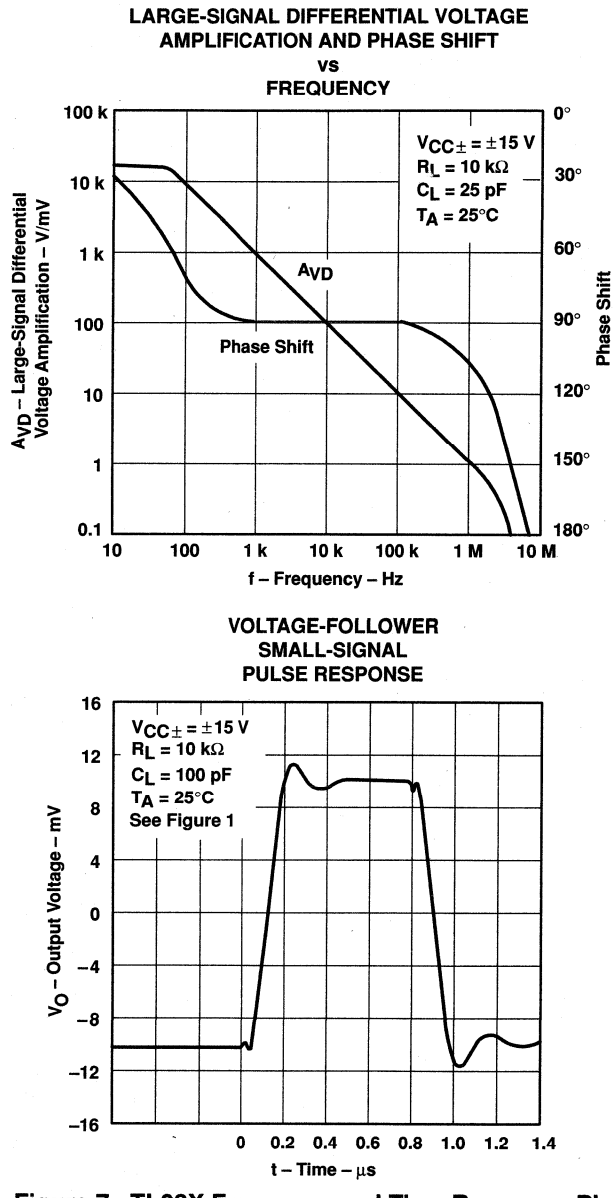

Figure 7. TL03X Frequency and Time Response Plots

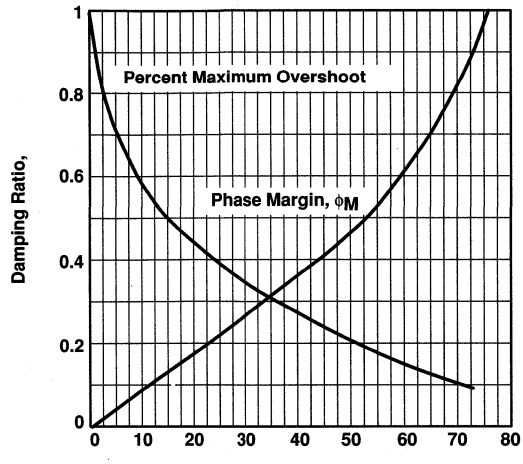

Figure 8. Phase Margin and Percent Overshoot Versus Damping Ratio

Why does the loading capacitance make the op amp unstable? Look closely at the gain/phase response between 1 MHz and 9 MHz, and observe that the gain curve changes slope drastically while the rate of phase change approaches 120°/decade. The radical gain/phase slope change proves that several poles are located in this area. The loading capacitance works with the op amp output impedance to form another pole, and the new pole reacts with the internal op amp poles. As the loading capacitor value is increased, its pole migrates down in frequency, causing more phase shift at the 0 dB crossover frequency. The proof of this is given in the TL03X data sheet where plots of ringing and oscillation versus loading capacitance are shown.

Figure 9 shows similar plots for the TL07X which is the newer family of op amps. Notice that the phase shift is 90° when the gain crosses the 0 dB axis. This yields a phase margin of 90°, which is considered unconditionally stable. The slope of the phase curve changes to 180°/decade about one decade from the 0 dB crossover point. The radical slope change causes suspicion about the 90° phase margin, furthermore the gain curve must be changing radically when the phase is changing radically. The gain/phase plot may not be totally false, but it sure is overly optimistic.

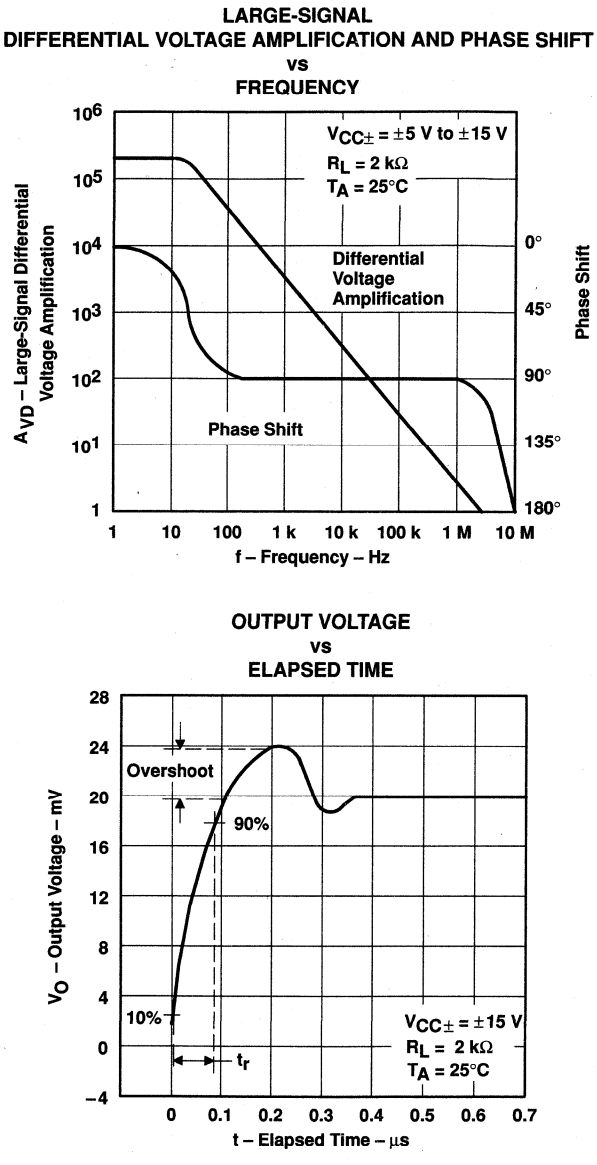

Figure 9. TL07X Frequency and Time Response Plots

The TL07X pulse response plot shows approximately 20% overshoot. There is no loading capacitance indicated on the plot to account for an unconditionally stable op amp exhibiting this large an overshoot. Something is wrong here: the analysis is wrong, the plots are wrong, or the parameters are wrong. Figure 10 shows the plots for the TL08X family of op amps which are sisters to the TL07X family. The gain/phase curve and pulse response is virtually identical, but the

pulse response lists a 100 pF loading capacitor. This little exercise illustrates three valuable points: first, if the data seems wrong it probably is wrong, second, even the factory people make mistakes, and third, the loading capacitor makes op amps ring, overshoot, or oscillate.

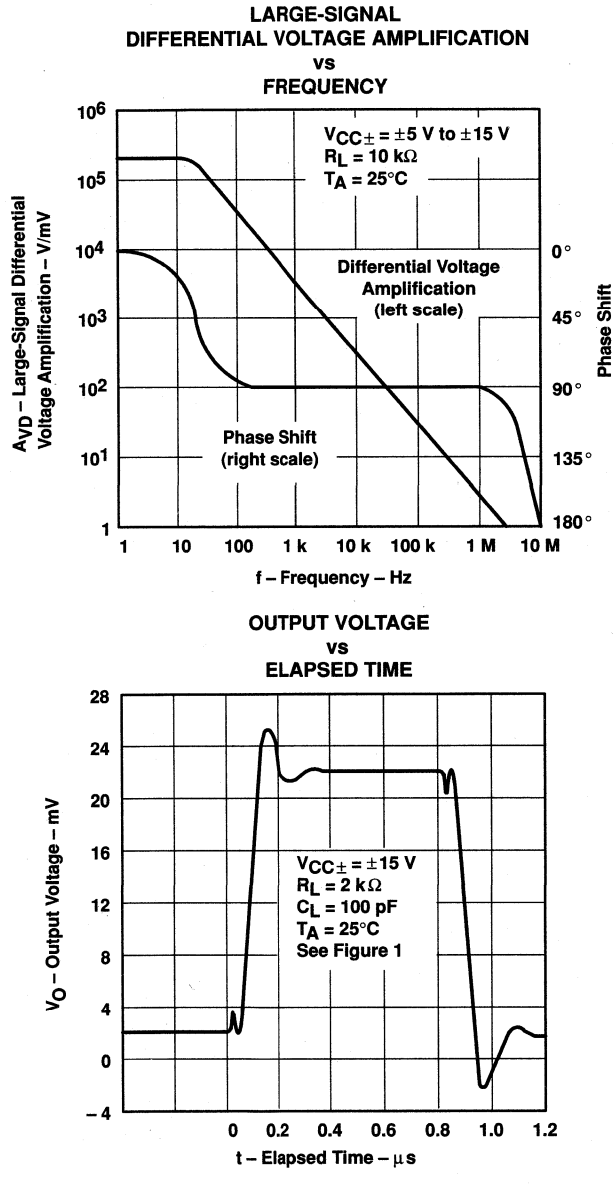

Figure 10. TL08X Frequency and Time Response Plots

The frequency and time-response plots for the TLV277X family of op amps is

shown in Figures 11 and 12. First, notice that the information is more sophisticated because the phase response is given in degrees of phase margin; second, both gain/phase plots are done with substantial loading capacitors (600 pF), so they have some practical value; and third, the phase margin is a function of power supply voltage.

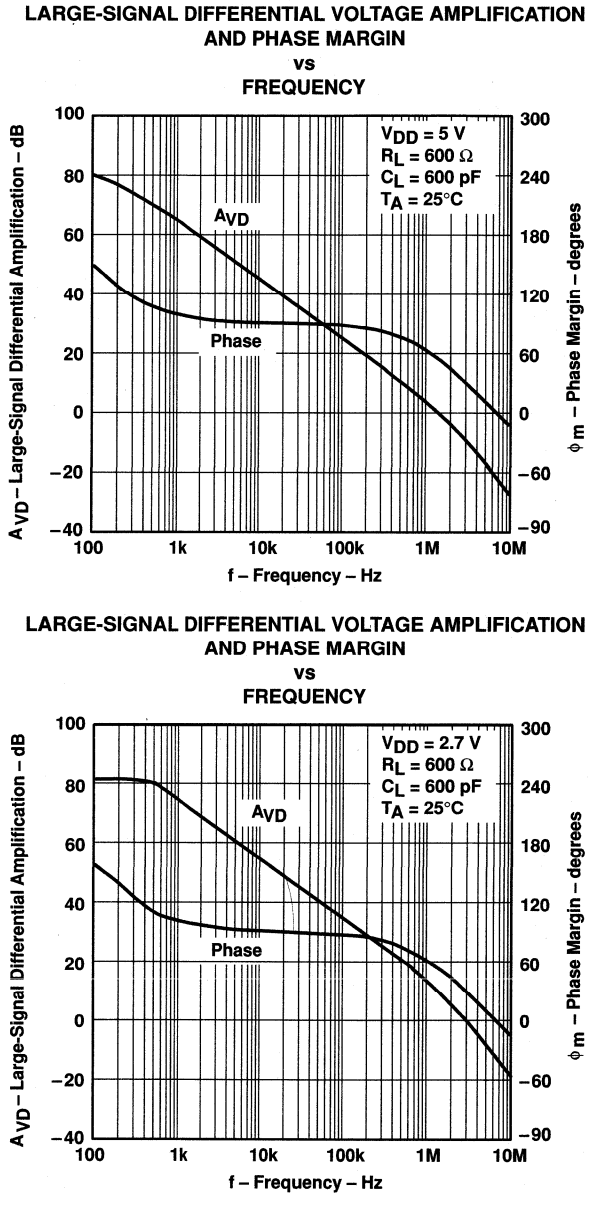

Figure 11. TLV277X Frequency Response Plots

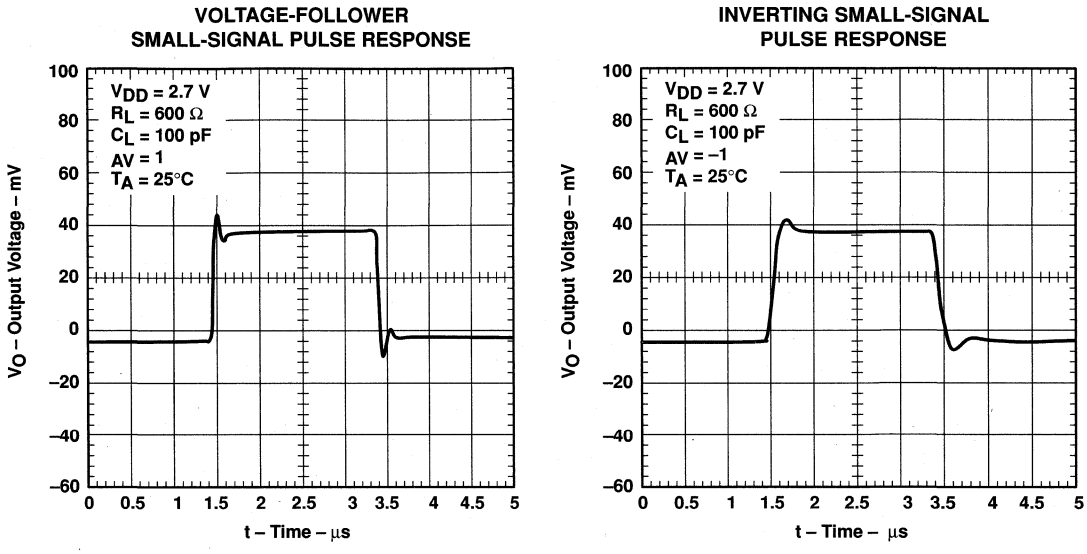

Figure 12. TLV227X Time Response Plots

At V_{CC} = 5 V, the phase margin at the 0-dB crossover point is 60°, while it is 30° at V_{CC} = 2.7 V. This translates into an expected overshoot of 18% at V_{CC} = 5 V, and 28% at V_{CC} = 2.7 V. Unfortunately the time response plots are done with 100-pF loading capacitance, hence we can not check our figures very well. The V_{CC} = 2.7 V overshoot is approximately 2%, and it is almost impossible to figure out what the overshoot would have been with a 600 pF loading capacitor. The small-signal pulse response is done with mV-signals, and that is a more realistic measurement than using the full-signal swing.

Internally compensated op amps are very desirable because they are easy to use, and they do not require external compensation components. Their drawback is that the bandwidth is limited by the internal compensation scheme. The error in an op amp circuit is determined by the op amp open-loop gain. In a noninverting buffer configuration, the TL277X is limited to 1% error at 50 kHz (V_{CC} = 2.7 V) because the op amp gain is 40 dB at that point. Circuit designers can play tricks such as bypassing the op amp with a capacitor to emphasize the high-frequency gain, but the error is still 1%. Keep equation 7 in mind because it defines the error. If the TLV277X were not internally compensated, it could be externally compensated for a lower error at 50 kHz because the gain would be much higher.

External Compensation, Stability, and Performance

This section is approached on a compensation type basis. Nobody compensates an op amp because it is there; they have a reason to compensate the op amp, and that reason is usually stability. They want the op amp to perform a function in a circuit where it is potentially unstable. Internally and noninternally compensated op amps are compensated externally because certain circuit configurations do cause oscillations. Several potentially unstable circuit configurations are analyzed in this section, and the reader can extend the external compensation techniques as required.

Other reasons for externally compensating op amps are noise reduction, absolutely flat amplitude response, and obtaining the highest bandwidth possible from an op amp. An op amp generates noise, and noise is generated by the system. The noise contains many frequency components, and when a high pass filter is incorporated in the signal path, it reduces high frequency noise. Compensation can be employed to roll off the op amp's high frequency, closed loop response, thus causing the op amp to act as a noise filter. Internally compensated op amps are modeled with a second order equation, and this means that the output voltage can overshoot in response to a step input. When this overshoot (or peaking) is undesirable, external compensation can increase the phase margin to 90° where there is no peaking. An uncompensated op amp has the highest bandwidth possible. External compensation is required to stabilize uncompensated op amps, but the compensation can be tailored to the specific circuit, thus yielding the highest possible bandwidth consistent with the pulse response requirements.

Dominant-Pole Compensation

We saw that capacitive loading caused potential instabilities, thus an op amp loaded with an output capacitor is a circuit configuration that must be analyzed. This circuit is called dominant pole compensation because if the pole formed by the op amp output impedance and the loading capacitor is located close to the zero frequency axis, it becomes dominant. The op amp circuit is shown in Figure 13, and the open loop circuit used to calculate the loop gain (Aβ) is shown in Figure 14.

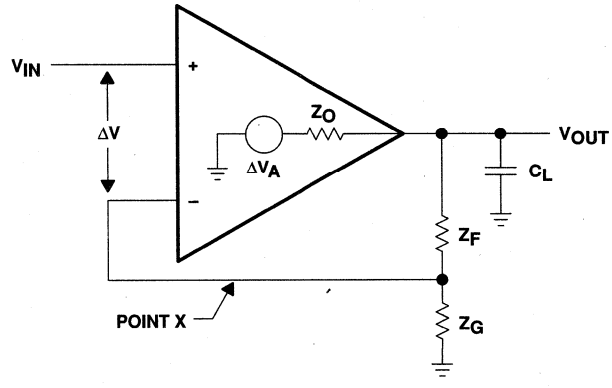

Figure 13. Capacitively-Loaded Op Amp

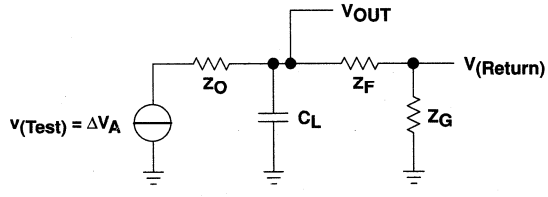

Figure 14. Capacitively-Loaded Op Amp With Loop Broken for Loop Gain (Aβ) Calculation

The analysis starts by looking into the capacitor and taking the Thevenin equivalent circuit.

$$V_{TH} = \frac{\Delta Va}{Z_O C_L s + 1} \tag{18}$$

$$Z_{TH} = \frac{Z_O}{Z_O C_L s + 1} \tag{19}$$

Then the output equation is written:

$$V_{RETURN} = \frac{V_{TH} Z_G}{Z_G + Z_F + Z_{TH}} = \frac{\Delta Va}{Z_O C_L s + 1} \left[\frac{Z_G}{Z_F + Z_G + \frac{Z_O}{Z_o C_L s + 1}} \right] \tag{20}$$

Rearranging terms yields equation 21:

$$\frac{V_{RETURN}}{V_{TEST}} = A\beta = \frac{\dfrac{aZ_F}{Z_F + Z_G + Z_O}}{\dfrac{(Z_F + Z_G)Z_O C_L s}{Z_F + Z_G + Z_O} + 1} \tag{21}$$

When the assumption is made that $(Z_F + Z_G) >> Z_O$, equation 21 reduces to equation 22:

$$A\beta = \frac{aZ_G}{Z_F + Z_G}\left(\frac{1}{Z_O C_L s + 1}\right) \tag{22}$$

Equation 23 models the op amp as a second-order system. Hence, substituting the second-order model for *a* in equation 22 yields equation 24 which is the stability equation for the dominant-pole compensation circuit:

$$a = \frac{K}{(s + \tau_1)(s + \tau_2)} \tag{23}$$

$$A\beta = \frac{K}{(s + \tau_1)(s + \tau_2)} \frac{Z_G}{Z_F + Z_G} \frac{1}{Z_O C_L s + 1} \tag{24}$$

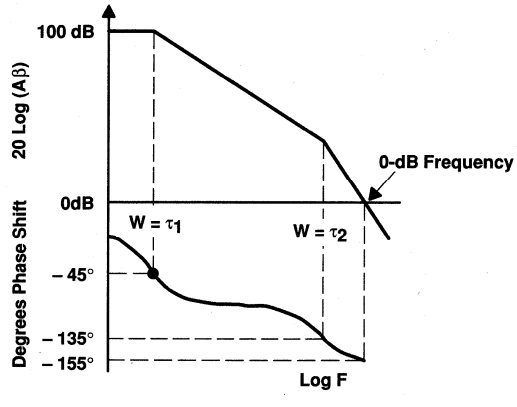

Figure 15. Possible Bode Plot of the Op Amp Described in Equation 23

Several conclusions can be drawn from equation 24 depending on the location of the poles. If the Bode plot of equation 23, the op amp transfer function, looks like that shown in Figure 15, it only has 25° phase margin, and there is approximately 48% overshoot. When the pole introduced by Z_O and C_L moves towards the zero frequency axis it comes close to the τ_2 pole, and it adds phase shift to the system. Increased phase shift increases peaking and decreases stability. In the real world, many loads, especially cables, are capacitive, and an op amp like the one pictured in Figure 15 would ring while driving a capacitive load. The load capacitance causes peaking and instability in internally compensated op amps when the op amps do not have enough phase margin to allow for the phase shift introduced by the load.

Prior to compensation, the Bode plot of an uncompensated op amp looks like that shown in Figure 16. Notice that the break points are located close together thus accumulating about 180° of phase shift before the 0 dB crossover point; the op amp is not usable and probably unstable. Dominant pole compensation is often used to stabilize these op amps. If a dominant pole, in this case ω_D, is properly placed it rolls off the gain so that τ_1 introduces 45° phase at the 0 dB crossover point. After the dominant pole is introduced the op amp is stable with 45° phase margin, but the op amp gain is drastically reduced for frequencies above ω_D. This procedure works well for internally compensated op amps, but is seldom used for externally compensated op amps because inexpensive discrete capacitors are readily available.

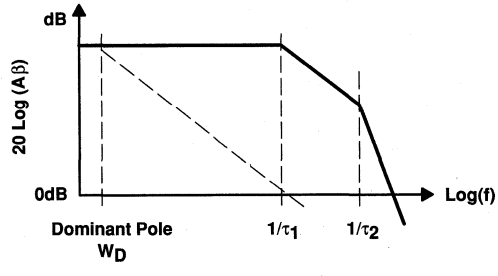

Figure 16. Dominant-Pole Compensation Plot

Assuming that $Z_O << Z_F$, the closed-loop transfer function, is easy to calculate because C_L is enclosed in the feedback loop. The ideal closed-loop transfer equation is the same as equation 11 for the noninverting op amp, and is repeated below as equation 25:

$$\frac{V_{OUT}}{V_{IN}} = \frac{a}{1 + \frac{aZ_G}{Z_G + Z_F}} \tag{25}$$

When $a \Rightarrow \infty$ equation 25 reduces to equation 26:

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_F + Z_G}{Z_G} \tag{26}$$

As long as the op amp has enough compliance and current to drive the capacitive load, and Z_O is small, the circuit functions as though the capacitor wasn't there. When the capacitor becomes large enough, its pole interacts with the op amp pole causing instability. When the capacitor is huge, it completely kills the op amp's bandwidth, thus lowering the noise while retaining the high low frequency gain.

Gain Compensation

When the closed loop gain of an op amp circuit is related to the loop gain, as it is in voltage feedback op amps, the gain can be used to stabilize the circuit. This type of compensation can not be used in current feedback op amps because the mathematical relationship between the loop gain and ideal closed loop gain does not exist. The loop gain equation is repeated as equation 27. Notice that the closed loop gain parameters Z_G and Z_F are contained in equation 27, hence the stability can be controlled by manipulating the closed loop gain parameters.

$$A\beta = \frac{aZ_G}{Z_G + Z_F} \tag{27}$$

The original loop gain curve for a closed loop gain of one is shown in Figure 17, and it is or comes very close to being unstable. If the closed loop noninverting gain is changed to 9, then K changes from K/2 to K/10. The loop gain intercept on the Bode plot (see Figure 17) moves down 14 dB, and the circuit is stabilized.

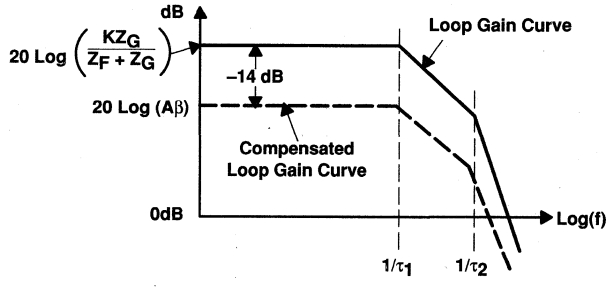

Figure 17. Gain Compensation

Gain compensation works for inverting or noninverting op amp circuits because the loop gain equation contains the closed loop gain parameters in both cases. When the closed loop gain is increased, the accuracy and the bandwidth decrease. As long as the application can stand the higher gain, gain compensation is the best type of compensation to use. Uncompensated versions of internally compensated op amps are offered for sale as internally compensated op amps with minimum gain restrictions. As long as the circuit gain exceeds the specified gain, this is economical and a safe mode of operation.

Lead Compensation

Sometimes lead compensation is forced on the circuit designer because of the parasitic capacitance associated with packaging and wiring op amps. Figure 18 shows the circuit for lead compensation; notice the capacitor in parallel with R_F. That capacitor is often made by parasitic wiring and the ground plane, and high frequency circuit designers go to great lengths to minimize or eliminate it. What is good in one sense is bad in another, because adding the parallel capacitor is a good way to stabilize the op amp and reduce noise. Let us analyze the stability first, and then we will analyze the closed loop performance.

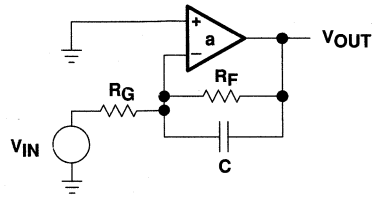

Figure 18. Lead-Compensation Circuit

The loop equation for the lead-compensation circuit is given by equation 28:

$$A\beta = \left(\frac{R_G}{R_G + R_F}\right)\left(\frac{R_F Cs + 1}{R_G \| R_F Cs + 1}\right)\left[\frac{K}{(s+\tau_1)(s+\tau_2)}\right] \tag{28}$$

The compensation capacitor introduces a pole and zero into the loop equation. The zero always occurs before the pole because $R_F > R_F || R_G$. When the zero is properly placed it cancels out the τ_2 pole along with its associated phase shift. The original transfer function is shown in Figure 19 drawn in solid lines. When the $R_F C$ zero is placed at $\omega = 1/\tau_2$, it cancels out the τ_2 pole causing the bode plot to continue on a slope of –20 dB/decade. When the frequency gets to $\omega = 1/(R_F||RG)C$, this pole changes the slope to –40 dB/decade. Properly placed, the capacitor aids stability, but what does it do to the closed loop transfer function? The equation for the inverting op amp closed loop gain is repeated below.

$$\frac{V_{OUT}}{V_{IN}} = \frac{\dfrac{-aZ_F}{Z_G + Z_F}}{1 + \dfrac{aZ_G}{Z_G + Z_F}} \tag{29}$$

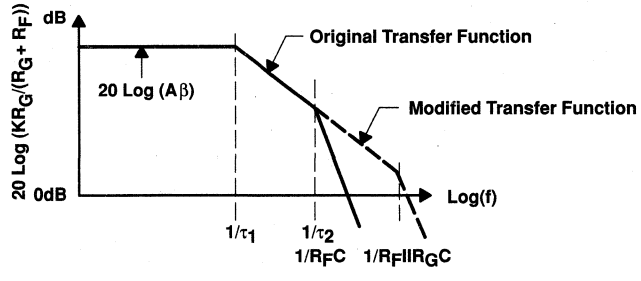

Figure 19. Lead-Compensation Bode Plot

When *a* approaches infinity, equation 29 reduces to equation 30:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{Z_F}{Z_{IN}} \tag{30}$$

Substituting $R_F \| C$ for Z_F and R_G for Z_G in equation 30 yields equation 31, which is the ideal closed-loop gain equation for the lead compensation circuit:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_G}\left(\frac{1}{R_F Cs + 1}\right) \tag{31}$$

The forward gain for the inverting amplifier is given by equation 32. Compare equation 29 with equation 5 to determine A.

$$A = \frac{aZ_F}{Z_G + A_F}\left(\frac{R_F}{R_G + R_F}\right)\left(\frac{1}{R_F \| R_G Cs + 1}\right) \tag{32}$$

The op amp gain (a) the forward gain (A) and the ideal closed loop gain are plotted in Figure 20. The op amp gain is plotted for reference only. The forward gain for the inverting op amp is not the op amp gain. Notice that the forward gain is reduced by the factor $R_F/(R_G + R_F)$, and it contains a high frequency pole. The ideal closed loop gain follows the ideal curve until the $1/R_FC$ breakpoint (same location as $1/\tau_2$ breakpoint), and then it slopes down at –20 dB/decade. Lead compensation sacrifices the bandwidth between the $1/R_FC$ breakpoint and the forward gain curve. The location of the $1/R_FC$ pole determines the bandwidth sacrifice, and it can be much greater than shown here. The pole caused by R_F, R_G, and C does not appear until the op amp's gain has crossed the 0 dB axis, thus it does not effect the ideal closed loop transfer function.

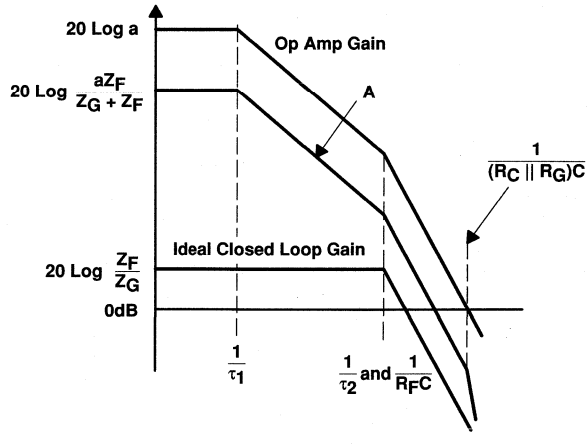

Figure 20. Inverting Op Amp With Lead Compensation

The forward gain for the noninverting op amp is *a*; compare equation 11 to equation 5. The ideal closed-loop gain is given by equation 33:

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_F + Z_G}{Z_G} = \left(\frac{R_F + R_G}{R_G}\right)\left(\frac{R_F \| R_G Cs + 1}{R_F Cs + 1}\right) \tag{33}$$

The plot of the noninverting op amp with lead compensation is shown in Figure 21. There is only one plot for both the op amp gain (a) and the forward gain (A), because they are identical in the noninverting circuit configuration. The ideal starts out as a flat line, but it slopes down because its closed loop gain contains a pole and a zero. The pole always occurs closer to the low frequency axis because $R_F > R_F||R_G$. The zero flattens the ideal closed loop gain curve, but it never does any good because it can not fall on the pole. The pole causes a loss in the closed loop bandwidth by the amount separating the closed loop and forward gain curves.

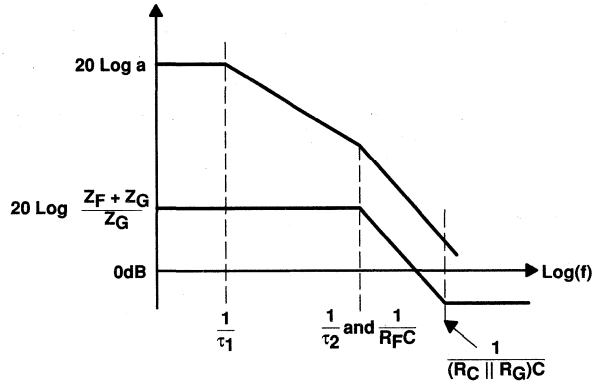

Figure 21. Noninverting Op Amp With Lead Compensation

Although the forward gain is different in the inverting and noninverting circuits, the closed loop transfer functions take very similar shapes. This becomes truer as the closed loop gain increases because the noninverting forward gain approaches the op amp gain. This relationship can not be relied on in every situation, and each circuit must be checked to determine the closed loop effects of the compensation scheme.

Compensated Attenuator Applied to Op Amp

Stray capacitance on op amp inputs is a problem that circuit designers are always trying to get away from because it decreases closed loop frequency response or causes peaking. The circuit shown in Figure 22 has some stray capacitance (C_G,) connected from the inverting input to ground. Equation 34 is the loop gain equation for the circuit with input capacitance.

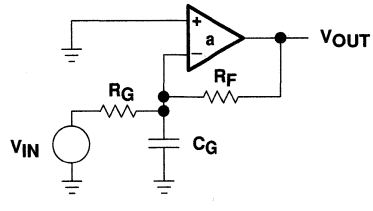

Figure 22. Op Amp With Stray Capacitance on the Inverting Input

$$A\beta = \left(\frac{R_G}{R_G + R_F}\right)\left(\frac{1}{R_G \| R_F Cs + 1}\right)\left[\frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)}\right] \quad (34)$$

Op amps having high input and feedback resistors are subject to instability caused by stray capacitance on the inverting input. Referring to equation 34, when the $1/(R_F||R_G C_G)$ pole moves close to τ_2 the stage is set for instability. Reasonable component values for a CMOS op amp are R_F = 1 MΩ, R_G = 1 MΩ, and
C_G = 10 pF. The resulting pole occurs at 318 kHz, and this frequency is lower than the breakpoint of τ_2 for many op amps. There is 90° phase shift resulting from τ_1, the $1/(R_F||R_G C)$ pole adds 45° phase shift at 318 kHz, and τ_2 starts adds another 45° phase shift at about 600 kHz. This circuit is unstable because of the stray input capacitance. The circuit is compensated by adding a feedback capacitor as shown in Figure 23.

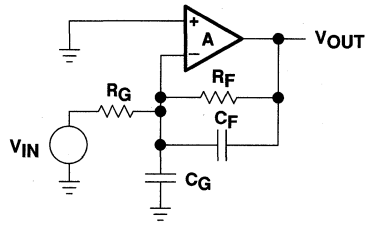

Figure 23. Compensated Attenuator Circuit

The loop gain with C_F added is given by equation 35:

$$A\beta = \left[\frac{\frac{R_G}{R_G C_G s+1}}{\frac{R_G}{R_G C_G s+1} + \frac{R_F}{R_F C_F s+1}}\right]\left[\frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)}\right] \quad (35)$$

If $R_G C_G = R_F C_F$ equation 35 reduces to equation 36:

$$A\beta = \left(\frac{R_G}{R_G + R_F}\right)\left[\frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)}\right] \quad (36)$$

The compensated attenuator Bode plot is shown in Figure 24. Adding the correct $1/R_F C_F$ breakpoint cancels out the $1/R_G C_G$ breakpoint, the loop gain is independent of the capacitors. Now is the time to take advantage of the stray capacitance. C_F can be formed by running a wide copper strip from the output of the op amp over the ground plane under R_F; do not connect the other end of this copper strip. The circuit is tuned by removing some copper (a razor works well) until all peaking is eliminated. Then measure the copper, and have an identical trace put on the printed-circuit board.

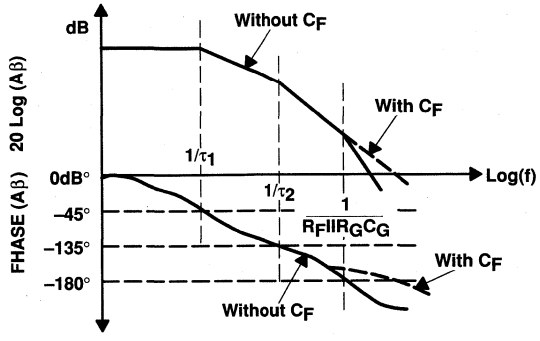

Figure 24. Compensated Attenuator Bode Plot

The inverting and noninverting closed loop gain equations are a function of frequency. Equation 37 is the closed loop gain equation for the inverting op amp. When $R_F C_F = R_G C_G$ equation 37 reduces to equation 38 which is independent of the breakpoint. This also happens to the noninverting op amp circuit. This is one of the few occasions when the compensation does not affect the closed loop gain frequency response.

$$\frac{V_{OUT}}{V_{IN}} = - \frac{\frac{R_F}{R_F C_F s + 1}}{\frac{R_G}{R_G C_G s + 1}} \tag{37}$$

When $R_F C_F = R_G C_G$

$$\frac{V_{OUT}}{V_{IN}} = - \left(\frac{R_F}{R_G} \right) \tag{38}$$

Lead-Lag Compensation

Lead-lag compensation stabilizes the circuit without sacrificing the closed-loop gain performance. This type of compensation leads to excellent high-frequency performance. The circuit schematic is shown in Figure 25, and the loop gain is given by equation 39.

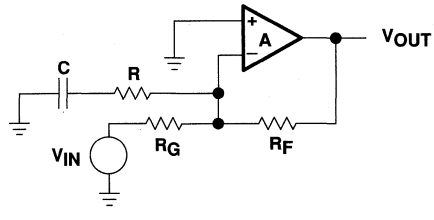

Figure 25. Lead-Lag Compensated Op Amp

$$A\beta = \frac{K}{(\tau_1 s + 1)(\tau_2 s + 1)} \frac{R_G}{R_G + R_F} \frac{RCs + 1}{\frac{(RR_G + RR_F + R_G R_F)}{(R_G + R_F)} Cs + 1} \tag{39}$$

Referring to Figure 26, a pole is introduced at $\omega = 1/RC$, and this pole reduces the gain 3 dB at the breakpoint. When the zero occurs prior to the first op amp pole it cancels out the phase shift caused by the $\omega = 1/RC$ pole. The phase shift is completely canceled before the second op amp pole occurs, and the circuit reacts as if the pole was never introduced. Nevertheless, $A\beta$ is reduced by the 3 dB or more, so the loop gain crosses the 0 dB axis at a lower frequency. The beauty of lead lag compensation is that the closed loop ideal gain is not affected as is shown below. The Thevenin equivalent of the input circuit is calculated in equation 40, the circuit gain in terms of Thevenin equivalents is calculated in equation 41, and the ideal closed loop gain is calculated in equation 42.

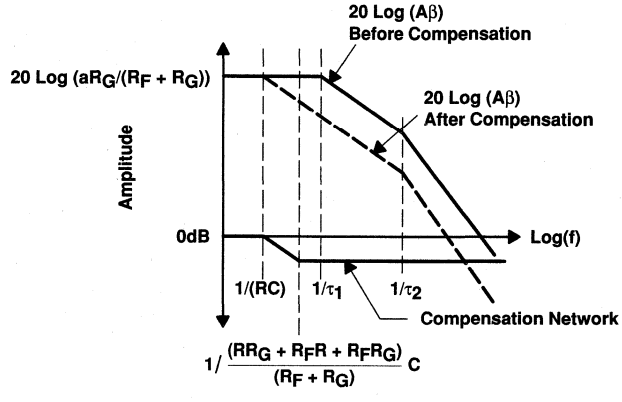

Figure 26. Bode Plot of Lead-Lag Compensated Op Amp

$$V_{TH} = V_{IN}\frac{R + \frac{1}{Cs}}{R + R_G + \frac{1}{Cs}} \qquad R_{TH} = \frac{R_G\left(R + \frac{1}{Cs}\right)}{R + R_G + \frac{1}{Cs}} \tag{40}$$

$$V_{OUT} = -V_{TH}\frac{R_F}{R_{TH}} \tag{41}$$

$$-\frac{V_{OUT}}{V_{IN}} = \frac{R + \frac{1}{Cs}}{R + R_G + \frac{1}{Cs}} \frac{R_F}{\frac{R_G\left(R+\frac{1}{Cs}\right)}{R+R_G+\frac{1}{Cs}}} = \frac{R_F}{R_G} \tag{42}$$

Equation 42 is intuitively obvious because the RC network is placed across a virtual ground. As long as the loop gain, $A\beta$, is large the feedback will null out the closed loop effect of RC, and the circuit will function as if it weren't there. The closed loop log plot of the lead-lag compensated op amp is given in Figure 27. Notice that the pole and zero resulting from the compensation occur and are gone before the first amplifier poles come on the scene. This prevents interaction, but it is not required for stability.

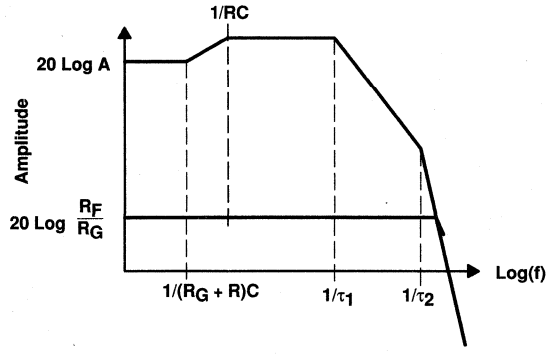

Figure 27. Closed-Loop Plot of Lead-Lag Compensated Op Amp

Comparison of Compensation Schemes

Internally compensated op amps can, and often do, oscillate under some circuit conditions. Internally compensated op amps need an external pole to get the oscillation or ringing started, and circuit stray capacitances often supply the phase shift required for instability. Loads, such as cables, often cause internally compensated op amps to ring severely.

Dominant pole compensation is often used in IC design because it is easy to implement. It rolls off the closed loop gain early; thus, it is seldom used as an external form of compensation unless filtering is required. Load capacitance, depending on its pole location, usually causes the op amp to ring. Large load capacitance can stabilize the op amp because it acts as dominant pole compensation.

The simplest form of compensation is gain compensation. High closed loop gains are reflected in lower loop gains, and in turn, lower loop gains increase stability. If an op amp circuit can be stabilized by increasing the closed loop gain, do it.

Stray capacitance across the feedback resistor tends to stabilize the op amp because it is a form of lead compensation. This compensation scheme is useful for limiting the circuit bandwidth, but it decreases the closed loop gain.

Stray capacitance on the inverting input works with the parallel combination of the feedback and gain setting resistors to form a pole in the Bode plot, and this pole decreases the circuit's stability. This effect is normally observed in high impedance circuits built with CMOS op amps. Adding a feedback capacitor forms a compensated attenuator scheme which cancels out the input pole. The cancellation occurs when the input and feedback RC time constants are equal. Under the conditions of equal time constants, the op amp functions as though the stray input capacitance was not there. An excellent method of implementing a compensated attenuator is to build a stray feedback capacitor using the ground plane and a trace off the output node.

Lead-lag compensation stabilizes the op amp, and it yields the best closed-loop frequency performance. Contrary to some published opinions, no compensation scheme will increase the bandwidth beyond that of the op amp. Lead-lag compensation just gives the best bandwidth for the compensation.

Conclusions

The stability criteria often is not oscillation, rather it is circuit performance as exhibited by peaking and ringing.

The circuit bandwidth can often be increased by connecting an external capacitor in parallel with the op amp. Some op amps have hooks which enable a parallel capacitor to be connected in parallel with a portion of the input stages. This increases bandwidth because it shunts high frequencies past the low bandwidth g_m stages, but this method of compensation depends on the op amp type and manufacturer.

The compensation techniques given here are adequate for the majority of applications. When the new and challenging application presents itself, use the procedure outline here to invent your own compensation technique.

Reference

Mancini, Ron, *Feedback Amplifier Analysis Tools*, SLVA058, Texas Instruments, 1999.

Understanding Basic Analog – Ideal Op Amps Application Report

By Ron Mancini

Literature Number: SLAA068
July 1999

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Contents

List of Figures

Understanding Basic Analog – Ideal Op Amps

By Ron Mancini

ABSTRACT

This application report develops the equations for the ideal operational amplifier (op amp). It assumes that salient parameters are perfect. Several examples of op amp circuits are described.

Introduction

The name *Ideal Op Amp* is applied to this and similar analysis because the salient parameters of the op amp are assumed to be perfect. There is no such thing as an ideal op amp, but present day op amps come so close to ideal that *Ideal Op Amp* analysis becomes close to actual analysis. Op amps depart from the ideal in two ways. First, dc parameters, such as input offset voltage, are large enough to cause departure from the ideal. The ideal assumes that input offset voltage is zero. Second, ac parameters, such as gain, are a function of frequency, so they go from large values at dc to small values at high frequencies. Both error sources are treated in later *Understanding* .... application notes published in this series.

This assumption simplifies the analysis, thus it clears the path for insight. It is so much easier to see the forest when brush and huge trees do not surround you. Although the ideal op amp analysis makes use of perfect parameters, the analysis is often valid because some op amps approach perfection. In addition, when working at low frequencies, several kHz, the ideal op amp analysis produces accurate answers. Voltage feedback op amps are covered in this application note, and current feedback op amps are covered in later application notes.

Several assumptions have to be made before the ideal op amp analysis can proceed. First, assume that the current flow into the input leads of the op amp is zero. This assumption is almost true in FET op amps where input currents can be less than a pA, but this is not always true in bipolar high-speed op amps where tens of μA input currents are found.

Second, the op amp gain is assumed to be infinite, hence it drives the output voltage to any value required to satisfy the input conditions. This assumes that the op amp output voltage can achieve any value. Saturation occurs when the output voltage comes close to a power supply rail, but reality does not negate the assumption, it only bounds it.

Also, implicit in the infinite gain assumption is the need for zero input signal. The gain drives the output voltage until the voltage between the input leads (the error voltage) is zero. This leads to the third assumption that the voltage between the input leads is zero. The implication of zero voltage between the input leads means that if one input is tied to a hard voltage source such as ground, then the other input is at the same potential. The current flow into the input leads is zero, so the input impedance of the op amp is infinite.

Four, the output impedance of the ideal op amp is zero. The ideal op amp can drive any load without an output impedance dropping voltage across it. The output impedance of most op amps is a fraction of an ohm for low current flows, so this assumption is valid in most cases. Five, the frequency response of the ideal op amp is flat; this means that the gain does not vary as frequency increases. By constraining the use of the op amp to the low frequencies, we make the frequency response assumption true.

PARAMETER NAME	PARAMETERS SYMBOL	VALUE
Input current	I_{IN}	0
Input offset voltage	V_{OS}	0
Input impedance	Z_{IN}	∞
Output impedance	Z_{OUT}	0
Gain	a	∞

The Noninverting Op Amp

The noninverting op amp has the input signal connected to its noninverting input, thus its input source sees an infinite impedance. There is no input offset voltage because $V_{OS} = V_E = 0$, hence the negative input must be at the same voltage as the positive input. The op amp output drives current into R_F until the negative input is at the voltage, V_{IN}. This action causes V_{IN} to appear across R_G.

The voltage divider rule is used with V_{OUT} being the input to the voltage divider, and V_{IN} being the output of the voltage divider. Since no current can flow into either op amp lead, use of the voltage divider rule is allowed. Equation 1 is written with the aid of the voltage divider rule, and algebraic manipulation yields equation 2 in the form for a gain parameter.

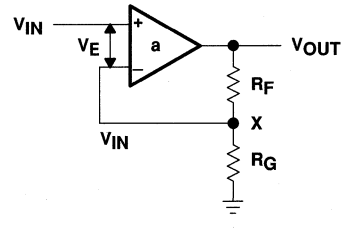


Figure 1. The Noninverting Op Amp

$$V_{IN} = V_{OUT} \frac{R_G}{R_G + R_F} \tag{1}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_G + R_F}{R_G} = 1 + \frac{R_F}{R_G} \tag{2}$$

When R_G becomes very large with respect to R_F, $R_F/R_G \Rightarrow 0$ and equation 2 reduces to equation 3.

$$V_{OUT} = 1 \tag{3}$$

Under these conditions $V_{OUT} = 1$ and the circuit becomes a unity gain buffer. R_G is usually deleted to achieve the same results, and when R_G is deleted, R_F can also be deleted (RF must be shorted when it is deleted). When R_F and R_G are deleted, the op amp output is connected to its inverting input with a wire. Some op amps are self–destructive when R_F is left out of the circuit, so R_F is used in many buffer designs. When R_F is included in a buffer circuit, its function is to protect the inverting input from an over voltage, and it can have almost any value (20k is often used). R_F can never be left out of the circuit in a current feedback amplifier design because R_F determines stability in current feedback amplifiers.

Notice that the gain is only a function of the feedback and gain resistors, so the feedback has accomplished its function of making the gain independent of the op amp parameters. The gain is adjusted by varying the ratio of the resistors. The actual resistor values are determined by the impedance levels that the designer wants to establish. If $R_F = 10K$ and $R_G = 10K$ the gain is two as shown in equation 2, and if $R_F = 100K$ and $R_G = 100K$ the gain is still two. The impedance levels of 10 K or 100 K determine the current drain, the effect stray capacitance will have, and a few other points, but the impedance level does not set the gain.

The Inverting Op Amp

The noninverting input of the inverting op amp circuit is grounded. One assumption we made is that the input error voltage is zero, so the feedback keeps inverting the input of the op amp at a virtual ground (not actual ground but acting like ground). The current flow in the input leads is assumed to be zero, hence the current flowing through R_G equals the current flowing through R_F. Using Kirchoff's law, we write equation 4. Algebraic manipulation gives us equation 5.

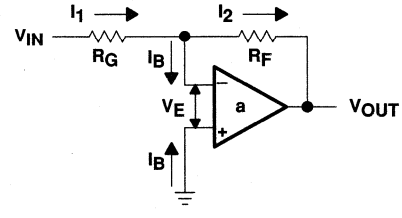


Figure 2. The Inverting Op Amp

$$I_1 = \frac{V_{IN}}{R_G} = -I_2 = -\frac{V_{OUT}}{R_F} \quad (4)$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_G} \quad (5)$$

Notice that the gain is only a function of the feedback and gain resistors, so the feedback has accomplished its function of making the gain independent of the op amp parameters. The actual resistor values are determined by the impedance levels that the designer wants to establish. If R_F=10K and R_G=10K the gain is minus one as shown in equation 5, and if R_F=100K and R_G=100K the gain is still minus one. The impedance levels of 10K or 100K determine the current drain, the effect stray capacitance will have, and a few other points, but the impedance level does not set the gain.

One final note; the output signal is the input signal amplified and inverted. The input impedance is set by R_G because the inverting input lead is held at a virtual ground.

The Adder

An adder circuit can be made by connecting more inputs to the inverting op amp. The opposite end of the resistor connected to the inverting input is held at virtual ground by the feedback; therefore, adding new inputs does not affect the response of the existing inputs.

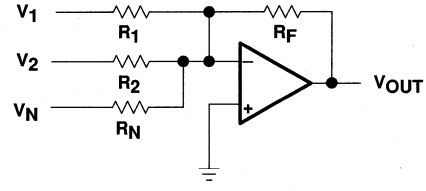


Figure 3. The Adder Circuit

Superposition is used to calculate the output voltages resulting from each input, and the output voltages are added algebraically to obtain the total output voltage. Equation 6 is the output equation when V_1 and V_2 are grounded. Equations 7 and 8 are the other superposition equations, and the final result is given in equation 9.

$$V_{OUTN} = -\frac{R_F}{R_N} V_N \tag{6}$$

$$V_{OUT1} = -\frac{R_F}{R_1} V_1 \tag{7}$$

$$V_{OUT2} = -\frac{R_F}{R_2} V_2 \tag{8}$$

$$V_{OUT} = -\left(\frac{R_F}{R_1} V_1 + \frac{R_F}{R_2} V_2 + \frac{R_F}{R_N} V_N\right) \tag{9}$$

The Differential Amplifier

The differential amplifier circuit amplifies the difference between signals applied to the inputs. Superposition is used to calculate the output voltage resulting from each input voltage, and then the two output voltages are added to arrive at the final output voltage.

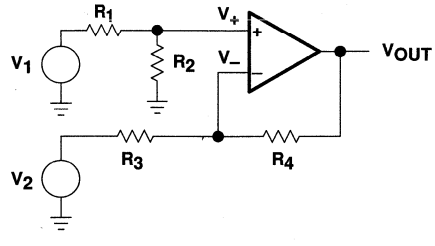


Figure 4. The Differential Amplifier

The output voltage resulting from the input source, V_1, is calculated in equation 10. The voltage divider rule is used to calculate the voltage, V_+, and the noninverting gain equation (equation 2) is used to calculate the noninverting output voltage, V_{OUT1}.

$$V_+ = V_1 \frac{R_2}{R_1 + R_2} \tag{10}$$

$$V_{OUT1} = V_+(G_+) = V_1 \frac{R_2}{R_1 + R_2}\left(\frac{R_3 + R_4}{R_3}\right) \tag{11}$$

The inverting gain (equation 5) is used to calculate the stage gain for V_{OUT2} in equation 12. These inverting and noninverting gains are added in equation 13.

$$V_{OUT2} = V_2\left(-\frac{R_4}{R_3}\right) \tag{12}$$

$$V_{OUT} = V_1 \frac{R_2}{R_1 + R_2}\left(\frac{R_3 + R_4}{R_3}\right) - V_2 \frac{R_4}{R_3} \tag{13}$$

When $R_2 = R_4$ and $R_1 = R_3$, equation 13 reduces to equation 14.

$$V_{OUT} = (V_1 - V_2)\frac{R_4}{R_3} \tag{14}$$

It is now obvious that the differential signal, $(V_1–V_2)$, is multiplied by the stage gain, so the name differential amplifier suits the circuit. Because it only amplifies the differential portion of the input signal, it rejects the common–mode portion of the input signal. A common-mode signal is illustrated in Figure 5. Because the differential amplifier strips off or rejects the common-mode signal, this circuit configuration is often employed to strip dc or injected common-mode noise off a signal.

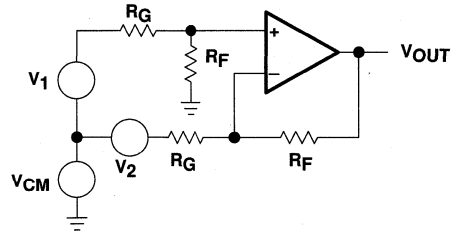


Figure 5. Differential Amplifier With Common-Mode Input Signal

The disadvantage of this circuit is that the two input impedances cannot be matched when it functions as a differential amplifier, thus there are two and three op amp versions of this circuit specially designed for high performance applications requiring matched input impedances.

Complex Feedback Networks

When complex feedback networks are put into the feedback loop, the circuits get harder to analyze because the gain equations can not be used. The usual technique is to write node or loop equations, and to solve these equations. Because a component is grounded, superposition is not of any use, but Thevenin's theorem usually can be used as is shown in the example problem given below.

Sometimes it is desirable to have a low resistance path to ground in the feedback loop. Standard inverting op amps can not do this when the driving circuit sets the input resistor value, and the gain specification sets the feedback resistor value. Inserting a *T* network in the feedback loop yields a degree of freedom that enables both specifications to be met with a low dc resistance path in the feedback loop.

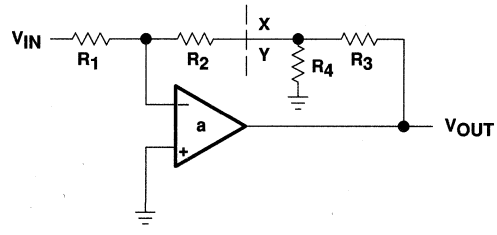


Figure 6. T Network in Feedback Loop

Break the circuit at point X–Y, stand on the terminals looking into R_4, and calculate the Thevenin equivalent voltage as shown in equation 15. The Thevenin equivalent impedance is calculated in equation 16.

$$V_{TH} = V_{OUT} \frac{R_4}{R_3 + R_4} \tag{15}$$

$$R_{TH} = R_3 \parallel R_4 \tag{16}$$

Replace the output circuit with the Thevenin equivalent circuit as shown in Figure 7, and calculate the gain with the aid of the inverting gain equation as shown in equation 17.

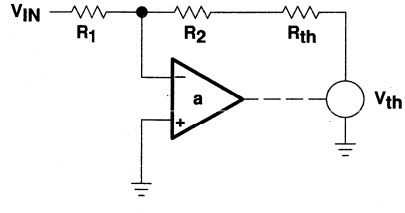


Figure 7. Thevenin's Theorem Applied to T Network

Substituting the Thevenin equivalents into equation 17 yields equation 18.

$$-\frac{V_{OUT}}{V_{TH}} = \frac{R_2 + R_{TH}}{R_1} \tag{17}$$

$$-\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + R_{TH}}{R_1}\left(\frac{R_3 + R_4}{R_4}\right) = \frac{R_2 + (R_3 \parallel R_4)}{R_1}\left(\frac{R_3 + R_4}{R_4}\right) \quad (18)$$

Algebraic manipulation yields equation 19.

$$-\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + R_3 + \frac{R_2 R_3}{R_4}}{R_1} \quad (19)$$

Specifications for the circuit you are required to build are an inverting amplifier with an input resistance of 10K (R_G = 10K), a gain of 100, and a feedback resistance of 20K or less. The inverting op amp circuit can not meet these specifications because R_F must equal 1000K. Inserting a *T* network with R_2 =R_4= 10K and R_3 = 485K does meet the specifications.

Video Amplifiers

Video signals contain high frequencies, and they use coaxial cable to transmit and receive signals. The cable connecting these circuits has a characteristic impedance of 75 Ω. To prevent reflections, which cause distortion and ghosting, the input and output circuit impedances must match the 75 Ω cable.

Matching the input impedance is simple for a noninverting amplifier because its input impedance is very high; just make R_{IN} = 75 Ω. R_F and R_G can be selected as very high values, in the kΩ range, so that they have minimal affect on the impedance of the input or output circuit. A matching resistor, R_M, is placed in series with the op amp output to raise its output impedance to 75 Ω; a terminating resistor, R_T, is placed at the input of the next stage to match the cable.

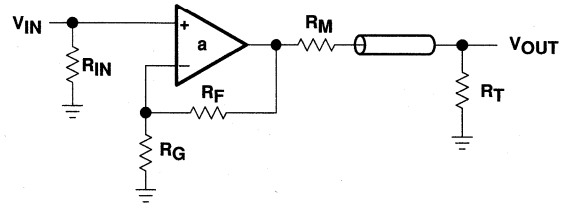


Figure 8. Video Amplifier

The matching and terminating resistors are equal in value, and they form a voltage divider of 1/2 because R_T is not loaded. Very often R_F is selected equal to R_G so that the op amp gain equals two. Then the system gain, which is the op amp gain multiplied by the divider gain, is equal to one (2 × 1/2 = 1).

Capacitors

Capacitors are a key component in a circuit designer's tool kit, thus a short discussion on evaluating their affect on circuit performance is in order. Capacitors have an impedance of $X_C = 1 \div (2\pi fC)$. Note that when the frequency is zero the capacitive impedance (also known as reactance) is infinite, and that when the frequency is infinite the capacitive impedance is zero. These end-points are derived from the final value theorem, and they are used to get a rough idea of the affect of a capacitor. When a capacitor is used with a resistor, they form what is called a break-point. Without going into complicated math, just accept that the break frequency occurs at $f = 1/2\pi$ RC and the gain is –3 dB at the break frequency.

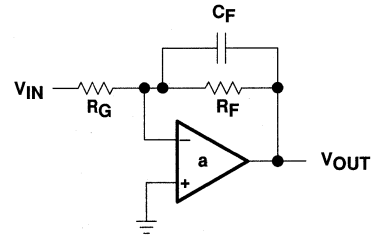


Figure 9. Low-Pass Filter

The low pass filter circuit has a capacitor in parallel with the feedback resistor. The gain for the low pass filter is given in equation 20.

$$\frac{V_{OUT}}{V_{IN}} = -\frac{X_C \parallel R_F}{R_G} \tag{20}$$

At very low frequencies $X_C \Rightarrow \infty$, so R_F dominates the parallel combination in equation 20, and the capacitor has no effect. The gain at low frequencies is $-R_F/R_G$. At very high frequencies $X_C \Rightarrow 0$, so the feedback resistor is shorted out, thus reducing the circuit gain to zero. At the frequency where $X_C = R_F$ the gain is reduced to half or –3 dB because equal impedances in parallel equal half the value of either impedance.

Connecting the capacitor in parallel with R_G where it has the opposite effect makes a high pass filter. Equation 21 gives the equation for the high pass filter.

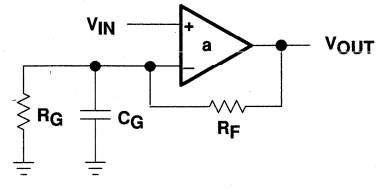


Figure 10. High-Pass Filter

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_F}{X_C \parallel R_G} \tag{21}$$

At very low frequencies $X_C \Rightarrow \infty$, so RG dominates the parallel combination in equation 21, and the capacitor has no effect. The gain at low frequencies is $1+R_F/R_G$. At very high frequencies $X_C \Rightarrow 0$, so the gain setting resistor is shorted out thus increasing the circuit gain to maximum.

This simple technique is used to predict the form of a circuit transfer function rapidly. Better analysis techniques are presented in more advanced application notes for those applications requiring more precision.

Conclusions

When the proper assumptions are made, the analysis of op amp circuits is straightforward. These assumptions, which include zero input current, zero input offset voltage, and infinite gain, are not an unrealistic assumption because the new op amps make them true in many applications.

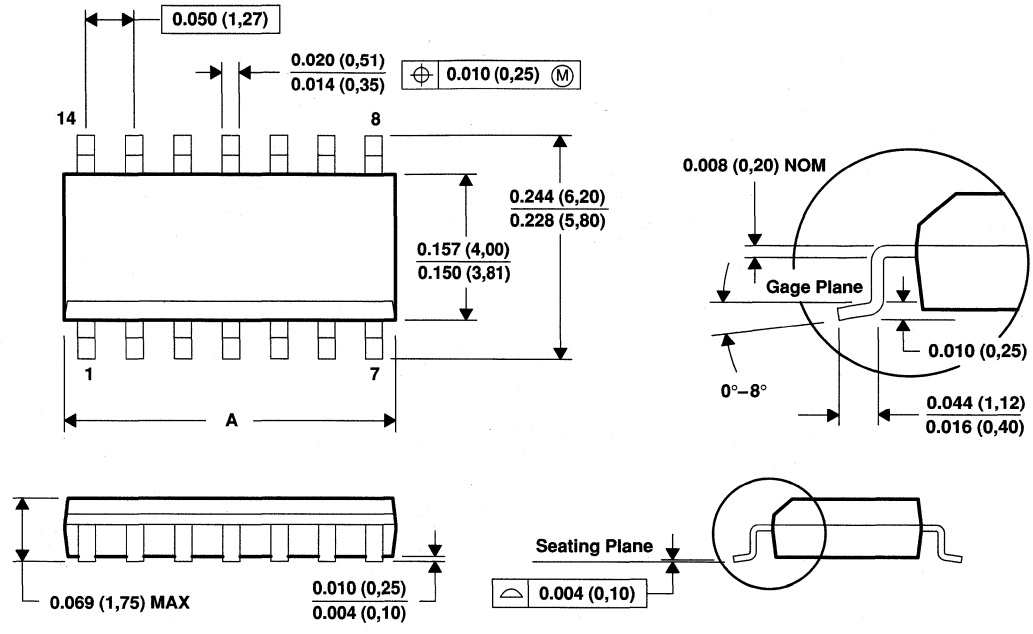
When the signal is comprised of low frequencies, the gain assumption is valid because op amps have very high gain at low frequencies. When CMOS op amps are used, the input current is in the femto amp range; close enough to zero for most applications. Laser trimmed input circuits reduce the input offset voltage to a few micro volts; close enough to zero for most applications. The ideal op amp is becoming real; especially for undemanding applications.

The math required for ideal op amp analysis is not rigorous, thus most people should be able to analyze simple op amp circuits. The more advanced applications require complex op amp circuits, but there are many of these shown in the applications literature. Grab a TI op amp and have fun.

Contents

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



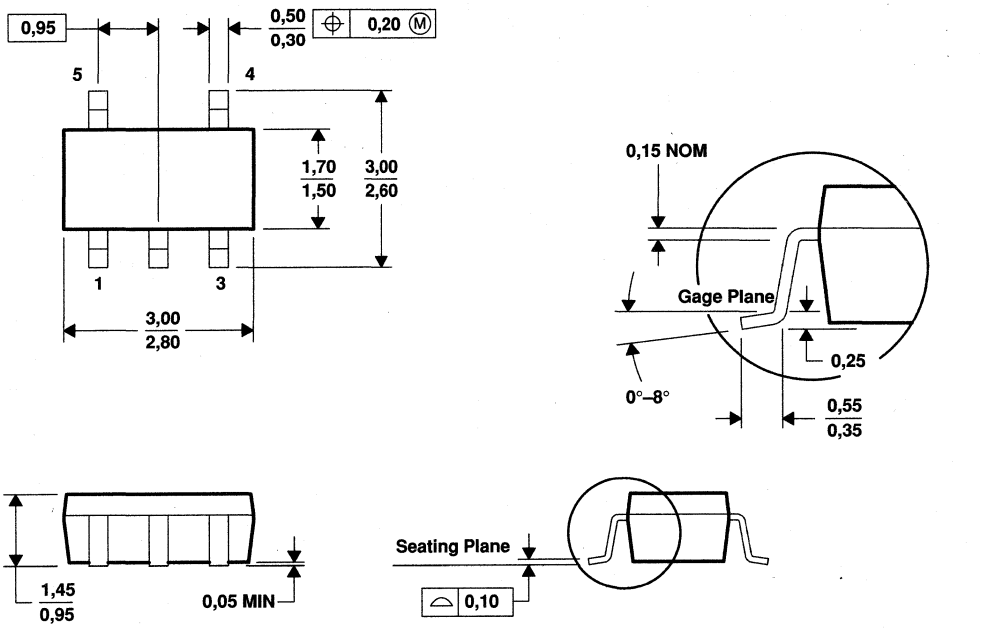
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL INFORMATION

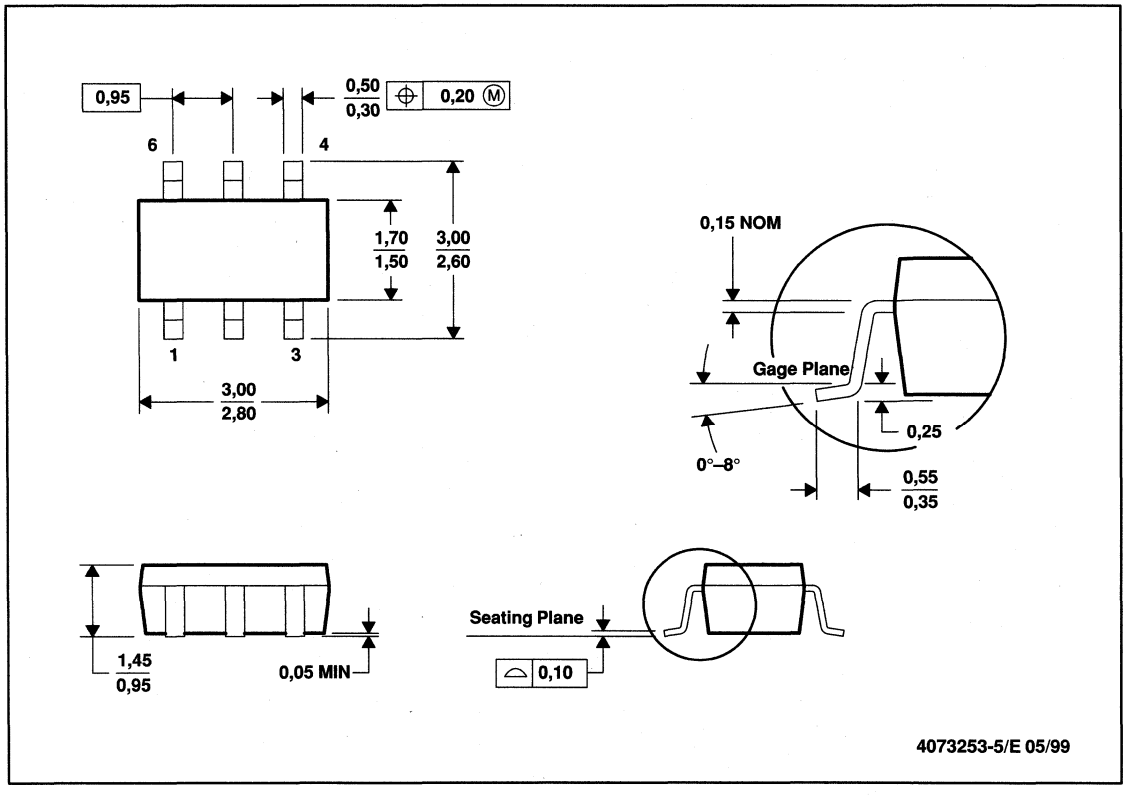
DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178

MECHANICAL INFORMATION

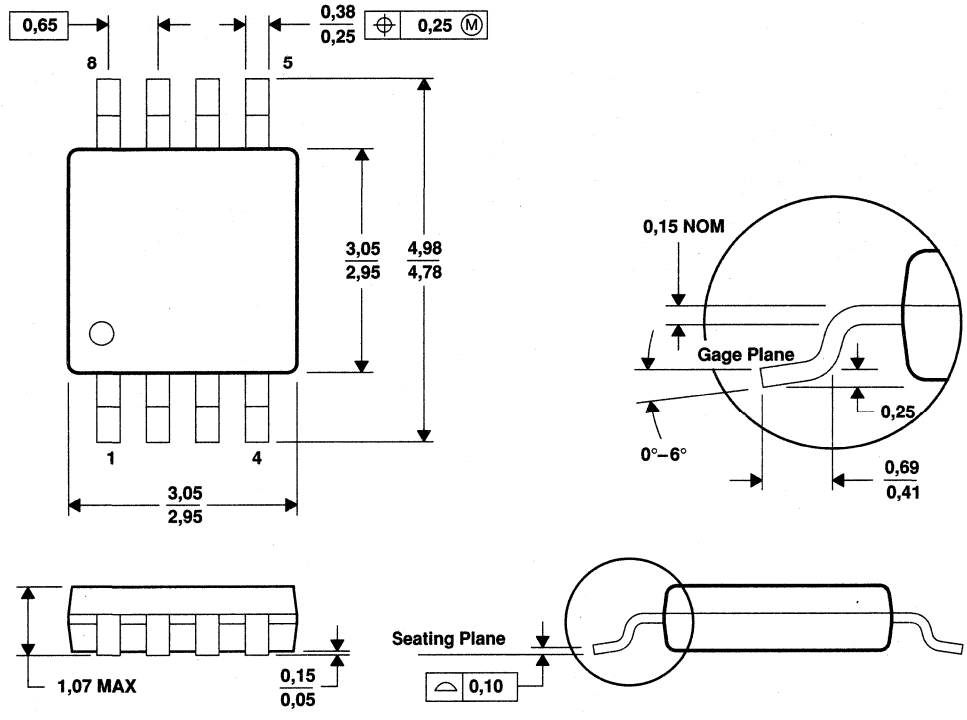
DBV (R-PDSO-G6) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

MECHANICAL INFORMATION

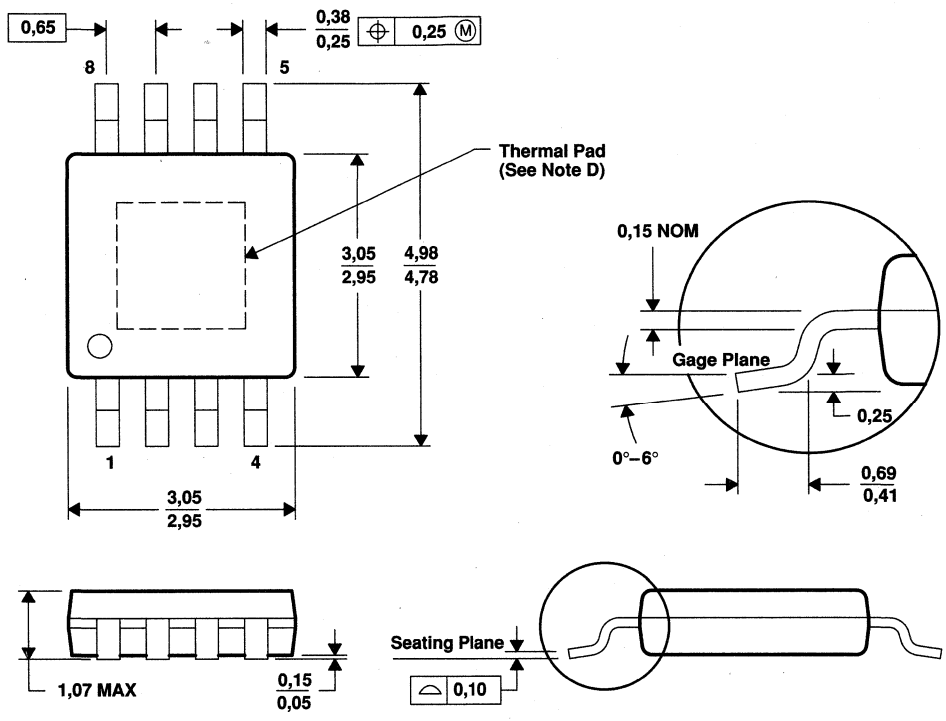
DGK (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187

MECHANICAL INFORMATION

DGN (S-PDSO-G8) **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

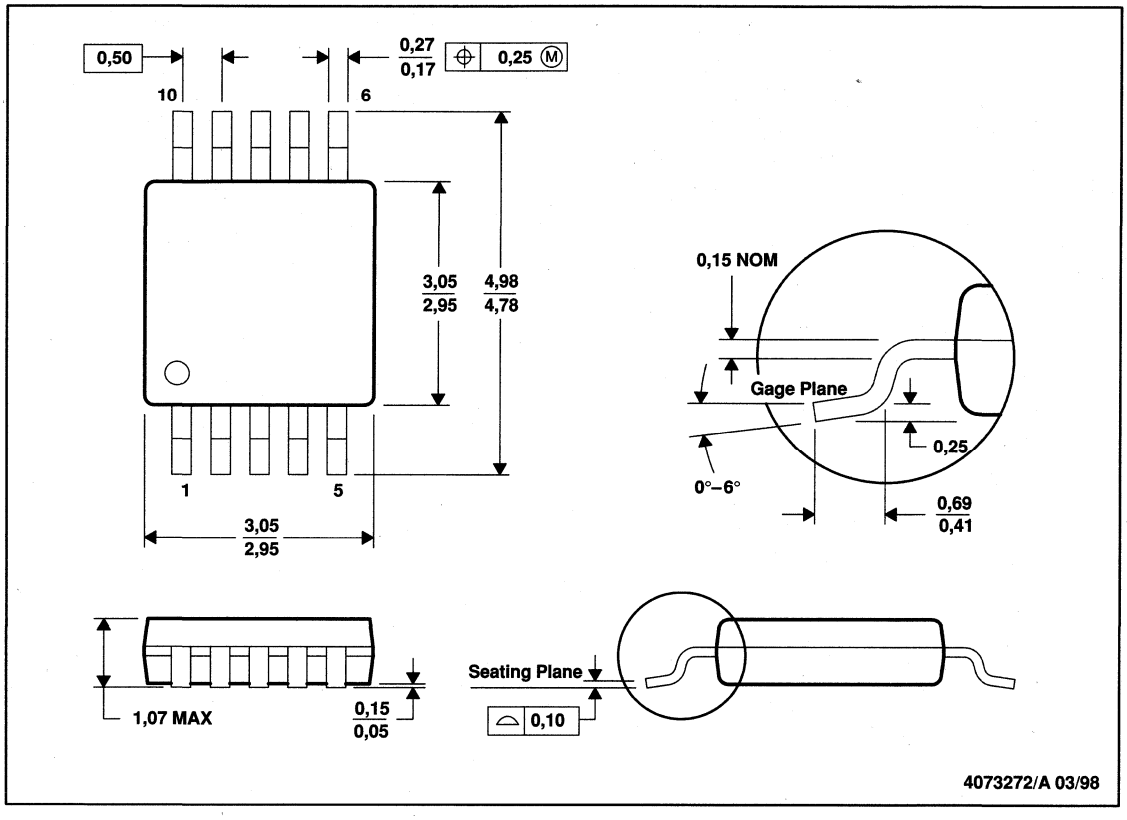


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads. The dimension of the thermal pad is 68 mils (height as illustrated) × 70 mils (width as illustrated) (maximum). The pad is centered on the bottom of the package.
E. Falls within JEDEC MO-187

PowerPAD is a trademark of Texas Instruments Incorporated.

MECHANICAL INFORMATION

DGS (S-PDSO-G10) **PLASTIC SMALL-OUTLINE PACKAGE**

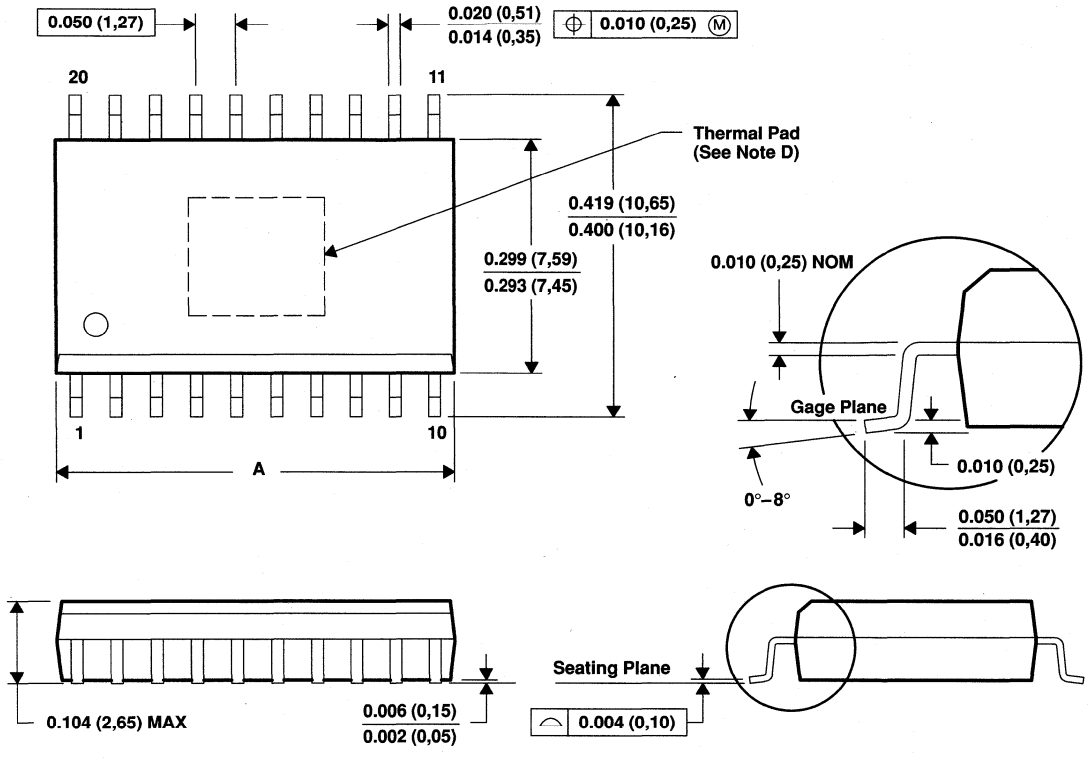


NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

MECHANICAL INFORMATION

DWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

20 PINS SHOWN



DIM \ PINS **	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4147575/A 04/98

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.

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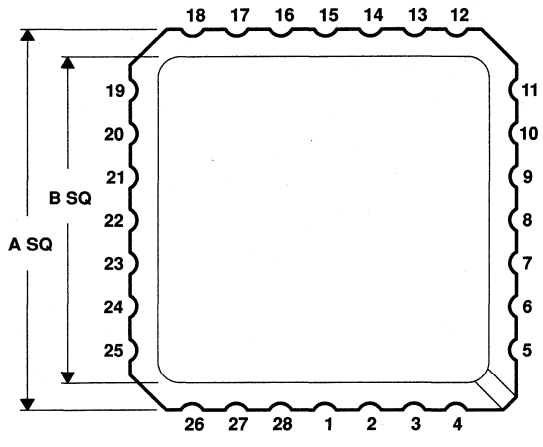
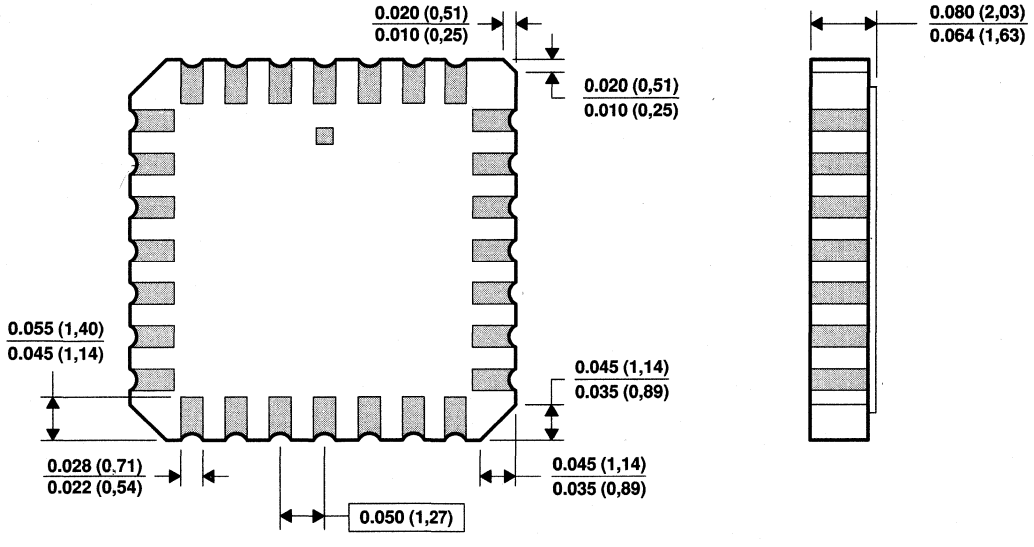
MECHANICAL INFORMATION

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINALS SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

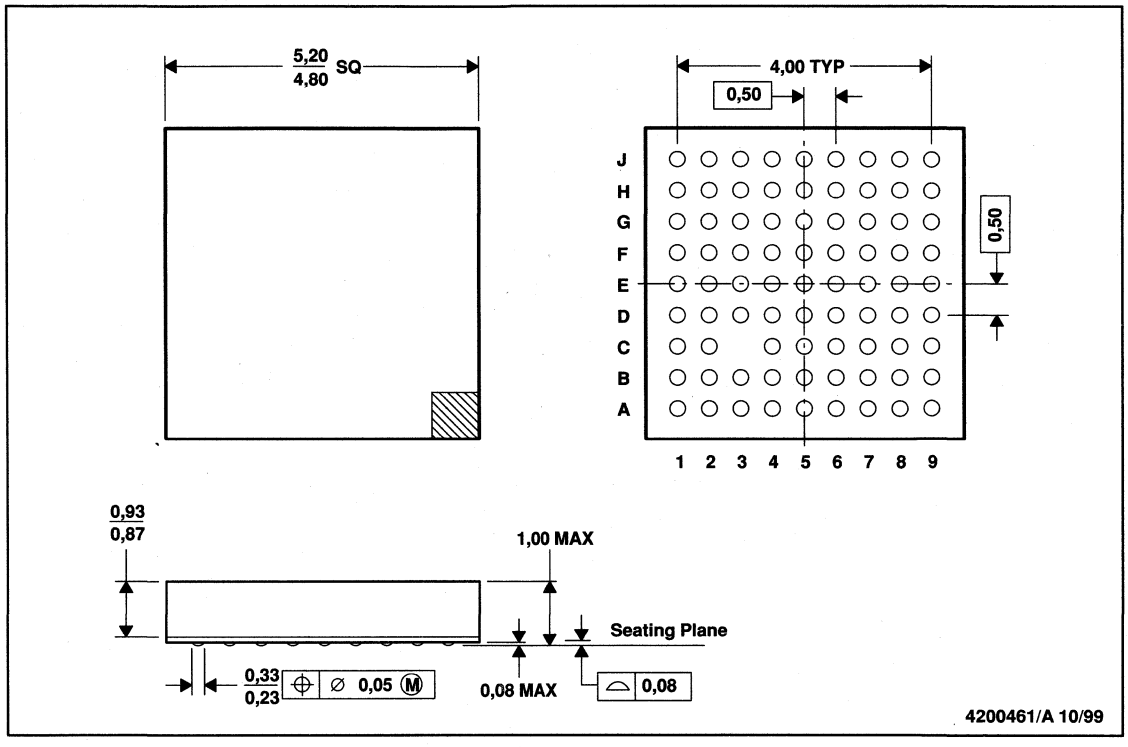


4040140/C 11/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold-plated.
E. Falls within JEDEC MS-004

MECHANICAL INFORMATION

GQE (S-PLGA-N80) **PLASTIC LAND GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior LGA™ configuration

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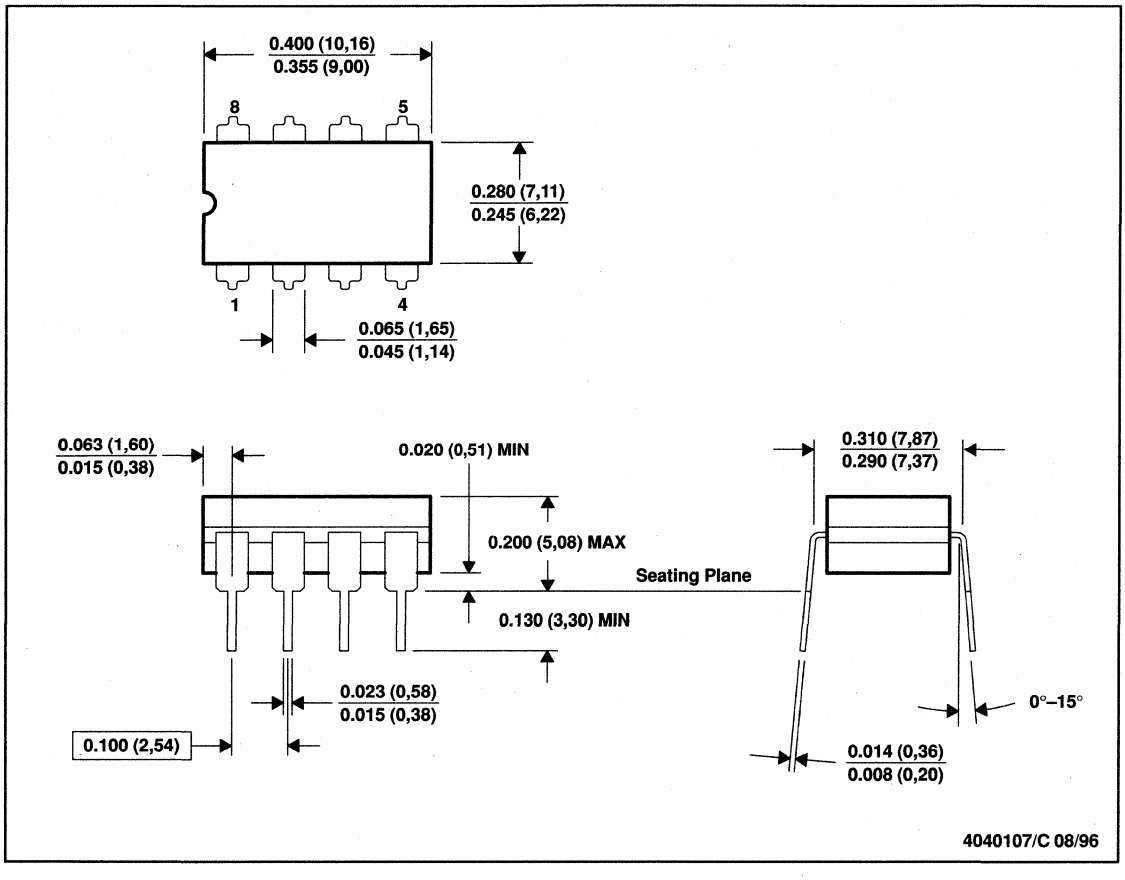
MECHANICAL INFORMATION

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**

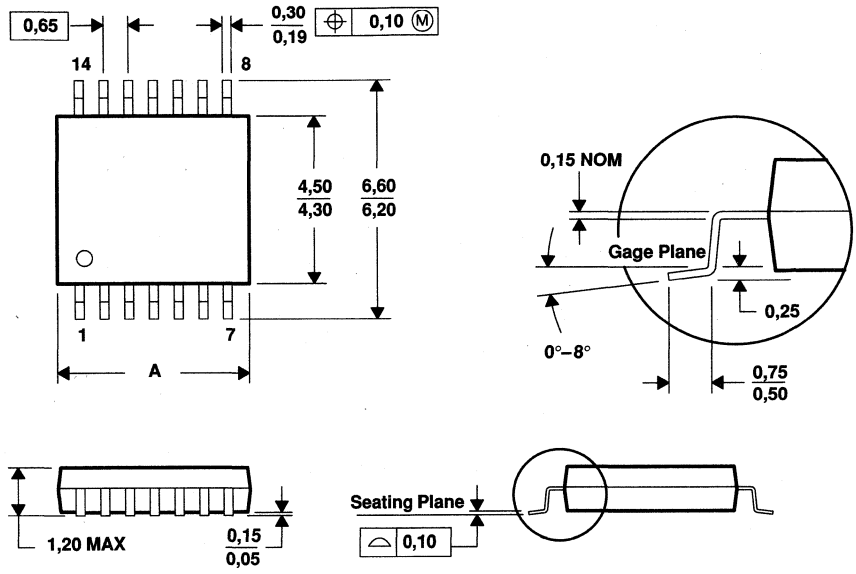


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

MECHANICAL INFORMATION

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

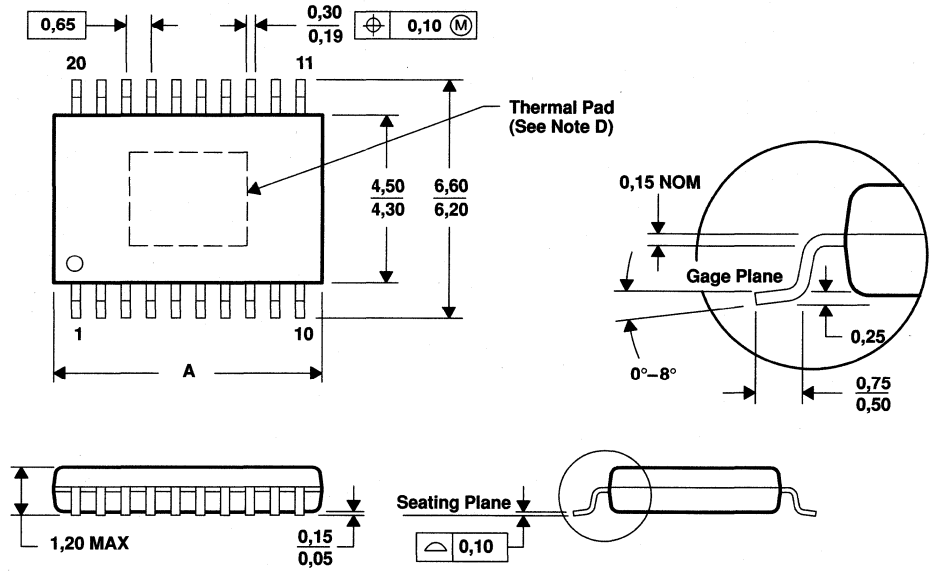
4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

MECHANICAL INFORMATION

PWP (R-PDSO-G)** **PowerPAD™ PLASTIC SMALL-OUTLINE**

20 PINS SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/F 10/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions.
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-153

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India	000-117	-800-800-1450
Indonesia	001-801-10	-800-800-1450
Korea	001-800-8800-6800	-
Malaysia	1-800-800-011	-800-800-1450
New Zealand	000-911	-800-800-1450
Philippines	105-11	-800-800-1450
Singapore	800-0111-111	-800-800-1450
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